iC-PVL LINEAR OFF/ON-AXIS BATTERY-BUFFERED HALL MULTITURN ENCODER

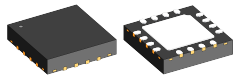
FEATURES

- Integrated Hall sensors with automatic gain and offset control
- For magnetic scales of 1.0 up to 5.0 mm pole width and diametric magnets
- Current consumption of only 2 µA to 30 µA in typ. applications
- Tracking speed of up to 24 m/s (1.5 mm poles) or 15 000 rpm (32 pole pairs)
- Configurable multiturn counting up to 40 bits
- Adjustable period count per revolution: FlexCount® logic for 1 to 256 pole pairs
- Serial, parallel and incremental singleturn operating modes
- SSI multiturn data output with error, warning, parity, and synchronization bits
- Multiturn preset by pin or command
- I²C master function for initial boot-up from EEPROM
- I²C slave function for controller operation
- Supply voltage of 3.0 V to 5.5 V
- Automatic low-power operation on backup battery
- Overspeed, battery and RAM (CRC) monitoring
- Space-saving 16-pin QFN package

APPLICATIONS

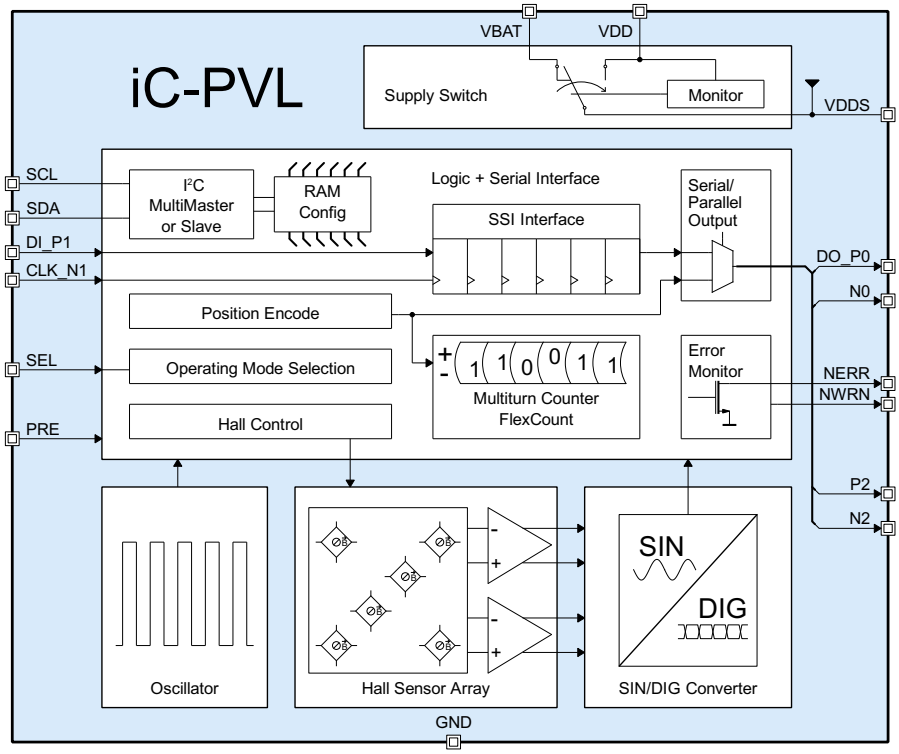
- Absolute hollow-shaft position encoders
- Absolute on-axis position encoders
- Gearless revolution counting
- Linear position sensors
- Metering applications
- Battery-powered portable equipment

PACKAGES



QFN16
4 mm x 4 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-PVL is an ultra low power magnetic encoder, used for linear and off-axis multiturn position sensing. On main power shutdown, iC-PVL automatically switches to battery supply and continues scanning the position.

iC-PVL operates with pole wheels or linear scales with a pole width of 1.0 mm up to 5.0 mm. Due to various operating modes, iC-PVL can work with iC-Haus singleturn encoders (e.g. iC-MU Series, iC-MHM, iC-MNF, iC-TW29 etc.), as stand-alone SSI or incremental encoder, or links to embedded controllers via I^2C.

The Hall signal processing stage is designed for ultra low power applications and can be configured to support angular accelerations up to 180 000 rad/s^2 with 16 magnetic periods per revolution. The maximum magnetic signal frequency is 8 000 Hz. This corresponds to a rotational frequency of 30 000 rpm for magnetic scales with 16 pole pairs. With higher demands on acceleration, the power consumption increases. The maximum supported acceleration is configurable, therefore an optimal trade-off between power consumption and supported acceleration can be individually chosen to meet the demands of the target application.

iC-PVL reads its configuration from an external EEPROM via an I^2C interface with multimaster support. Among others, the bit length for multiturn and synchronization data, the interface mode, the maximum supported acceleration and the usage of error or parity bits can be configured. The configuration read-in is triggered by the preset pin PRE. A pulse on this pin resets the device and reads a new configuration from the EEPROM. The multiturn counter is preset to a configurable value (default 0).

The configuration RAM and multiturn counter value are protected against bit errors by an 8 bit CRC. Additionally, an error is generated on excessive speed or acceleration. An integrated battery monitor is used to signalize an empty battery as error. If an error is detected, it is displayed at output NERR and via the error bit in the SSI communication protocol. Additionally, a low battery voltage is indicated at output NWRN. Optionally, this warning can be transmitted in the serial data stream.

Besides linear position encoding, iC-PVL is also used for off-axis scanning of magnetic pole wheels or on-axis scanning of diametric cylindrical magnets. In these applications, a certain number of magnetic north-south field periods may be interpreted as one mechanical revolution. The FlexCount® circuitry offers this functionality. By electrically emulating the characteristics of a gear box, a transmission is freely programmable. For instance, 1-256 magnetic periods can be interpreted as one mechanical revolution.

The iC-PVL multiturn encoder comes in a space-saving QFN16 package. This allows its integration in existing encoder systems or the design of smaller encoders.

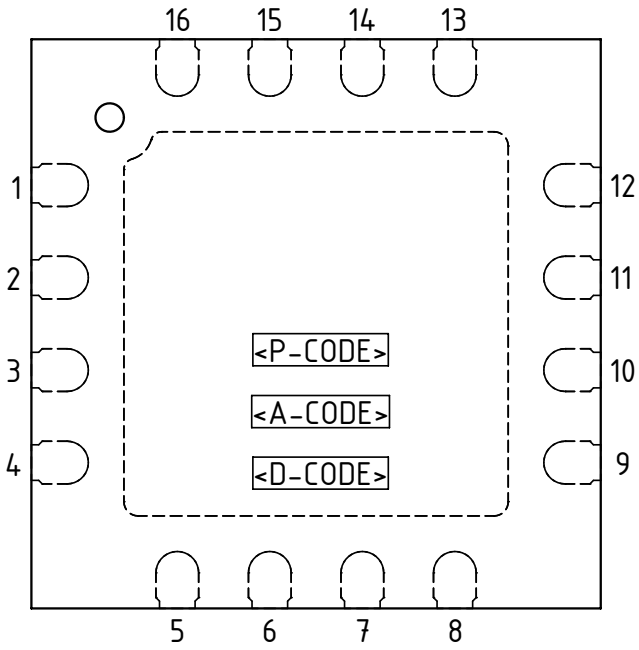
General notice on application-specific programming
Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

The performance of iC-PVL in application is impacted by system conditions like quality of the magnetic target and its adjustment, field strength and stray fields, temperature and mechanical stress.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION
QFN16 4 mm x 4 mm (top view)

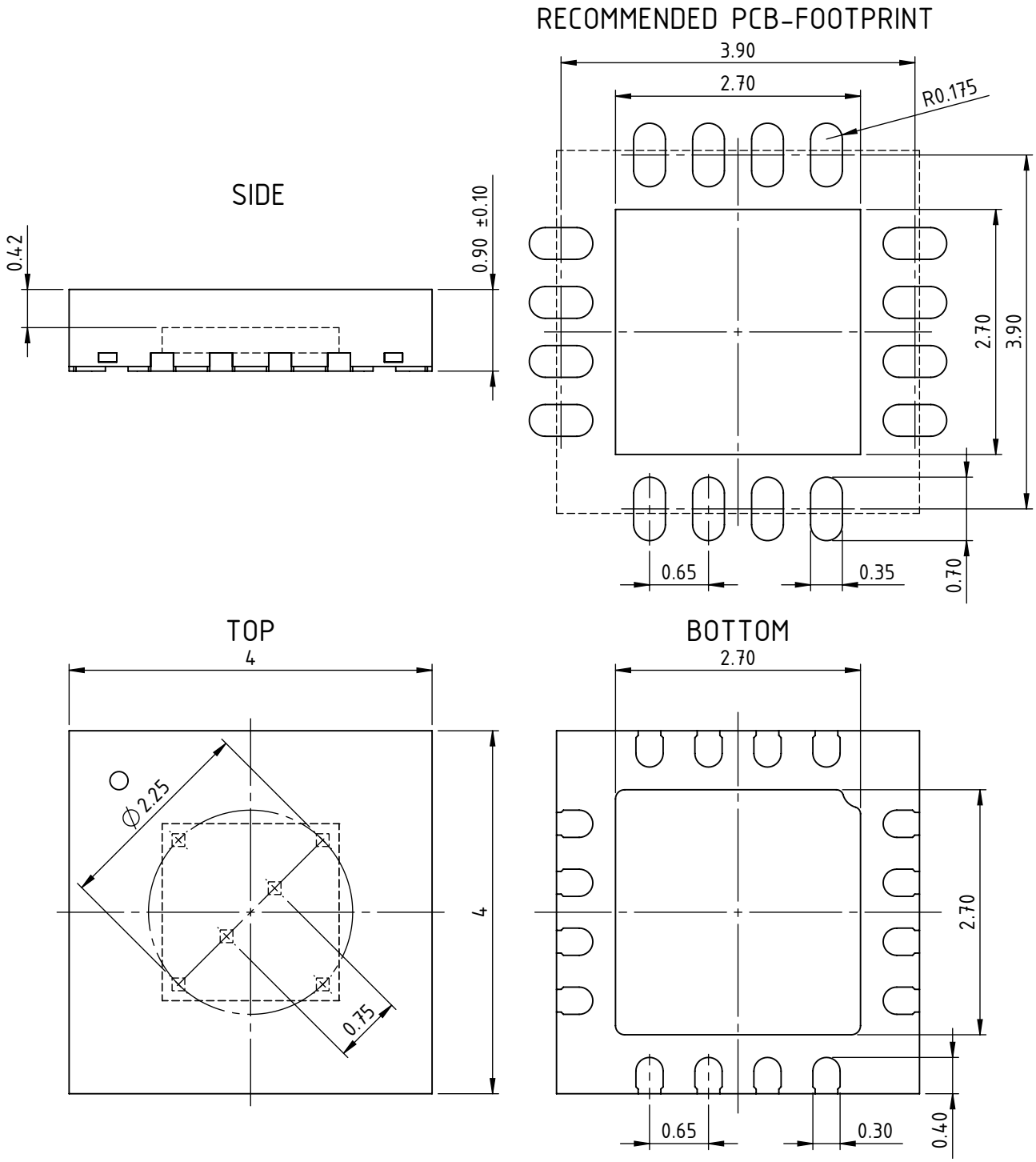


PIN FUNCTIONS

No.	Name	Function
1	SEL	Mode Select Input[1)] Low: Battery buffered counter with serial readout High: 3 bit parallel complementary output Shorted to PRE input : I²C slave mode
2	PRE	Preset Trigger Input
3	NERR	Error Output (active low)
4	SDA	I²C Interface, Data Line
5	GND	Ground
6	VBAT	Battery Supply Voltage Input (typ. 3.6 V) [2)]
7	VDDS	Switched Supply Voltage Output
8	VDD	+3.0 V to 5.5 V Main Supply Voltage Input
9	N2	Parallel Position Output MSB, Incremental Output B, Parallel Mode Output Bit 2 (neg. logic)
10	P2	Parallel Position Output MSB-1, Incremental Output A, Parallel Output Bit 2 (pos. logic)
11	N0	Parallel Position Output LSB, Parallel Mode Output Bit 0 (neg. logic)
12	NWRN	Battery Warning Output (active low)
13	DO_P0	Multiturn Interface, Data Output, Parallel Mode Output Bit 0 (pos. logic)
14	CLK_N1	Multiturn Interface, Clock Line, Parallel Mode Output Bit 1 (neg. logic)
15	DI_P1	Multiturn Interface, Data Input, Parallel Mode Output Bit 1 (pos. logic)
16	SCL	I²C Interface, Clock Line
	BP	Backside paddle [3)]

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
1) Do not leave pin open.
2) Connect pin to VDD if iC-PVL is used without a backup power source (e.g. battery, supercap).
3) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS QFN16 4x4



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad).

dra_qfn16-4x4-4_pvl_0_pack_1, 15:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V(VDD)	Voltage at VDD		-0.25	6	V
G002	V(VBAT)	Voltage at VBAT	VDD > Von: VBAT < VDD + 1.0 V	-0.25	6	V
G003	V(VDDS)	Voltage at VDDS		-0.25	6	V
G004	V()	Voltage at SCL, SDA, DI_P1, CLK_N1, DO_P0, N0, NERR, NWRN, P2, N2, PRE, SEL		-0.25	6	V
G005	I(VDD)	Current in VDD		-10	50	mA
G006	I(VBAT)	Current in VBAT		-10	50	mA
G007	I(VDDS)	Current in VDDS		-10	50	mA
G008	I(GND)	Current in GND		-50	10	mA
G009	I()	Current in SCL, SDA, DI_P1, CLK_N1, DO_P0, N0, NERR, NWRN, P2, N2, PRE, SEL		-30	30	mA
G010	Vd()	ESD Susceptibility at All Pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Junction Temperature		-40	150	°C
G012	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating conditions:
VDD = 3.0...5.5 V, VBAT < VDD + 1.0 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package QFN16	-40		125	° C
T02	Rthja	Thermal Resistance Chip/Ambience	QFN16-4x4 surface mounted to PCB according to JEDEC 51 thermal measurement standards		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDD = 3.0...5.5 V, VBAT < VDD + 1.0 V, Tj = -40...125 °C, fslow calibrated to 34 kHz with IBIAS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	V(VDD)	Permissible Main Supply Voltage	VDD must never go below GND - 0.25V	3.0		5.5	V
002	I(VDD)	Supply Current in VDD	Tj = 27 °C, no load	1.5	4.0	6.0	mA
003	V(VBAT)	Permissible Battery Voltage	if VDD > Von: VBAT < VDD + 1 V	3.0	3.6	5.5	V
004	Iavg(VBAT)	Average Supply Current in VBAT in Battery State	VBAT = 3.6 V, Tj = 27 °C, VDD < Von depending on fmag and A_MAX, see Table 34	1	10	800	µA
005	Iavg(VBAT)	Average Supply Current in VBAT in PowerOn or Sleep State (POWON_ST = 1 or SLEEP_ST = 1)	VBAT = 3.6 V, VDD < Von Tj = 27 °C, Tj = 125 °C,		0.3 1.0	1.0 3.0	µA µA
006	Ispike()	Peak Current in VDD and VBAT	tspike < 5 µs		4.0	10.0	mA
007	Vc()hi	Clamp Voltage hi at All Pins	Vc()hi = V() - VDDS, I() = +1 mA	0.3	0.7	1.6	V
008	Vc()lo	Clamp Voltage lo at All Pins	I() = -1 mA	-1.6	-0.7	-0.25	V
009	tconfig	Power-Up Time After Preset	VDD > 3 V, initializing from EEPROM start address = 0x00, data valid start address = 0xA0, data valid		12 50	20 100	ms ms
010	C(VBAT)	External Bypass Capacitor at Pin VBAT	ceramic capacitor placed as close as possible to the pin	1			µF
011	C(VDDS)	External Bypass Capacitor at Pin VDDS	ceramic capacitor placed as close as possible to the pin	100			nF
012	C(VDD)	External Bypass Capacitor at Pin VDD	ceramic capacitor placed as close as possible to the pin	100			nF
013	C(PWR)	Additional Bypass Capacitor at VDD Power Supply	ceramic capacitor placed on PCB to reduce power supply switching transients	10			µF
Magnetic Signal Conditioning							
101	Hext	Permissible Magnetic Field Strength	at chip surface	10		100	kA/m
102	Bext	Permissible Magnetic Flux Density	at chip surface in air	12.5		125	mT
103	fmag	Magnetic Input Frequency	VDDS = 3.0 V, tested via electrical input			8	kHz
104	frot	Permissible Rotation of Pole Wheel with	16 pole pairs 32 pole pairs 64 pole pairs			30000 15000 7500	rpm rpm rpm
105	vmax	Permissible Movement Speed (Linear)	1.5 mm pole width (3 mm magnetic period)			24	m/s
106	dsens	Diameter of Hall Sensor Circle	measured from center of each Hall plate, ONAX = 1		2.25		mm
107	hpac	Sensor-to-Package-Surface Distance	QFN16		0.4		mm
108	Ht	Differential Magnetic Field Strength Working Threshold for Position Tracking	ATHR = 0x00 ATHR = 0x01 ATHR = 0x02 ATHR = 0x03 device is in NoMagnet working state if field strength (at chip surface) is below this value		2.5 1.25 0.625 5.0		kA/m kA/m kA/m kA/m
109	Bt	Differential Magnetic Flux Density Working Threshold for Position Tracking	ATHR = 0x00 ATHR = 0x01 ATHR = 0x02 ATHR = 0x03 flux value at chip surface in air		3.13 1.56 0.78 6.25		mT mT mT mT
Oscillator Frequencies							
301	fslow	Slow Oscillator Frequency	calibrated to 34 kHz with IBIAS	32	34	36	kHz
302	ffast	Fast Oscillator Frequency	fslow calibrated with IBIAS	4.0	6.0	8.0	MHz
Supply and Battery Monitoring							
401	Von	Switch to VDD Supply (VDD Power On)	increasing voltage at VDD; VBAT > 3.0 V	2.8	2.9	3.0	V

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDD = 3.0...5.5 V, VBAT < VDD + 1.0 V, Tj = -40...125 °C, fslow calibrated to 34 kHz with IBIAS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
402	Voff	Switch Back to Battery Supply (VDD Power Off)	decreasing voltage at VDD; VBAT > 3.0 V	2.7	2.8	2.9	V
403	Vhys	Hysteresis (VDD Switch)	Vhys = Von - Voff	25	100	150	mV
404	Vt()err	Battery Monitoring Error Threshold Voltage	BAT_THR = "11" BAT_THR = "10" BAT_THR = "01" BAT_THR = "00"	2.65 2.75 2.85 2.95	2.75 2.85 2.95 3.05	2.85 2.95 3.05 3.15	V V V V
405	Vt()wrn	Battery Monitoring Warning Threshold Voltage	BAT_THR = "11" BAT_THR = "10" BAT_THR = "01" BAT_THR = "00"	2.75 2.85 2.95 3.05	2.85 2.95 3.05 3.15	2.975 3.075 3.175 3.275	V V V V
406	Vew	Difference Battery Error-to-Warning	ΔVew = Vt()wrn - Vt()err	40	100	175	mV
Digital Outputs: DI_P1, CLK_N1, DO_P0, N0, P2, N2							
501	Vs()hi	Saturation Voltage hi	Vs()hi = VDDS - V(), I() = -1.6 mA	0.05		0.4	V
502	Vs()lo	Saturation Voltage lo	I() = 1.6 mA	0.05		0.4	V
503	Isc()hi	Short-Circuit Current hi	VDDS = 3.0 V, V() = GND	-15		-4	mA
504	Isc()lo	Short-Circuit Current lo	VDDS = 3.0 V, V() = VDDS	4		15	mA
505	tr()	Rise Time	CL = 30 pF			50	ns
506	tf()	Fall Time	CL = 30 pF			50	ns
EEPROM Interface: SCL, SDA							
601	Vt()hi	Input Threshold Voltage hi			1.7	2	V
602	Vt()lo	Input Threshold Voltage lo		0.8	1.4		V
603	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi - Vt()lo	75	200	500	mV
604	Vs()lo	Saturation Voltage lo	I() = 1.6 mA	0.05		0.4	V
605	Isc()lo	Short-Circuit Current lo	VDDS = 3.0 V, V() = VDDS	8		30	mA
606	Ipu()	Pull-Up Current	V() = 0 V...VDDS - 1 V	-1000	-300	-30	µA
607	fclk(SCL)	I^2C Output Frequency at SCL			f_{fast} / 128		kHz
Error Monitoring Output: NERR, NWRN							
701	Vs()lo	Saturation Voltage lo	I() = 1.6 mA	0.05		0.4	V
702	Isc()lo	Short-Circuit Current lo	VDDS = 3.0 V, V() = VDDS	4		15	mA
Digital Inputs: DI_P1, CLK_N1							
801	Vt()hi	Threshold Voltage hi			1.7	2	V
802	Vt()lo	Threshold Voltage lo		0.8	1.4		V
803	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	75	200	500	mV
804	Ipd()	Pull-Down Current	V() = 1 V...VDDS	2	30	100	µA
Mode Select Input: SEL							
901	Vt()hi	Threshold Voltage hi			1.7	2	V
902	Vt()lo	Threshold Voltage lo		0.8	1.4		V
903	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	75	200	500	mV
Preset Input: PRE							
A01	Vt()hi	Threshold Voltage hi			60	75	%VDD
A02	Vt()lo	Threshold Voltage lo		30	40		%VDD
A03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	0.7	1.0	1.4	V
A04	Ipd()	Pull-Down Current	V() = 1 V...VDDS, SEL = GND	10	120	300	µA
A05	t_{preset}	Length of Preset Pulse on PRE Pin		2			µs
Serial Interface to Singleturn Sensor, SSI and Chain Mode							
B01	tp()	Propagation Delay: Clock Edge vs. DO Output		10		100	ns
B02	tout	Timeout	fslow calibrated via IBIAS	15	25	35	µs

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDD = 3.0...5.5 V, VBAT < VDD + 1.0 V, Tj = -40...125 °C, fslow calibrated to 34 kHz with IBIAS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Parallel Encoder Mode							
C01	tprocess	Processing Time (Parallel Output)	see Figure 14		10	30	µs

OPERATING REQUIREMENTS: Serial and Parallel Interface

Operating conditions:
VDD = 3.0...5.5 V, VBAT < VDD + 1.0 V, Tj = -40...125 °C, fslow calibrated to 34 kHz with IBIAS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Serial Interface SSI Mode						
I001	t_{wait}	SSI Request after VDD Power-on		10		µs
I002	t_{req}	Request Signal lo Level Duration		250		ns
I003	t_C	Permissible Clock Period	due to Elec. Char. B02	500	$2 \cdot t_{out}$	ns
I004	f_C	Permissible Clock Frequency	due to Elec. Char. B02	$1/(2 \cdot t_{out})$	2	MHz
I005	t_{L1}	Clock Signal hi Level Duration		250		ns
I006	t_{L2}	Clock Signal lo Level Duration		250		ns
I007	t_{frame}	Cyclic Multiturn Data Frame Request Interval		85		µs
I^2C Slave Mode Direct Access						
I010	t_C	Permissible Clock Period	due to Elec. Char. B02			
I011	t_{wait}	I^2C Request after VDD Power-on		10		µs
I012	f_{scl}	Permissible Input Clock Frequency	I^2C standard mode with timeout Elec. Char. B02	$1/(2 \cdot t_{out})$	100	kHz
Parallel Encoder Mode (SEL = High)						
I013	t_{start}	Length of Start Pulse on PRE Pin	see Figure 14 on Page 26	2		µs
I014	t_{cycle}	Time Between Two Consecutive Sensor Read Cycles	see Figure 14 on Page 26	30		µs
Serial Interface Chain Mode						
I015	f_C	Permissible Clock Frequency	due to Elec. Char. B02	$1/(2 \cdot t_{out})$	1	MHz
I016	t_C	Permissible Clock Period	due to Elec. Char. B02	1	$2 \cdot t_{out}$	µs
I017	t_{L1}	Clock Signal hi Level Duration		500		ns
I018	t_{L2}	Clock Signal lo Level Duration		500		ns

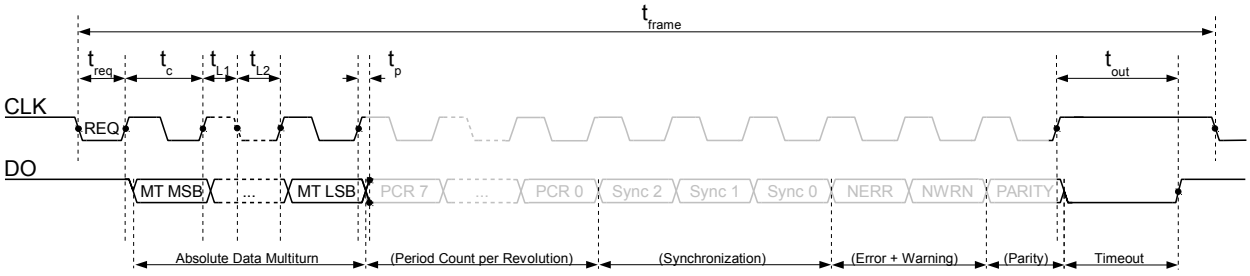


Figure 1: I/O line signals of the serial interface in SSI mode (INT_MODE = 0)

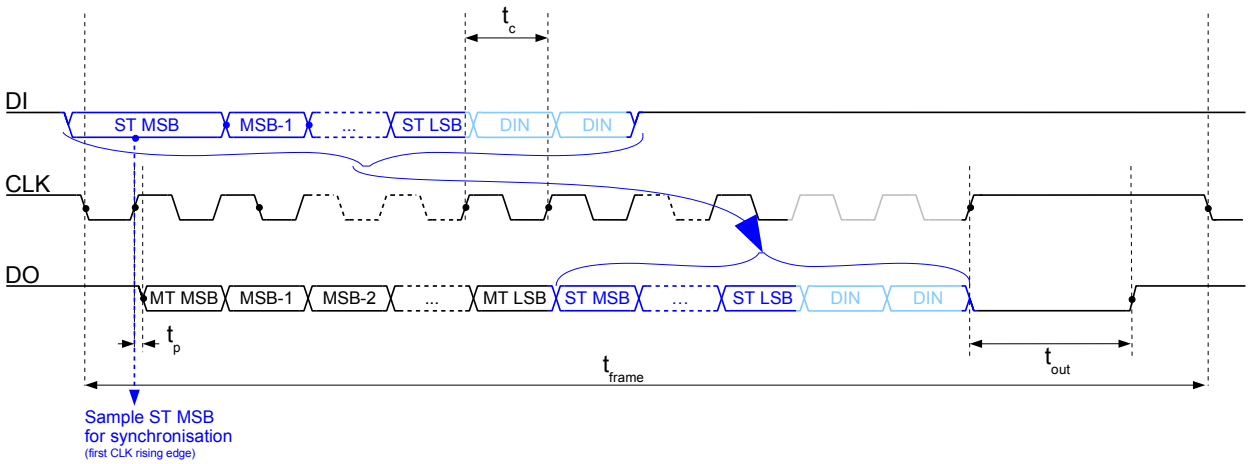


Figure 2: I/O line signals of the serial interface in Chain Mode (INT_MODE = 1). **Note:** Chain Mode can only be used in specific system setups. Extended system requirements apply.

CONFIGURATION PARAMETERS

Hall Sensor Signal Conditioning
DIR: Code Direction (P. 22)
OS: Electrical Offset Multiturn to Singleturn (P. 22)

Serial Interface
INT_MODE: Serial Interface Operating Mode (P. 23)
MT_GRAY: Multiturn Output Data Format (P. 23)
ST_GRAY: Singleturn Input Data Format (P. 23)
MT_BW: Bit Width of Multiturn Data and Counter (P. 23)
SYNC_BW: Synchronization Bit Width (P. 23)
PCR: Period Count per Revolution (P. 21)
PCR_OUT: PCR Output Mode (P. 21)
EN_ERR: Error Bit Transmission Enable (P. 24)
EN_PAR: Parity Bit Transmission Enable (P. 24)

Bias and Oscillators
IBIAS: Bias Current; Oscillator Frequency Calibration (P. 34)
A_MAX: Maximum Angle Acceleration (P. 33)

Battery Monitor
BAT_MON: Battery Monitoring Enable (P. 32)
EN_WRN: Low Battery Warning Enable (P. 24)
BAT_THR: Battery Monitor Thresholds (P. 32)

Miscellaneous
POLEWID: Pole Size of Magnetic Scale (P. 20)
ONAX: On-Axis Magnetic Scanning (P. 21)
ABQUAD: AB Quadrature Output (P. 24)
HYS: Hysteresis (P. 24)
I2C_POS: Enable I^2C Position Readout (P. 28)
MT_PREL: Multiturn Counter Preload Value (P. 25)
CHIP_REL: Chip Release (P. 28)
ATHR: Field Amplitude Threshold Value (P. 29)
NOMAG: NoMagnet Detection (P. 29)

CRC Checksums
CRC_CFG: Checksum for Chip Configuration (0x00-0x05) (P. 27)
CRC_CTR: Checksum for MT_PREL (0x07-0x0B) (P. 27)

REGISTER MAP (EEPROM)

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interface and Hall Signal Processing								
0x00	EN_PAR		EN_ERR		DIR	ST_GRAY	MT_GRAY	INT_MODE
0x01	OS			MT_BW				
0x02	PCR							
Battery Monitor, Bias and Oscillators								
0x03	EN_WRN	BAT_MON	A_MAX			IBIAS		
Miscellaneous								
0x04	0	NOMAG		ATHR		ONAX	POLEWID	
0x05	I2C_POS	PCR_OUT	SYNC_BW		BAT_THR		HYS	ABQUAD
CRC Configuration (inverted)								
0x06	CRC_CFG(7:0)							
Multiturn Counter: Preload Value								
0x07	MT_PREL(7:0)							
0x08	MT_PREL(15:8)							
0x09	MT_PREL(23:16)							
0x0A	MT_PREL(31:24)							
0x0B	MT_PREL(39:32)							
CRC Counter (inverted)								
0x0C	CRC_CTR(7:0)							

Table 1: Register map EEPROM

REGISTER MAP (I²C slave ID = 0b1100 001)

The I²C slave ID 0b1100 001 allows access to all iC-PVL registers.

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interface and Hall Signal Processing								
0x00	EN_PAR		EN_ERR		DIR	ST_GRAY	MT_GRAY	INT_MODE
0x01	OS			MT_BW				
0x02	PCR							
Battery Monitor, Bias and Oscillators								
0x03	EN_WRN	BAT_MON	A_MAX			IBIAS		
Miscellaneous								
0x04	0	NOMAG		ATHR		ONAX	POLEWID	
0x05	I2C_POS	PCR_OUT	SYNC_BW		BAT_THR		HYS	ABQUAD
CRC Configuration (inverted)								
0x06	CRC_CFG(7:0)							
Multiturn Counter: Current Count (PCR_OUT = 0)					**Multiturn Counter: Current Count (PCR_OUT = 1)**			
0x07	MT_COUNT(7:0)				Current PCR(7:0)			
0x08	MT_COUNT(15:8)				MT_COUNT(7:0)			
0x09	MT_COUNT(23:16)				MT_COUNT(15:8)			
0x0A	MT_COUNT(31:24)				MT_COUNT(23:16)			
0x0B	MT_COUNT(39:32)				MT_COUNT(31:24)			
CRC Counter (inverted)								
0x0C	CRC_CTR(7:0)							
Synchronization Bits (I²C slave mode read only)								
0x0D	0	0	0	0	0	SYNC(2:0)		
0x0E	Reserved							
Chip Release (I²C slave mode read only)								
0x0F	CHIP_REL							
Status Register (I²C slave mode only)								
0x10	PRESET	PDR	BAT_WRN	BAT_ERR	POS_ERR	CTR_ERR	CFG_ERR	STUP_ERR
Command Register (I²C slave mode write only)								
0x11	CMD(7:0)							
Extended Status Register for Working States and Amplitude Monitor (I²C slave mode only)								
0x12	SLEEP_ST	NOMAG_ST	ACTIVE_ST	POWON_ST	Unused	NOMAG_L	MAG_ERR	AMPL_ERR

Table 2: Register map I²C slave ID = 0b1100 001

REGISTER MAP (I²C slave ID = 0b1100 000)

The I²C slave ID 0b1100 000 allows access to the iC-PVL command and status registers only. It is implemented to ensure compatibility with certain iC-Haus singleturn devices.

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status Register (I²C slave mode only)								
0x00	PRESET	PDR	BAT_WRN	BAT_ERR	POS_ERR	CTR_ERR	CFG_ERR	STUP_ERR
Command Register (I²C slave mode write only)								
0x01	CMD(7:0)							
Extended Status Register for Working States and Amplitude Monitor (I²C slave mode only)								
0x02	SLEEP_ST	NOMAG_ST	ACTIVE_ST	POWON_ST	Unused	NOMAG_L	MAG_ERR	AMPL_ERR

Table 3: Register map I²C slave ID = 0b1100 000

OPERATING MODE SELECTION

The input SEL defines the operating mode of iC-PVL. For the default application as battery buffered multiturn counter with serial position readout (SSI Interface), it is mandatory to connect the SEL input to GND potential. In case a three bit parallel and differential position output is desired, a high state at SEL input selects a parallel encoder mode. It is mandatory to connect SEL to a defined high or low potential.

An additional operating mode is activated when SEL is shorted to input PRE. In this mode, the preset pulse does not trigger an EEPROM readout. iC-PVL now behaves as I²C slave and all registers (configuration, position, status and command registers) are accessible via I²C device ID = 0b1100 001 (see Table 6).

The register layout visible via I²C is shown on page 13 for each particular address. Please note that some addresses are read only.

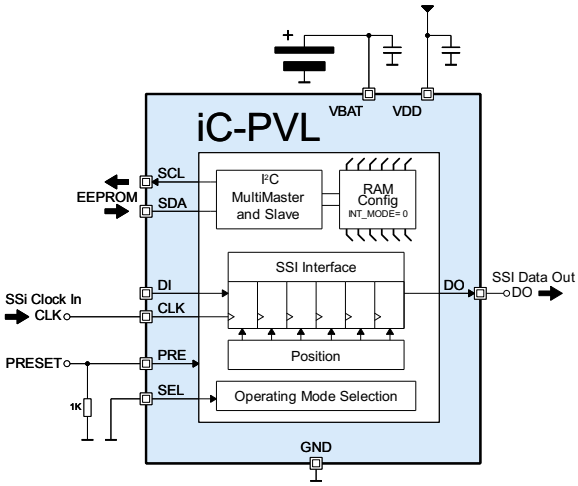


Figure 3: SEL = low: serial interface SSI mode

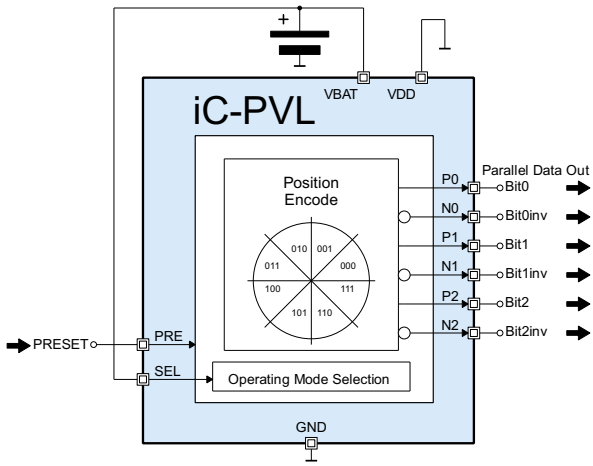


Figure 4: SEL = high: parallel encoder mode

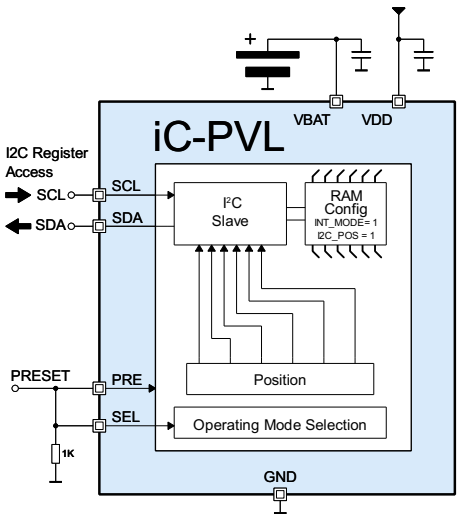


Figure 5: SEL = PRE: I²C slave mode

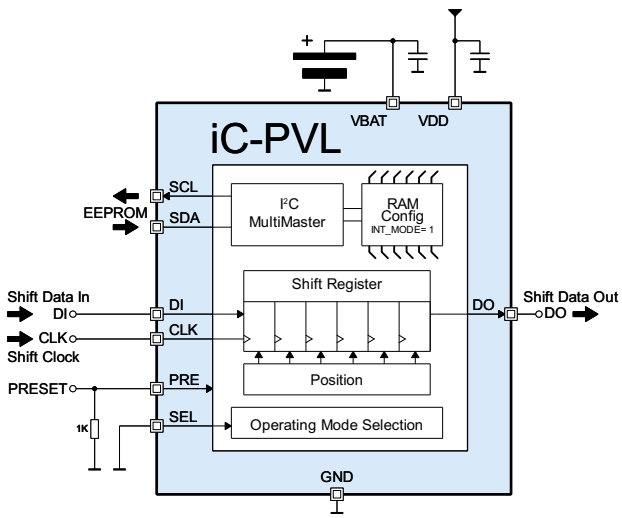


Figure 6: SEL = low: serial interface chain mode. **Note:** Chain Mode can only be used in specific system setups. Extended system requirements apply.

OPERATING MODE SELECTION						
Operating Mode	**Description**	**Pin SEL**	**Parameter INT_MODE (see Table 12)**	**Parameter I2C_POS (see Table 23)**	**I²C Slave Function**	**I²C Master Function (Read E2P cfg...)**
SSI Mode (Fig. 3)	Battery buffered counter with serial readout.	low	0	0	yes (without position readout)	only after preset pulse* or I²C command REBOOT
I²C Slave mode (Fig. 5)	iC-PVL operates as I²C slave, ID = 0b1100 001.	Shorted to PRE	0	1	yes (with position readout)	only after I²C command REBOOT
Parallel Mode (Fig. 4)	3 bit Parallel Encoder Mode, complementary output.	high	-	-	-	-
Chain Mode (Fig. 6)	Battery buffered counter with serial readout. **Note:** Chain Mode can only be used in specific system setups. Extended system requirements apply.	low	1	0	no	only after preset pulse

Table 4: Operating mode selection, configuration settings, available functions

* For iC-PVL W4 or newer: Please refer to the design review on p. 36.

DEVICE WORKING STATES

The iC-PVL operates in different working states according to its configuration and the environmental conditions, especially regarding power supply and magnetic field strength. Table 5 and Figure 7 show their main characteristics and the transitions between the states. These working states do not apply to the Parallel Encoder Operating Mode.

Working State	VDD Supply	Description	Position Tracking	Position Readout	Status Indication	I(VDD)	I(VBAT)
PowerOn	Off	Security state after reset/preset	Off	No		0 mA	typ. 300nA, max. 3µA
PowerOn	On	Security state after reset/preset	Off	No	Error	1 mA	0 mA
Active	On	Normal operation using VDD supply, backup battery is connected	High speed capable	Yes		4 mA	0 mA
Battery	Off	Backup operation using VBAT supply, current consumption depends on rotational speed and parameter A_MAX	High speed capable	Not possible		0 mA	1-800 µA
NoMagnet	On	Low magnetic field amplitude detected	Low speed	Yes	Error	1 mA	0 mA
NoMagnet	Off	Low magnetic field amplitude detected, current consumption defined by parameter A_MAX	Low speed	No		0 mA	1-50 µA
Sleep	On	Sleep state activated via command	Off	No	Error	1 mA	0 mA
Sleep	Off	Sleep state activated via command	Off	No		0 mA	typ. 300nA, max. 3µA

Table 5: Definition of device working states

In states were position readout is marked with <no>, the read action via serial interface SSI/I2C is possible, but the read position is invalid. I.e. the interfaces answers with all position bits = '1'. I2C communication for register operation is possible in all states when VDD supply is on (VDD > V_{on}). For values of V_{on} and V_{off} refer to Elec. Char. No. 401 and 402.

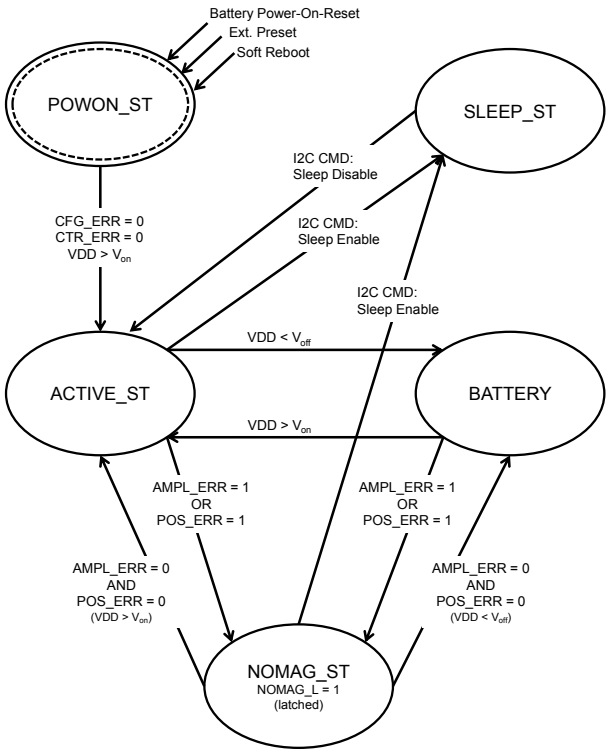


Figure 7: State Diagram

STARTUP BEHAVIOR

As shown in chapter OPERATING MODE SELECTION, iC-PVL can be booted up in four distinct operating modes. These are the SSI Mode, the Parallel Encoder Mode, the I²C Slave Mode and the Chain Mode, respectively. Via SEL, the operating mode is selected according to Table 4. In case of a faulty startup procedure, an error is indicated at pin NERR.

Figure 8 shows the startup procedure of iC-PVL. The procedure starts when a battery supply is available. This would be the case if a battery is newly attached to the encoder system or the battery supply is switched on by an external microcontroller. Alternatively VDD can be connected first followed by connecting the battery. Active battery errors can be removed using the SCLR command.

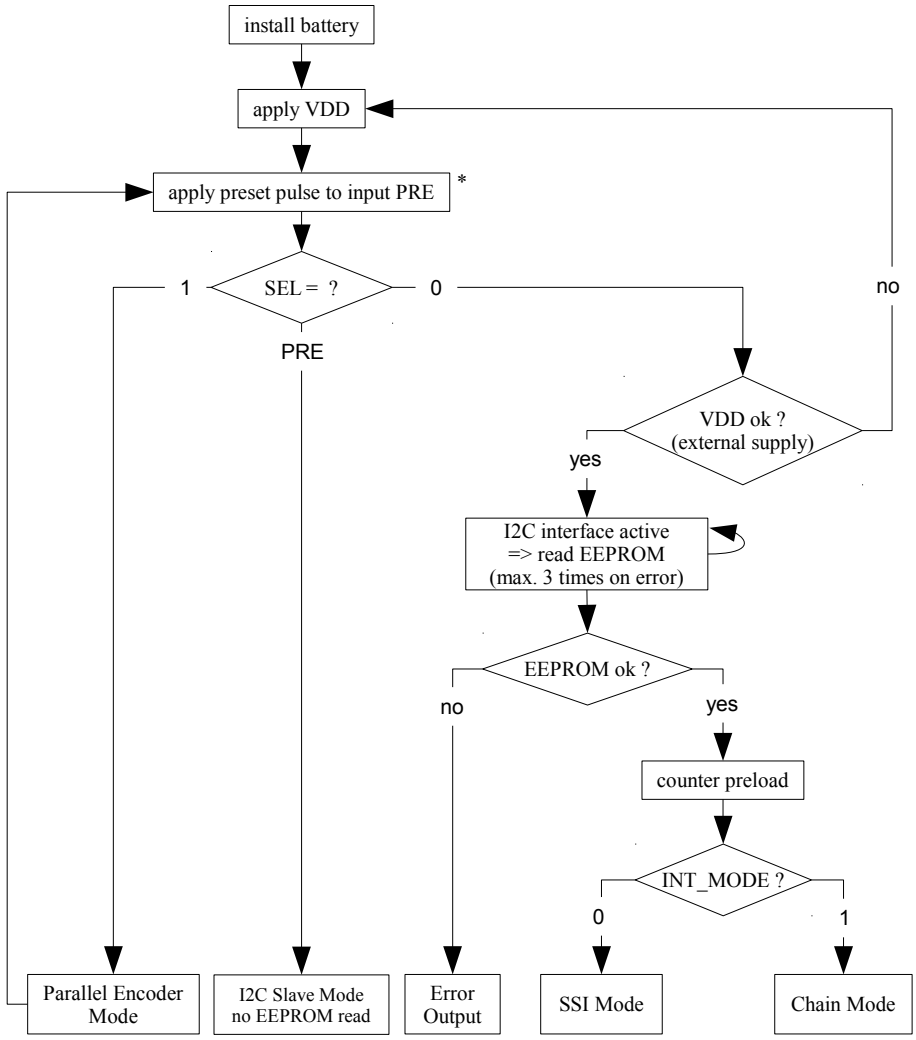


Figure 8: Startup behavior

SSI Mode (SEL = low)

For V(VDD) > V_{on} during the initial startup in SSI mode, a preset pulse is mandatory* and triggers EEPROM readout. VDD supply has to remain above V_{on} for at least t_{config}. The I²C multimaster tries to read the configuration data from an EEPROM connected to SCL and SDA. When the data is read without errors, the iC-PVL operates in SSI Mode or Chain Mode according to the configuration bit INT_MODE and stays in this operating mode as long as the battery supply is above V_{off}. After a third faulty attempt, EEPROM readout is stopped and an error is indicated at pin NERR. Both serial interface modes are further explained on Page 23.

* For iC-PVL W4 or newer: Please refer to the design review on p. 36

I²C communication is possible in this operating mode, but position readout via SSI or I²C is exclusive (refer to I²C SLAVE MODE on Page 28).

I²C slave mode (SEL = PRE)
For V(VDD) > V_{on} during the initial startup in I²C mode, a preset pulse applied simultaneously to the SEL and PRE pin (refer to Figure 5) will set position readout to I²C (setting of I²C_POS is ignored in this case) and suppress a potential EEPROM readout. If this functionality is not required, the preset pulse can be omitted. iC-PVL responds to the I²C device ID = 0b1100 001.

Parallel Encoder Mode (SEL = high)
In Parallel Encoder Mode, an external microcontroller can activate the iC-PVL via the PRE pin in distinct intervals to acquire the current position. The encoded position is valid when all complementary bits have changed their logic value (see Figure 14). After successful position readout, iC-PVL is in ultra low power idle mode. The battery supply may then be switched off.

MAGNETIC SCALE SELECTION

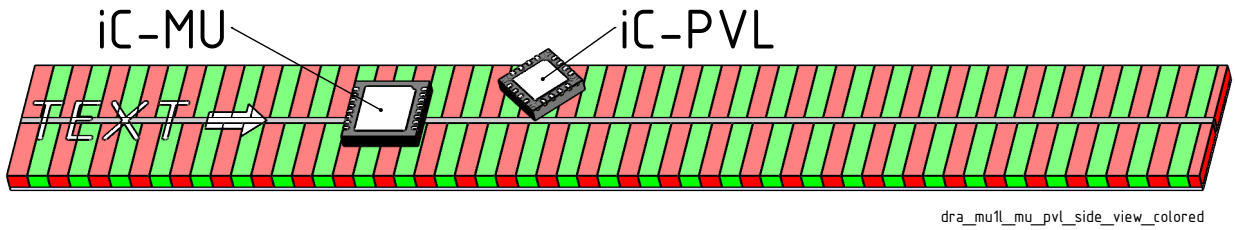


Figure 9: Positioning of iC-PVL on a linear scale (iC-MU nonius type)

iC-PVL is able to scan magnetic pole wheels or linear scales with a pole width of 1 mm to 5 mm. This corresponds to a magnetic period (N-S sequence) of 2 to 10 mm. Due to the diagonal sensor array, iC-PVL is rotated 45° in relation to the magnetic code (see Figures 9, 10, 11).

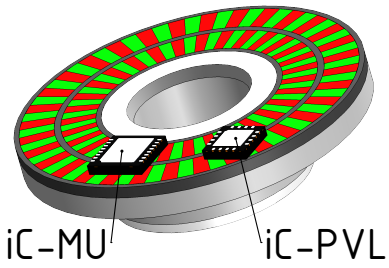


Figure 10: Positioning of iC-PVL on a pole wheel (iC-MU nonius type)

With the recommended differential scanning mode (POLEWID = 0x00), the measurement is highly tolerant to external common mode magnetic stray fields. The ideal pole width in this operating mode is 1.5 mm, but the device is functional with a pole width range of about 1 to 3 mm. This enables iC-PVL to use the same magnetic scale as a linear or off-axis singleturn sensor (e.g. iC-MU (1.28 mm), iC-MU150 (1.5 mm), iC-MHL200 (2 mm)).

POLEWID	Addr. 0x04; bit 1:0		
Code	Pole size	Ideal size	Scanning
0x00	1 - 3 mm	1.5 mm	Off-axis, differential
0x01	4 - 5 mm	4.5 mm	Off-axis, single-ended
0x02	2 - 4 mm	3.0 mm	Off-axis, single-ended
0x03	1 - 3 mm	1.5 mm	Off-axis, single-ended

Table 6: Pole size of magnetic scale

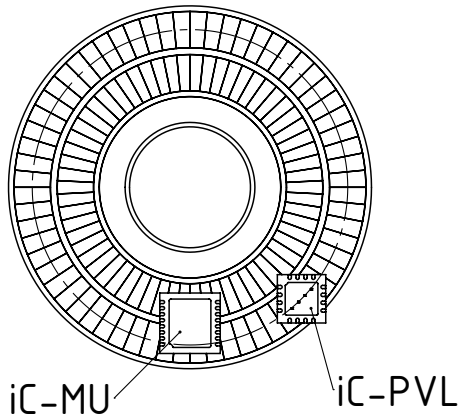


Figure 11: Positioning of iC-PVL on a pole wheel (iC-MU nonius type).

Together with the iC-MU off-axis nonius encoder, a magnetic multiturn encoder can be realized (see iC-PVL AN2) The iC-PVL Hall sensor array is placed over the center line of a magnetic track, e.g. at a radius of 13.375 mm to scan the master track of the MU18S 30-32N magnetic target (see Figure 11). In this case, the corresponding PCR value for 32 magnetic periods (PCR = 0x1F) has to be applied (see Table 7).

In these applications, a certain number of magnetic periods (i.e., north-south pole pairs) may be interpreted as one mechanical revolution. The FlexCount® logic offers this functionality. By electrically emulating the characteristics of a gear box, the gear transmission is freely programmable. 1 to 256 pole pairs can be interpreted as one mechanical revolution. The configuration parameter PCR, period counts per (mechanical) revolution, is used as defined in Table 7.

PCR	Addr. 0x02; bit 7:0
Code	Period counts per revolution
0x00	1
0x01	2
0x02	3
. . .	Code + 1
0xFE	255
0xFF	256

Table 7: Period counts per (mechanical) revolution

By way of example, assume a magnetic code disc with 32 periods. iC-PVL will make a multiturn count every 32 periods. The synchronization bits are distributed evenly over these 32 periods, i.e. the disc is divided in eight sectors.Therefore, one sector consists of 8 periods. While reading the position information, it looks like the iC-PVL would be placed above a normal diametrically polarized magnet. This scheme is also valid for non-binary, decimal or odd counts per revolution.

PCR_OUT	Addr. 0x05; bit 6
Code	Mode
0	No output of PCR in serial data stream
1	PCR is transmitted as 8 LSBs of MT data (Only for PCR > 0x00)

Table 8: Period count per revolution output mode

Alternatively, the current magnetic period of the mechanical revolution can be transmitted in the serial data stream with option PCR_OUT = 1. In this mode, the eight LSBs of the multiturn data are used for PCR output. Unused bits are filled with zeroes. As a consequence, the multiturn counter is limited to 32 bits in this mode. The multiturn, PCR and synchronization information give the exact position of the code disc down to one eighth of a magnetic period.

iC-PVL can also be used for on-axis scanning of a diametric cylindrical magnet. The on-axis scanning mode is activated with the configuration bit ONAX = 1. The sensor circle diameter is specified in Elec. Char. 106. In this mode, setting POLEWID to 0x01 is mandatory for differential scanning.

ONAX	Addr. 0x04; bit 2
Code	Magnetic scanning mode
0	Off-axis (default)
1	On-axis, differential (POLEWID = 0x01 required)

Table 9: Use off- or on-axis magnetic scanning

When iC-PVL is used for on-axis scanning the native zero position is shown in Figure 12 below.

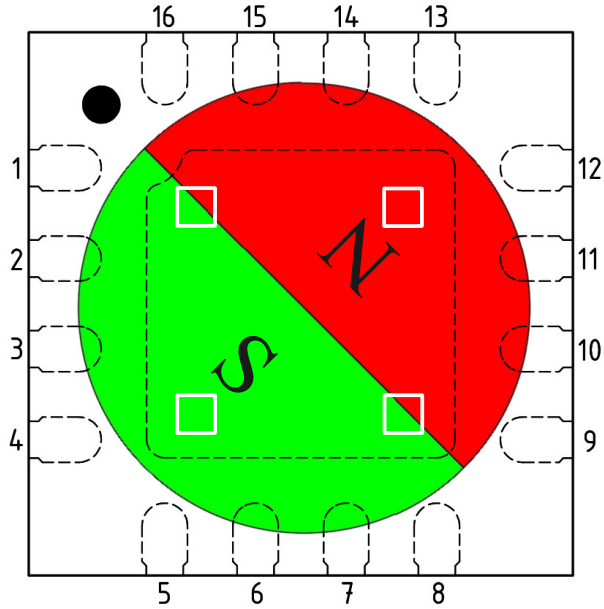


Figure 12: iC-PVL magnet zero position in on-axis mode (ONAX = 1) (top view)

COMPENSATION OF ASSEMBLY: Data Offset and Counting Direction

Assembled together with a magnetic code disc, code wheel, magnetic tape or diametric cylindrical magnet, the integrated Hall sensor signal processing generates a three bit position word, i.e. eight positions per magnetic period. Therefore, the iC-PVL provides up to three synchronization bits to the singleturn sensor in SSI readout mode.

The position can be electrically manipulated to achieve the desired (leading or trailing) phase shift, regardless of the actual mounting position. This is useful if the phase relationship between an additional singleturn iC and the iC-PVL as multiturn encoder is unknown, or the singleturn sensor takes care of the synchronization (SSI mode) and expects a defined phase relationship. An offset value is added to the digitized Hall sensor position according to parameter OS (see Table 10).

OS	Addr. 0x01; bit 7:5
Code	Phase shift
000	0 °, no shift
001	+ 45 ° leading
010	+ 90 ° leading
011	+ 135 ° leading
100	± 180 ° leading or trailing
101	- 135 ° trailing
110	- 90 ° trailing
111	- 45 ° trailing

Table 10: Offset multiturn to singleturn

Note: 0 ° to 180 ° is the ideal range for tolerated values of phase shift between ST and MT. This range is further reduced due to communication, propagation or processing delays for the specific application. Typically, it is reduced by a few degrees, but increases with the signal frequency.

DIR	Addr. 0x00; bit 3
Code	Code direction
0	Normal
1	Inverted

Table 11: Code direction

The counting direction can be easily swapped with the configuration bit DIR. The bit would be typically used to invert the counting direction if the iC-PVL is assembled rotated or flipped.

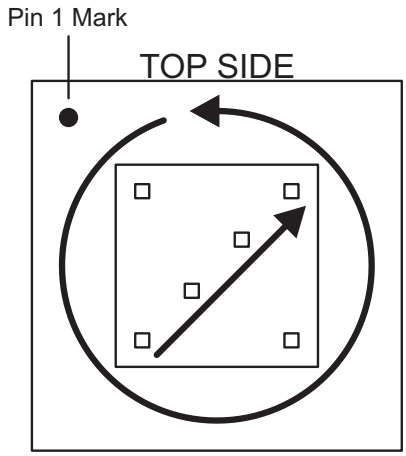


Figure 13: iC-PVL - positive direction of magnet / linear tape movement with DIR = 0. Magnet / linear tape above iC-PVL top side.

SERIAL INTERFACE MODE (SEL = LOW)

iC-PVL can be connected to a singleturn sensor or interpolator via its serial interface. To ensure compatibility with different devices, iC-PVL's serial interface can operate in two distinct modes: standard SSI or in a chain mode.

In SSI mode, iC-PVL replies to a multiturn data request of an SSI protocol master. The master takes care of data synchronization and calculates a consistent absolute position. Data input DI is not used in this operating mode. iC-PVL is compatible with all iC-Haus optical or magnetic singleturn encoders or interpolators featuring a multiturn or absolute data interface. For details refer to the application note iC-PVL AN2. In SSI mode, iC-PVL can also be used as stand-alone magnetic period counter. The position data is output in an SSI compatible protocol (see Figure 16 on Page 35).

In Chain Mode, a singleturn sensor transmits its singleturn position to the data input DI of iC-PVL. In this mode, iC-PVL takes care of synchronization, calculates a consistent absolute position and outputs at data output DO, comparable to a shift register, with MSB first.

The operating mode is set using parameter INT_MODE.

INT_MODE	Addr. 0x00; bit 0
Code	Mode
0	Standard SSI readout mode (SSI mode)
1	Chain Mode*
Note	*) Chain Mode can only be used in specific system setups. Extended system requirements apply.

Table 12: Serial interface operating mode

By default, the iC-PVL expects binary data at input DI, and also outputs its counted multiturn position (and PCR) at DO in binary format. In case one data or both data is required in Gray format, this can be configured by setting the ST_GRAY bit or the MT_GRAY bit, respectively.

ST_GRAY	Addr. 0x00; bit 2
Code	Format
0	Binary code (default for SSI_MODE = 0)
1*	Gray code (lock I²C register access for SSI_MODE = 0)
Note	*) For I²C interlock refer to Page 28

Table 13: Singleturn input data format via port DI (in Chain Mode)

MT_GRAY	Addr. 0x00; bit 1
Code	Format
0	Binary code
1	Gray code

Table 14: Multiturn and PCR output data format via port DO

The internal multiturn counter is 40 bit wide. In applications where smaller counter depths are sufficient or the bit width of the serial interface is limited, the output length of the counter value can be configured with MT_BW as shown in Table 15.

MT_BW	Addr. 0x01; bit 4:0
Code	Bit width
0x00	9 bit
0x01	10 bit
...	...
0x1E	39 bit
0x1F	40 bit
Note:	If PCR_OUT = 1 and PCR > 0x00 the 8 LSBs of the MT data are used to transmit the period count information. Thus the MT counter width is reduced by 8 bit in that case.

Table 15: Bit width of multiturn data and counter

Additionally, iC-PVL can transmit up to 3 synchronization bits, according to configuration parameter SYNC_BW shown in Table 16.

SYNC_BW	Addr. 0x05; bit 5:4	
Code	Bit width	Tolerable phase shift range
00	0 bit	no synchronization bit
01	1 bit	0 ° ... 180 °
10	2 bit	0 ° ... 270 °
11	3 bit	0 ° ... 315 °
Note	*) The values for the tolerable phase shift are typical values and depend on the singleturn iC. Please always consult the singleturn iC specification for the applicable values.	

Table 16: Synchronization bit width and resulting tolerable ideal phase shift

After the transmission of the absolute position and the synchronization information, iC-PVL's serial protocol allows the optional transmission of an error bit, a warning bit and a parity bit.
The error bit signalizes a startup error, a wrong CRC checksum, an empty battery or a position error (e.g. overspeed or magnet loss). Its polarity is configured with parameter EN_ERR shown in Table 17.

The warning bit represents an early battery warning. It indicates a low battery while the system is still functional. The polarity of the warning bit follows the polarity configured with EN_ERR. Details regarding error and status information are explained on Page 29. The optional parity bit finishes the transmission. Its polarity is either even or odd according to parameter EN_PAR.

Finally, the last 8 LSBs of the multiturn data can be used to transmit the period counts revolution in off-axis applications. See Table 8 for details.

The line signals for both interface modes are shown in Figures 1 and 2 on Page 10. Optional bits are greyed-out. The number of transmitted multiturn bits depends on parameter MT_BW.

EN_ERR	Addr. 0x00; bit 5:4
Code	Mode
00	Communication without error bit
01	Calibration mode
10	Communication with additional error bit (negative polarity)
11	Communication with additional error bit (positive polarity)

Table 17: Error bit enable

EN_WRN	Addr. 0x03; bit 7
Code	Mode
0	Communication without warning bit
1	Communication with additional warning bit (polarity as configured via EN_ERR)

Table 18: Warning bit enable

EN_PAR	Addr. 0x00; bit 7:6
Code	Mode
00	Communication without parity bit
01	reserved
10	Communication with additional parity bit (even polarity)
11	Communication with additional parity bit (odd polarity)

Table 19: Parity bit enable

OUTPUTS N0, P2, N2

In serial interface (P. 23) or I^2C slave mode (P. 28), the outputs N0, P2, N2 provide either parallel or incremental position information. A magnetic period is divided in eight sectors. By default, these three bits are output in real-time at N0, P2, N2.

ABQUAD	Addr. 0x05; bit 0			
C.	Mode	N2	P2	N0
0	Parallel position	MSB	MSB-1	LSB
1	Quadrature AB	B	A	none
N.	The output is inverted to the internally generated position.			

Table 20: AB quadrature output

With configuration parameter ABQUAD, a quadrature output can be activated. In this mode, A and B are output at P2 and N2. One magnetic period is interpolated by a factor of two, i.e., two quadrature periods are observed per period corresponding to eight countable edges per period.

For evaluating these outputs, a hysteresis may be desired. Configuration parameter HYS activates a hysteresis of 45°.When active, the synchronization bits of the serial data output also feature a 45° hysteresis.

HYS	Addr. 0x05; bit 1
Code	Mode
0	No angle hysteresis
1	45° hysteresis on direction change

Table 21: Angle hysteresis

MULTITURN COUNTER

In battery buffered serial interface mode (SEL = low) or I²C slave mode, and as long as the system is powered up correctly (i.e. via battery or main supply), iC-PVL will count the multiturn position. Note that there is no counter overflow handling (positive or negative direction).

The internal counter (MT_COUNT) is 40 bits wide and thus can count up to $2^{40} - 1$ revolutions. In SSI mode, the output bit width is defined by MT_BW, so that $2^{MT\_BW} - 1$ revolutions can be counted. Position read-out via SSI or I²C is exclusive, please refer to I²C SLAVE MODE on Page 28.

The counter can be preloaded to a position defined by configuration parameter MT_PREL (Table 22). Refer to Table 15 for the configuration of the counter bit width.

The multiturn counter value as well as the configuration RAM are secured by an eight bit CRC. Refer to chapter I²C MULTIMASTER INTERFACE AND CRC PROTECTION for details.

MT_PREL	Addr. 0x07 - 0x0B;
Code	Value
0x0000000000	0
0x0000000001	1
...	...
0x00000000FF	255
...	...
0xFFFFFFFFFF	$2^{40} - 1$

Table 22: Multiturn preload value

Note: To avoid unwanted jumps of the multiturn position when setting the preset value in iC-PVL RAM, the following procedure is recommended:

1. Send command CMD = 0x04 (SLEEP ENABLE).
2. iC-PVL is now in sleep state, position sensing is halted. This can be checked by reading the status register STATUSEX Bit 7 = 1 (SLEEP_ST).
3. Write the desired multiturn counter value to register MT_PREL.
4. Send command CMD = 0x07 (SLEEP DISABLE).
5. iC-PVL is back in normal operating mode. The multiturn counter is at the desired value with a maximum deviation of +/-1 if the position sits exactly at the full rotation switchover point (SYNC 0→7 or 7→0).

PARALLEL ENCODER MODE (SEL = HIGH)

The input/output signals in parallel encoder mode are described in Figure 14. A start pulse on the PRE line triggers the Hall sensor signal acquisition. The current position is sent as a three bit complementary word via pins P0, N0 to P2, N2. In this mode, the iC-PVL operates with a single power supply on pin VBAT. Pin VDD must be tied to GND, and the select input SEL must be connected to a logic high level, e.g. VBAT (see circuit in Figure 4).

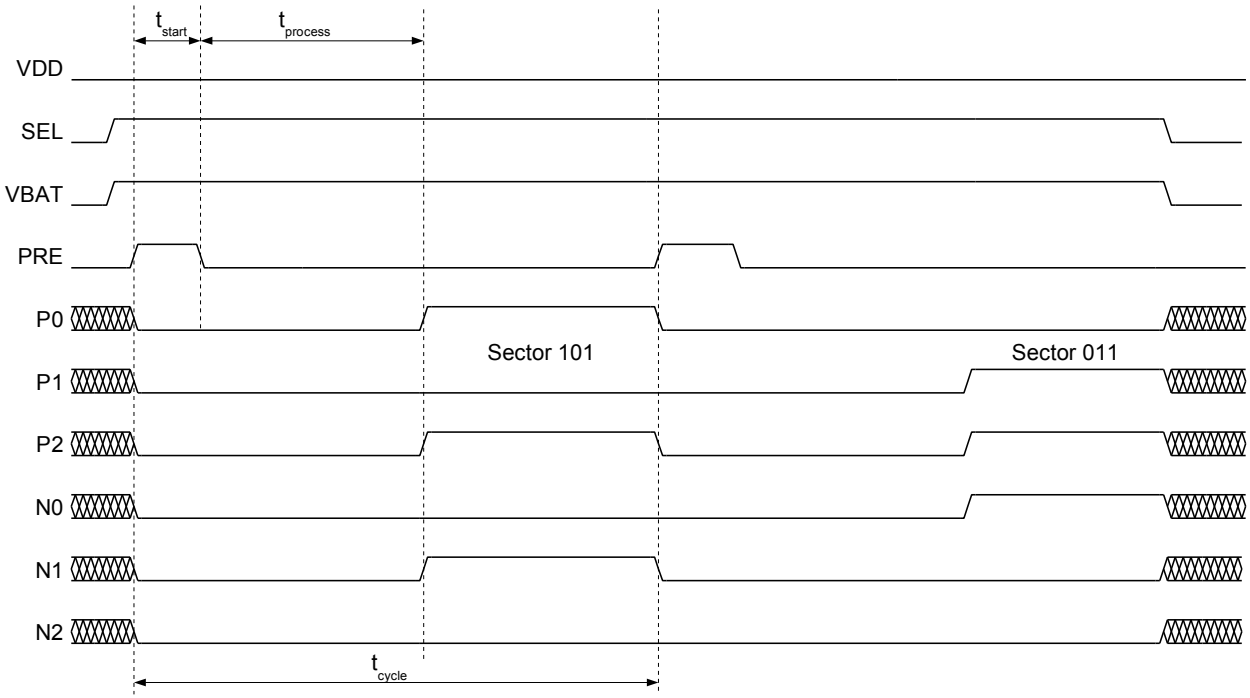


Figure 14: Line signals for parallel encoder mode (3 bit complementary P0-P2 and N0-N2)

I²C MULTIMASTER INTERFACE AND CRC PROTECTION

Pins SCL and SDA form an interface to read an external EEPROM according to the I²C protocol (with at least 128 bytes, e.g. 24C01, 24C02, 24C08 and maximum 24C16, extended address range is not supported). Writing to the EEPROM is not supported.

By default, this EEPROM is used to store the iC-PVL configuration (at addresses 0x00 to 0x0C) according to the register map on Page 12. The configuration is protected against bit errors by an 8-bit CRC checksum. A checksum failure is displayed at output NERR and via the error bit at the end of the SSI data. The multiturn counter preload value is stored in its own configuration area (0x07 - 0x0B) and is also saved with its own CRC on 0x0C. The CRC of the remaining four configuration bytes (0x00 - 0x05) is stored at address 0x06. Both CRC checksums are generated with the polynomial $X^8 + X^5 + X^3 + X^2 + X^1 + 1$ (0x12F). The CRC start value is zero. **Note:** In order to avoid an EEPROM content of all bytes = 0x00 to be a valid configuration, the CRC checksums in addresses 0x06 and 0x0C are stored inverted.

Example of CRC calculation routine:

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x12F;
unsigned char ucCRC;
unsigned char Reg[6]

// Calculate configuration CRC for area 0x00 – 0x05
// stored at 0x06

  ucCRC = 0; // startvalue = 0
  for (int iReg = 0 ; iReg<6; iReg ++) {
    ucDataStream = Reg[iReg];
    for (int i =0; i <=7; i ++) {
      if ( (ucCRC & 0x80) != (ucDataStream & 0x80) )
        ucCRC = (ucCRC << 1 ) ^ iCRCPoly ;
      else
        ucCRC = (ucCRC << 1 ) ;
      ucDataStream = ucDataStream << 1 ;
    }
  }
  Reg[6] = ~ucCRC; // stored inverted
```

Since iC-PVL does only read configuration data, writing EEPROM requires an external programming via pins SCL and SDA (I²C protocol). Refer to circuit on Page 35. In applications with a shared EEPROM, e.g. with iC-MU or iC-MHM, the EEPROM programming of the iC-PVL configuration can be done via the *BiSS* interface of the singleturn IC.

If no EEPROM is available or desired in the application, programming the iC-PVL by a microcontroller (MCU) is possible. As described in the subsequent chapter, the I²C slave mode allows direct read/write access to internal configuration and counter. Alternatively, the MCU may emulate an EEPROM (i.e. an I²C slave), since iC-PVL is acting as a bus master by default. At startup, after a short high pulse at pin PRE, the iC-PVL requests addresses 0x00 to 0x0C from the connected I²C slave. This is done in a combined write/read command as shown in Figure 15, repeating 13 times.

The expected slave address here is 0xA0 or "0b 1010 000", the standard I²C EEPROM address.

Notes: In typical applications, the iC-PVL is used in combination with external encoder, line driver or safety ICs. If several devices try to share one common EEPROM, the default configuration area of iC-PVL may not be usable (addresses 0x00 to 0x0C).
Therefore, the iC-PVL is capable to **boot from different addresses**. The EEPROM is scanned for the unique iC-PVL configuration footprint, i.e. 13 bytes with correct checksums of configuration and counter preload. If no configuration is found at address **0x00 to 0x0C**, the iC-PVL searches at address **0x40 to 0x4C**, then at address **0x80 to 0x8C** and finally at address **0xA0 to 0xAC**.

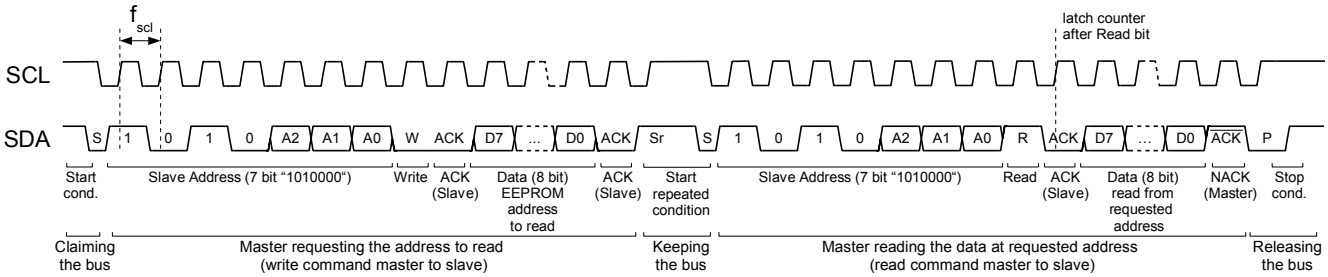


Figure 15: iC-PVL combined write/read command reading one slave address

I²C SLAVE MODE

Additionally to the I²C master interface described in the previous section, iC-PVL will always act as an I2C slave during operation (Vdd > V_{on}).

Two I²C device IDs are available:

- At I²C device ID = 0b1100 001 all iC-PVL's internal registers can be addressed according to the register map in Table 6.
- At I²C device ID = 0b1100 000 only the iC-PVL's status and command registers can be addressed according to the register map in Table 7. All other internal registers are not addressable at this I2C device ID.

The I²C communication protocol described in Figure 15 may be used for read and write register access.

Position readout via SSI or I²C is exclusive and defined by parameter I2C_POS. This bit locks position readout to SSI or I2C exclusively.

I2C_POS	Addr. 0x05; bit 7
Code	Function
0	SSI readout of MT counter only
1	I²C readout of MT counter only

Table 23: Enable I²C or SSI position readout

iC-PVL also features a pin selectable I²C mode (please refer to Figure 5 on page 15 and chapter "STARTUP BEHAVIOUR"). This mode can be used to ensure that iC-PVL does not attempt to read in an EEPROM via the I2C interface at startup. Position readout is automatically and internally set to I²C. The setting of parameter I2C_POS is ignored in that case.

Whenever I²C access to the internal multiturn counter is enabled, it is readable at address 0x07 to 0x0B and protected with a CRC checksum at address 0x0C. Additionally, the three synchronization bits are readable at address 0x0D.

Note: For a consistent position information, it is necessary to read all these position registers in one burst command. The counter and synchronization bits are latched after each read addressing (i.e. read/not write bit = high). At burst command, the addressing for read is done only once, for the first address 0x07. The effective clock edge is marked in Figure 15. If the seven registers are read in seven separate read instructions, the transmitted position may change during readout time and the transmitted position will be inconsistent.

In SSI or I²C slave mode the I²C slave register access can be interlocked. The lock is active if parameter INT_MODE = 0 and parameter ST_GRAY = 1. See also Table 13. Position readout via I²C remains possible.

For chip release verification purposes an identification value is stored under ROM address 0x0F; a write access to this address is not permitted.

CHIP_REL	Addr. 0x0F, bit 7:0 (ROM)
Code	Chip Release
0x04	iC-PVL X1
0x05	iC-PVL W
0x06	iC-PVL W1
0x07	iC-PVL W2
0x09	iC-PVL W4

Table 24: Chip Release

MAGNETIC FIELD AMPLITUDE MONITORING

The magnetic field amplitude is monitored and on detection of magnet loss the NoMagnet working state (NOMAG_ST) is entered in order to save battery power. Status Bit MAG_ERR is set as long as the NoMagnet working state is active.

Note: This feature is intended for encoder systems that can be stored without a magnet (e.g. kit-encoders). In that case, the magnetic field amplitude monitoring automatically reduces the battery power consumption to a minimum and and prevents premature discharge of the battery. If this is not a normal use case, the feature can be disabled by setting parameter NOMAG = 0x03.

Parameter NOMAG determines the trigger conditions. The default setting is 0x00 and triggers the NoMagnet

working state on low magnetic field amplitude or invalid position (POS_ERR = 1). This is the recommended setting if the magnetic field amplitude monitoring feature is used.

Alternatively, the NoMagnet working state can be entered on invalid position only or be completely deactivated. In case of an invalid configuration or device initialization parameter NOMAG is reset to 0x00 by default.

The different working states and transition conditions are described in chapter DEVICE WORKING STATES.

The error bit NOMAG_L is latched and set upon entry of the NoMagnet working state. It can be be cleared by a pin preset or using the status clear (SCLR) or reboot command.

The error bit AMPL_ERR is set whenever the magnetic field amplitude is below the threshold defined by parameter ATHR. Filtering is active, i.e. the bit is set only if the amplitude is low for 8 measurement cycles (approximately 128 ms). This prevents that short (electro-)magnetic interference triggers an error.

ATHR	Addr. 0x04; bit 4:3
Code	Condition
0x00	typ. 2.5 kA/m (default)
0x01	typ. 1.25 kA/m
0x02	typ. 0.625 kA/m
0x03	typ. 5.0 kA/m
Note	see Elec. Char. No. 108

Table 25: Differential field amplitude threshold

NOMAG	Addr. 0x04; bit 6:5
Code	Condition
0x00	NoMagnet state on Low amplitude OR invalid position (default)
0x01	reserved
0x02	NoMagnet state only on invalid position
0x03	NoMagnet detection disabled

Table 26: Behaviour of no NoMagnet detection

ERROR MONITOR, STATUS AND COMMAND REGISTER

The iC-PVL has several error conditions which are stored in the status- and extended status registers. Please also refer to Table 6 and Table 7.

Status Register

Table 27 gives a summary of available error and status bits in the Status Register. All errors except for BAT_WRN are latched and can be acknowledged by overwriting the status byte at the desired position or by sending the SCLR command. If the error is still active, iC-PVL error monitor will set it again immediately, i.e, the error condition is still present.

STATUS	Addr. 0x10; bit 7:0	
Bit	Name	Description
0	STUP_ERR	Startup error
1	CFG_ERR	Internal configuration error
2	CTR_ERR	Internal counter error
3	POS_ERR	Position error
4	BAT_ERR	Battery error
5	BAT_WRN	Battery early warning
6	PDR	Power down reset detected
7	PRESET	Pin preset detected, I^2C REBOOT detected, Sleep mode activated

Table 27: Status byte

STUP_ERR: Startup Error
Erroneous startup procedure, e.g., I^2C stuck-at, EEPROM read error or invalid CRC checksum stored in the EEPROM. No position acquisition is performed. Interfaces are blocked. Please revise configuration and checksums or replace EEPROM. Reboot iC-PVL.

CFG_ERR: Internal Configuration Error
This error is raised when:

- The configuration stored in the internal RAM doesn't match the CRC checksum. This can be caused for example by changing the configuration data without updating the checksum accordingly, or an unexpected level flip of one or more bits in the RAM configuration area. Position is invalid. Reboot iC-PVL.
- After writing to RAM configuration via I2C. CFG_ERR can be cleared by a SCLR command.

CTR_ERR: Internal Counter Error
This error is raised when:

- The value stored in the internal multiturn counter doesn't match the CRC checksum. This can be caused for example by changing the multiturn

counter value without updating the checksum accordingly, or and unexpected level flip of one or more bits in the multiturn counter RAM area. Position is invalid. Reboot iC-PVL.

- After writing to MT_COUNT via I2C. CTR_ERR can be cleared by a SCLR command.

POS_ERR: Position Error
The position encoding observed an unexpected position jump, caused e.g. by excessive speed or excessive acceleration of the magnetic disc or tape. Alternatively, this error bit is set on weak, disturbed magnetic signals or complete loss of magnet. Position is invalid. Optimize magnet position and cross-check angular velocity/acceleration with Table 33. Reboot iC-PVL.

BAT_ERR: Battery Error
Battery undervoltage according to Elec. Char. No. 404. Position is invalid. Change battery. Reboot iC-PVL. Battery monitoring is active during VDD supply.

BAT_WRN: Battery Early Warning
Battery voltage early warning according to Elec. Char. No. 405. Battery may be changed during main supply (VDD) as soon as possible. Alternatively, halt system, read current position and restore it. Switch off system, change battery and restart. Restored position may be set as counter preload. Battery monitoring is active during VDD supply.

PDR: Power Down Reset Detected
A power down reset was performed, caused by undervoltage considerably lower than the battery error threshold. Another reason may be due to insufficient stabilizing capacitors at the supply lines VDD and VBAT. If a power down reset is performed, all internal circuitry is initialized to its default state. Counter position is set to zero and the working state is reset to the POWON State. For power down reset, the voltage at VDDS is relevant. Therefore, it is only performed if both, VDD and VBAT are low. The voltage threshold is typically between 1.5 V and 2.5 V.

PRESET: Pin Preset Detected
This bit is set whenever the chip is coming from a power-down condition or a pin preset has been detected. It may be cleared by issuing a SCLR or RESET command. This can be interpreted as an acknowledgment that the power-down condition or pin preset was intentional. If the bit is set later during field operation, it is most likely unintentional. The cause may have been an external disruption, a short circuit error on the PRE line or a complete loss of power supply (VDD and VBAT). The PRESET bit is also set if the sleep mode has been enabled or an i^2C REBOOT has been performed.

Extended Status Byte
Table 28 shows the additionally available extended status register. The four MSBs indicate the current working state of iC-PVL (see Figure 7). Three additional status messages in the four LSBs can be evaluated.

STATUSEX	Addr. 0x12; bit 7:0	
Bit	Name	Description
0	AMPL_ERR	Amplitude error
1	MAG_ERR	Magnet error
2	NOMAG_L	NoMagnet working state (latched)
3	unused	unused
4	POWON_ST	iC-PVL in PowerOn working state
5	ACTIVE_ST	iC-PVL in Active working state
6	NOMAG_ST	iC-PVL in NoMagnet working state
7	SLEEP_ST	iC-PVL in Sleep working state

Table 28: Extended status byte

AMPL_ERR: Amplitude Error
The status bit is set, if the magnetic signal amplitude is below the threshold level configured via ATHR. Filtering is active, i.e. the bit is set only if the amplitude is low for approx. 128 ms.

MAG_ERR: Magnet Error
The status bit is set, if a magnet error is currently detected. The reason can be a low signal amplitude or a position consistency error (see POS_ERR). The condition is set by configuration parameter NOMAG.

NOMAG_L: NoMagnet Working State (latched)
By entering the NoMagnet state, the iC-PVL sets the status bit NOMAG_L. The bit is latched, i.e. it remains set even if the NoMagnet state is left again. Therefore it is possible to determine if the encoder magnetic field was lost once during the devices previous operating life. The status indication can be acknowledged with command SCLR to reset to state 0.

Error Output NERR
A LED may be connected to the error output NERR to signalize errors. The pin is an open drain output driver. If an error is detected, the pin is pulled low. STUP_ERR, CFG_ERR, CTR_ERR, POS_ERR, BAT_ERR, MAG_ERR, NOMAG_L are visible at NERR. Additionally, NERR is pulled low during the iC-PVL startup phase, if the device is in sleep state or a reset condition is currently active.

Error Output During Startup
During startup phase, a low level at NERR is visible, i.e. until complete and correct configuration read-in from the EEPROM. This indicates that iC-PVL is not ready to operate yet and does not answer a position

read request. A requesting node must wait until error indication is cleared after successful boot-up.

Warning Output NWRN
Battery early warning BAT_WRN is exclusively output at open drain pin NWRN.

Table 29 provides an overview of the iC-PVL status bit mapping to pin NERR and NWRN and the NERR and NWRN bits in the SSI serial data stream.

Status Bit	**Pin NERR**	**Pin NWRN**	**SSI NERR**	**SSI NWRN**
STUP_ERR	x		x	
CFG_ERR	x		x	
CTR_ERR	x		x	
POS_ERR	x		x	
BAT_ERR	x		x	
BAT_WRN		x		x
PDR				
PRESET				
AMPL_ERR				
MAG_ERR	x		x	
NOMAG_L	x		x	
POWON_ST	x		NA	NA
ACTIVE_ST				
NOMAG_ST	x		x	
SLEEP_ST	x		NA	NA
Note:	NA = SSI position readout not possible.			

Table 29: iC-PVL Status Bit Mapping Overview

Command Register
The commands given in Table 30 can be triggered by writing the respective command code to the iC-PVL command register. Please also refer to Table 6 and Table 7.

CMD	Addr. 0x11; bit 7:0	
Code	Name	Description
0x00	none	Reserved
0x01	none	Reserved
0x02	RESET	Soft reset
0x03	REBOOT	Reboot and preset from EEPROM
0x04	SLEEP ENABLE	Halt iC-PVL position sensing
0x05	SCLR	Clear all status bits
0x06	none	Reserved
0x07	SLEEP DISABLE	Restart iC-PVL position sensing
...	none	No operation

Table 30: Command register

The **RESET** command reinitializes the internal circuitry. Counter position and configuration remain untouched.

The **REBOOT** command reinitializes the internal circuitry and reloads the new configuration and counter preload value from the EEPROM. A preset pulse at pin PRE may be used as an alternative to the REBOOT command. Using the REBOOT command as a substitute for a preset pulse at pin PRE is not possible, as this will not properly set the operating mode of iC-PVL.

The **SLEEP ENABLE** command stops all position sensing action during battery mode and VDD mode. No position is tracked anymore. Power consumption is reduced to a minimum but interfaces are active during VDD supply. This is useful for the storage of encoders with installed battery.

The **SLEEP DISABLE** restarts the position sensing action during battery mode and VDD mode. The device switches back to active or battery working state.

The **SCLR** command (Status CLEAR) is used to clear all status messages in the status register.

SUPPLY SWITCH AND BATTERY MONITORING

To retain and acquire the absolute position even on main power shutdown, iC-PVL monitors VDD and switches to a battery supply on pin VBAT automatically. The switching point is just below 3 V. So, if the main supply voltage on VDD drops below 3 V, the internal circuitry will be powered by VBAT instead of VDD.

Note: iC-PVL continuously tracks the absolute position even on main power shutdown and during the transition from VDD to battery supply and vice-versa. Special care must be taken during the design of the power supply management of the encoder board. Very fast switching edges, chatter and over- / undershoot on the iC-PVL VDD supply line shall be avoided, resulting in a smooth and continuous charging and discharging ramp for power-on and off. Electrical Characteristics 001 and 008 must be adhered to at all times during the power transition phase.

The supply switch features a built-in hysteresis. The threshold voltages are defined in the Electrical Characteristics: V_{off} (Item No. 402), the voltage at which the circuit switches from VDD supply to VBAT supply, and V_{on} (Item No. 401) for the voltage at which the circuit switches back to VDD supply.

BAT_MON	Addr. 0x03; bit 6
Code	Function
0	Battery monitoring off
1*	Battery monitoring on
Note	*) Battery monitoring is only active during VDD supply.

Table 31: Enable battery monitoring

Depending on the power pack, e.g. a 3.6 V battery with 1 Ah capacity, the device can operate for several years. During VDD supply, the iC-PVL monitors the voltage at pin VBAT to detect a low battery voltage. If the supply drops below the error threshold V_{err} voltage (Item No. 404), an error is generated and signalized at pin NERR, by the error bit in the SSI communication protocol, and by the I^2C status register. The battery monitoring function can be enabled/disabled with the configuration parameter BAT_MON (Table 31).

Additionally an early battery warning message is generated independently of the setting of parameter BAT_MON. The warning threshold is specified in V_{wrn} (Elec. Char. No. 405) and depends on the setting of parameter BAT_THR. If the voltage at pin VBAT drops below this warning threshold, a warning is generated and signalized at pin NWRN and optionally by the warning bit of the SSI data (refer to Table 18).

The thresholds of V_{err} and V_{wrn} are defined by Elec. Char. 404 and Elec. Char. 405. They can be configured with configuration parameter BAT_THR according to Table 32.

BAT_THR	Addr. 0x05; bit 3:2	
Code	V_{err}	V_{wrn}
00*	3.05	3.15
01	2.95	3.05
10	2.85	2.95
11	2.75	2.85
Notes	Nominal values. Refer to Elec. Char. 404 and 405 for variation. *) BAT_THR = 0x00 is recommended. The usage of any other setting is discouraged.	

Table 32: Battery monitor threshold levels

CURRENT CONSUMPTION IN BATTERY MODE

Serial Interface Mode (SEL = LOW)

Note: In this chapter, all values for angular velocity and acceleration refer to one magnetic period, i.e. one north-south pole pair sequence per 360° mechanical. A velocity of one pole pair per second relates to 360°/s = 1 Hz = 60 ^{1}/min. When using a magnetic pole wheel the maximum angular acceleration or velocity that can occur in the application has to be multiplied with the number of magnetic pole pairs in order to choose the correct setting for A_MAX from Table 33.

Parameter A_MAX determines the lower limit of the hall sensor sampling rate of iC-PVL. Whenever movement of the magnetic target is detected, iC-PVL will automatically increase the sampling rate to match the magnetic input frequency if needed. Once the magnetic target is at standstill again, the sampling rate will revert to the frequency determined by parameter A_MAX.

Consequently, parameter A_MAX determines the iC-PVL current consumption in battery mode and the maximum permissible angular acceleration from standstill. The maximum application specific deceleration (braking) is not relevant for the selection of parameter A_MAX. The relationship between maximum permissible acceleration and current consumption is shown in Table 33. For accelerations below $48 \cdot 10^3 rad/s^2$, the typical current consumption is below 10 μA.

Note: The value for A_MAX needs to be chosen carefully, considering the precise motion profile during battery mode. Potential external factors like shock and vibration have to be taken into account, as the acceleration caused by such events may exceed the expected maximum system acceleration during normal operation. If A_MAX is chosen too low, counting errors can occur (missed counts) signalled by an active position error (POS_ERR).

For applications where only sporadic motor movement is expected during battery supply, Table 33 mainly defines the current consumed by iC-PVL. Additionally, Table 34 gives typical values in case of enduring movement at a certain angular velocity during battery supply.

Note: A magnetic field according to the specifications should be provided any time (see Elec. Char. No. 101). If a suitable magnetic target can not be provided during shipment or storage, use the sleep command (refer to Table 30), activate the magnetic field amplitude monitoring (refer to Table 25 and 26) or disconnect the battery.

A_MAX	Addr. 0x03; bit 5:3				
Code	α_{max} [$\frac{°}{s^2}$]	α_{max} [$\frac{rad}{s^2}$]	typ f_{min}[Hz]	typ I_{avg}[μA]	max I_{avg}[μA]
000	$160 \cdot 10^6$	$3000 \cdot 10^3$	2000	52	72
001	$40 \cdot 10^6$	$760 \cdot 10^3$	1000	26	36
010	$10 \cdot 10^6$	$190 \cdot 10^3$	500	14	18
011	$2.5 \cdot 10^6$	$48 \cdot 10^3$	250	7	10
100	$625 \cdot 10^3$	$12 \cdot 10^3$	125	4	6
101	$160 \cdot 10^3$	$3 \cdot 10^3$	63	2.5	4
110	$40 \cdot 10^3$	$0.75 \cdot 10^3$	32	2	3
111	$10 \cdot 10^3$	$0.2 \cdot 10^3$	16	1.5	2.5

Table 33: Maximum supported angular acceleration (from shaft halt), minimum sampling frequency and average current consumption on shaft halt or slow angular velocity. V(VBAT) = 3.6 V, V(PRE) < 0.5 V.

I(VBAT) for angular velocity [RPM]									
f[RPM] 2-pole magnet	f_{mag}[Hz] magnetic input freq.	I_{avg}[µA] A_MAX=111	I_{avg}[µA] A_MAX=110	I_{avg}[µA] A_MAX=101	I_{avg}[µA] A_MAX=100	I_{avg}[µA] A_MAX=011	I_{avg}[µA] A_MAX=010	I_{avg}[µA] A_MAX=001	I_{avg}[µA] A_MAX=000
0	0	1.5	2	2.5	4	7	14	26	52
<125	< 2	1.5	2	2.5	4	7	14	26	52
<250	< 4	2	2	2.5	4	7	14	26	52
<500	< 8	2.5	2.5	2.5	4	7	14	26	52
< 1000	< 16	4	4	4	4	7	14	26	52
< 2000	< 33	7	7	7	7	7	14	26	52
< 4000	< 66	14	14	14	14	14	14	26	52
< 8000	< 133	26	26	26	26	26	26	26	52
< 16000	< 266	52	52	52	52	52	52	52	52
< 32000	< 533	100	100	100	100	100	100	100	100
< 64000	< 1066	200	200	200	200	200	200	200	200
< 128000	< 2133	400	400	400	400	400	400	400	400
< 480000	< 8000	800	800	800	800	800	800	800	800

Table 34: Average current consumption vs. angular velocity. Typical values for V(VBAT) = 3.6 V, T_j = 27 °C and V(PRE) < 0.5 V.

Parallel Encoder Mode (SEL = HIGH)
The current consumption in parallel encoder mode is directly proportional to the sampling frequency, f_s. The typical average current consumption of iC-PVL is calculated as shown below (V(VBAT) = 3.6 V, T_j = 27 °C):

$$I_{avg}[\mu A] = 25 \cdot f_s[kHz]$$

For instance, at a sampling frequency of 1 000 samples per second: f_s = 1 kHz and I = 25 µA. At 100 samples per second: I = 2.5 µA.

OSCILLATOR FREQUENCY CALIBRATION

The bias current for the internal oscillator can be configured with parameter IBIAS. An increase or decrease in bias current will directly affect the oscillator frequency. The bias current should be calibrated at the typical battery supply voltage so that the frequency of the oscillator is around 34 kHz (see Elec. Char. No. 301). The clock frequency is observable at output pin DI_P1 in the dedicated calibration mode. The calibration mode is entered by configuring the EN_ERR parameter to "01" (see Table 17).

Note: Calibration mode is only entered if CFG_ERR is not active.

Calibrating the oscillator frequency is not absolutely necessary to ensure iC-PVL operation. Nevertheless, if left uncalibrated, among others, mainly the values defined in Table 33 and 34 may be out of range.

IBIAS Addr. 0x03; bit 2:0	
Code	Frequency change (typ.)
100	+10 %
101	+ 6 %
110	+ 3 %
111	0 %
000	0 %
001	- 3 %
010	- 6 %
011	-10 %

Table 35: Bias current: Oscillator frequency calibration.

APPLICATION EXAMPLE: iC-PVL as battery powered revolution counter or metering device

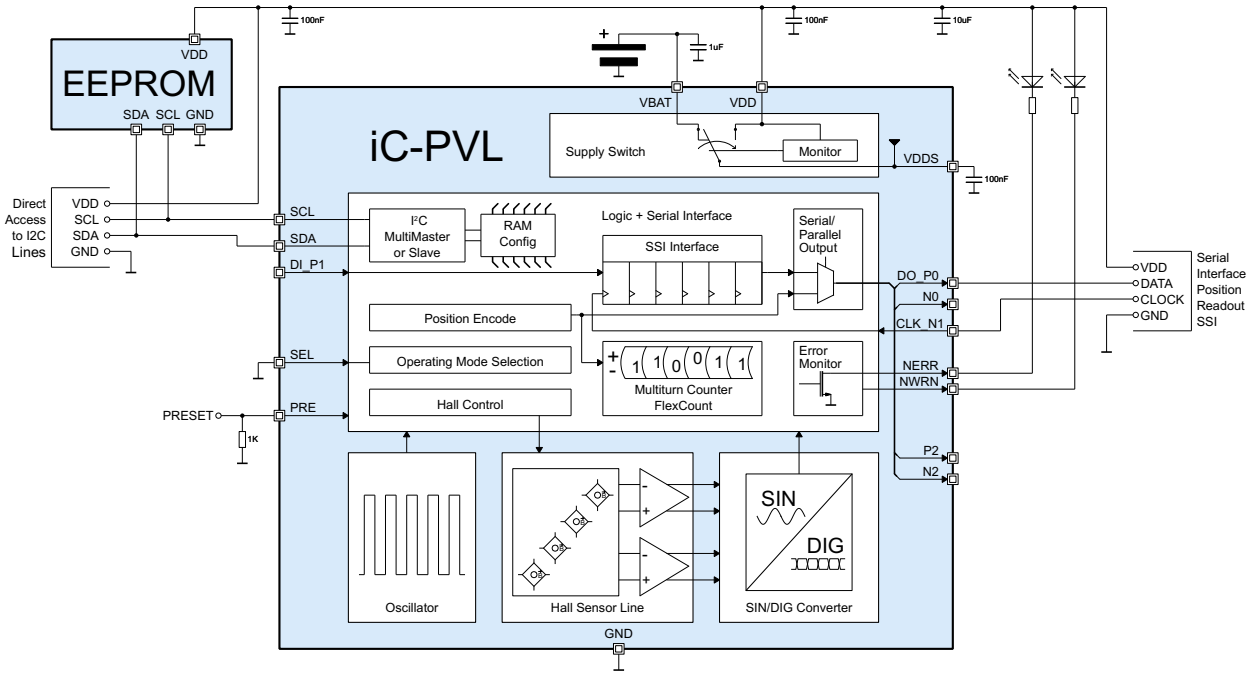


Figure 16: Principle application example. iC-PVL as battery powered multiturn counter, e.g. in a metering application. Interface operating in INT_MODE = 0, readout of the internal counter value via SSI or I²C. VDD supply is only needed during readout, otherwise iC-PVL is battery-powered. Direct access to iC-PVL EEPROM via SCL, SDA.

Note: All circuit examples shown in this chapter are principle wiring diagrams. Further components may be necessary but are omitted for clarification of the application principle.

DESIGN REVIEW: Notes On Chip Functions

iC-PVL X1		
No.	Function, parameter/code	Description and application notes
		See previous datasheet release F3.

Table 36: Notes on chip functions regarding iC-PVL chip revision X1

iC-PVL W1		
No.	Function, parameter/code	Description and application notes
		See previous datasheet release F3.

Table 37: Notes on chip functions regarding iC-PVL chip revision W1

iC-PVL W2		
No.	Function, parameter/code	Description and application notes
		See previous datasheet release F3.

Table 38: Notes on chip functions regarding iC-PVL chip revision W2

iC-PVL W4		
No.	Function, Parameter/Code	Description and Application Hints
1	Preset Pulse	Implemented auto preset feature at initial start-up. An externally applied preset pulse at pin PRE is not necessary anymore on initial start-up in SSI mode (SEL = low).
2	Position readout via SSI during initialization phase	While the iC-PVL is reading its configuration data from the EEPROM after initial startup or reinitialization, the data read out via SSI is invalid. The data is only valid after iC-PVL has set its NERR pin to high level.

Table 39: Notes on chip functions regarding iC-PVL chip release W4

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2016-06-09	All	Initial release	All

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2016-08-09		Please refer to former datasheet release	

Rel.	Rel. Date*	Chapter	Modification	Page
B2	2017-05-12		Please refer to former datasheet release	

Rel.	Rel. Date*	Chapter	Modification	Page
B3	2017-08-02		Please refer to former datasheet release	

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2017-09-14		Please refer to former datasheet release	

Rel.	Rel. Date*	Chapter	Modification	Page
C2	2017-10-19		Please refer to former datasheet release	

Rel.	Rel. Date*	Chapter	Modification	Page
C3	2018-01-23		Please refer to former datasheet release	

Rel.	Rel. Date*	Chapter	Modification	Page
D1	2018-10-31		Please refer to former datasheet release	

Rel.	Rel. Date*	Chapter	Modification	Page
D2	2018-11-08		Please refer to former datasheet release	

Rel.	Rel. Date*	Chapter	Modification	Page
E1	2019-07-16	PACKAGING INFORMATION	Added note for pin VBAT : If not used connect to VDD	4
		ELECTRICAL CHARACTERISTICS	Separated Item No. 005 by temperature	7
		OPERATING MODE SELECTION	Added footnote regarding chip revision W4	16
		STARTUP BEHAVIOR	Added footnote regarding chip revision W4	18
		SERIAL INTERFACE MODE (SEL = LOW)	Corrected bit range in Table 13 and 19 Added note to Table 15	23
		I^2C SLAVE MODE	Reworked chapter	28
		ERROR MONITOR, STATUS AND COMMAND REGISTER	Reworked chapter	29
		CURRENT CONSUMPTION IN BATTERY MODE	Reworked chapter - Added notes	33
		APPLICATION EXAMPLES: Singleturn iCs with multiturn interface (SSI Mode)	Removed chapter. Application examples now in iC-PVL AN2	

Rel.	Rel. Date*	Chapter	Modification	Page
F1	2021-02-22	DESCRIPTION	Added system responsibility disclaimer	2
		ABSOLUTE MAXIMUM RATINGS	Changed items No. G001 - G004	6
		ELECTRICAL CHARACTERISTICS	El. Char. item No. 001 - Added comment	7
		ELECTRICAL CHARACTERISTICS	Added item No. A05, Length of Preset Pulse on PRE pin	8
		OPERATING CONDITIONS: Serial and Parallel Interface	Updated item no. I002 - I006	10
		ELECTRICAL CHARACTERISTICS	Changed item No. I012 from 1µs to 2µs	10
		OPERATING CONDITIONS: Serial and Parallel Interface	Updated Figure 2 and added comment on Chain Mode	11
		OPERATING MODE SELECTION	Clarification on I2C Device ID in I2C Slave Mode	15

		OPERATING MODE SELECTION	Figure 6 and Table 4: Added comment on Chain Mode	15, 16
		COMPENSATION OF ASSEMBLY: Data Offset and Counting Direction	Updated caption of Figure 13	22
		SERIAL INTERFACE MODE (SEL = LOW)	Table 12: Added comment on Chain Mode. Removed Table 19 and associated note	23
		MULTITURN COUNTER	Corrected address range in Table 22	25
		I^2C MULTIMASTER INTERFACE AND CRC PROTECTION	Added CRC calculation code example	27
		SUPPLY SWITCH AND BATTERY MONITORING	Added note on VDD requirements during power-up and power-down phase	32
		OSCILLATOR FREQUENCY CALIBRATION	Added note: Calibration mode only entered if CFG_ERR is not active	34
		DESIGN REVIEW: Notes On Chip Functions	Removed design review for chip revision X. Please refer to former datasheet release E1	36

Rel.	Rel. Date*	Chapter	Modification	Page
F2	2021-02-25	REVISION HISTORY	Corrected Revision History entry under "PACKAGING INFORMATION" for Release E1: pin PRE -⟶ pin VBAT	37

Rel.	Rel. Date*	Chapter	Modification	Page
F3	2023-09-14	REGISTER MAP (I^2C slave ID = 0b1100 001), REGISTER MAP (I^2C slave ID = 0b1100 000)	Added annotations, updated register map headlines	13, 14
		MULTITURN COUNTER	Added note on how to safely write a MT preset value via I^2C to iC-PVL RAM	25
		MAGNETIC FIELD AMPLITUDE MONITORING	Added note on usage of magnetic field amplitude monitoring feature	28
		ERROR MONITOR, STATUS AND COMMAND REGISTER	Added Table 29 : iC-PVL Status Bit Mapping Overview	31
		DESIGN REVIEW: Notes On Chip Functions	Added item No. 2 for chip revision W4: Position readout via SSI during the startup phase	36

Rel.	Rel. Date*	Chapter	Modification	Page
G1	2024-03-15	ELECTRICAL CHARACTERISTICS	Added Elec. Char. Item No. 013; Removed chip revision X1 footnote for clarity	7
		I^2C SLAVE MODE	Removed old chip revisions from Table 24	28
		APPLICATION EXAMPLE: iC-PVL as battery powered revolution counter or metering device	Updated Figure 16, added C(PWR)	35

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-PVL	QFN16-4x4		iC-PVL QFN16-4x4
Evaluation kit	61 mm x 64 mm PCB		iC-PVL EVAL PVL1M
iC-PVL GUI		Evaluation software for Windows PC	For download link refer to www.ichaus.com/pvl_gui

Please send your purchase orders to our order handling team:

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