iC-PMX

ENERGY HARVESTING MULTITURN COUNTER/ENCODER

FEATURES

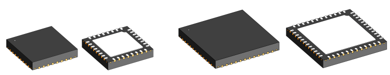
- Gearless and batteryless revolution counter
- Energy harvesting through Wiegand pulses[1]
- Integrated Hall switch for direction detection
- Evaluation of Pt1000 sensor output for high accuracy gas meter applications
- SPI interface to external nonvolatile RAM
- Independent SPI interface to microcontroller (configuration and data exchange)
- 4 low-noise Hall sensors with differential analog output
- Electrical Wiegand wire excitation for synchronization with singleturn data
- Runt pulse tolerant counting algorithm
- All accessory components are off-the-shelf products

[1] Devices and processes for energy harvesting by Wiegand wire within position encoders are protected by several worldwide patents, see notes on page 2.

APPLICATIONS

- Multiturn encoders
- Absolute end-of-shaft encoders
- Absolute hollow shaft encoders
- Absolute linear encoders
- Period counters
- Gas meters
- Liquid flow meters
- Encapsulated flow meters

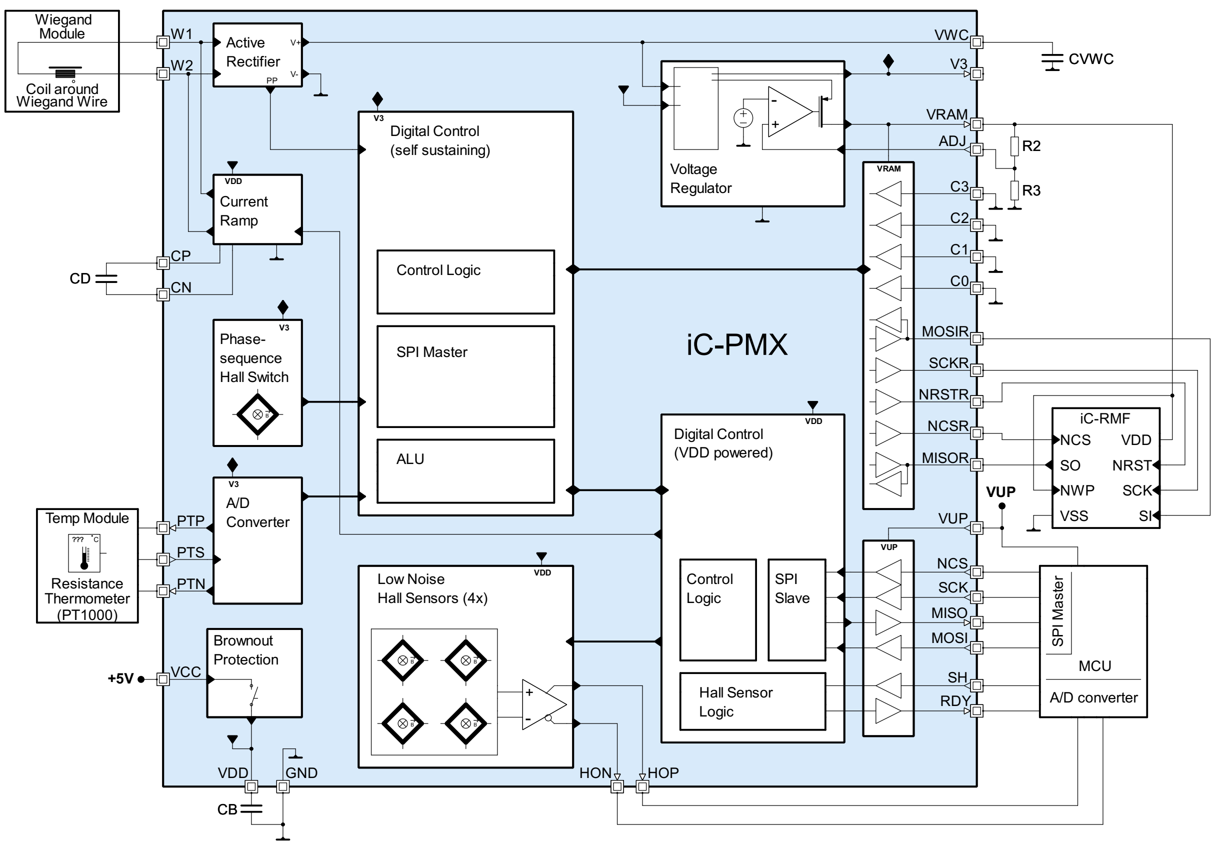
PACKAGES



QFN32
5 mm x 5 mm
RoHS compliant

QFN48
7 mm x 7 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-PMX uses a Wiegand wire to generate the electrical energy for acquiring, processing and storing the absolute position of any number of periods of the magnetic field. This energy harvesting capacity is supplemented with a singleturn sensor module for high resolutions and a special placement and electrical processing of the enclosed Hall sensors.

Additionally a temperature module can be connected to allow the precise calculation of gas volume in flow meters.

iC-PMX has an operating temperature range of up to 125 °C and is suitable for measuring at high speed.

Typical applications are highly integrated energy autonomous magnetic absolute encoders and metering applications. The absolute encoders can replace established gear or battery buffered solutions.

Note: Devices and processes for energy harvesting by Wiegand wire within position encoders are protected by several worldwide patents of the inventors Dr. Walter Mehnert and Dr. Thomas Theil (called MT patents) and require a license issued by the corresponding patent holders. iC-Haus is allowed to deliver iC-PMX to the licensees of MT patents.

A list of related MT patents, now held by Avago Technologies International Sales Pte. Limited can be provided on request without guarantee on actuality, accuracy and completeness. In general, users of our Integrated Circuits are responsible to consider third parties application relevant IPs.

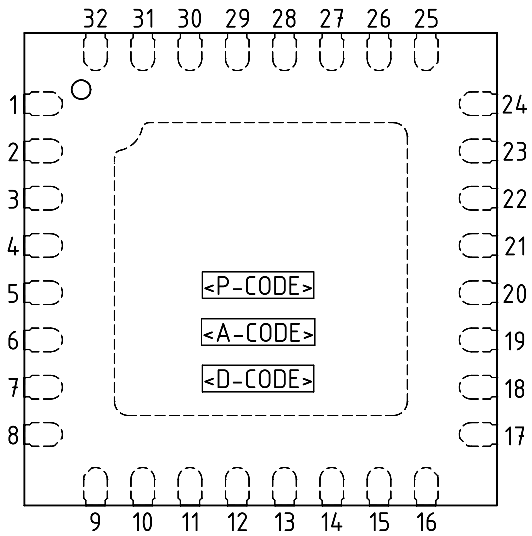
iC-PMX can also be used outside the scope of MT patents. However, a delivery to non-licensees is subject to a written statement that our ICs won't be used within the scope of the MT patents. A small quantity of ICs can be supplied subject to a written declaration that our ICs will solely be used for testing purposes in research and development.

Note: Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION QFN32 5 mm x 5 mm

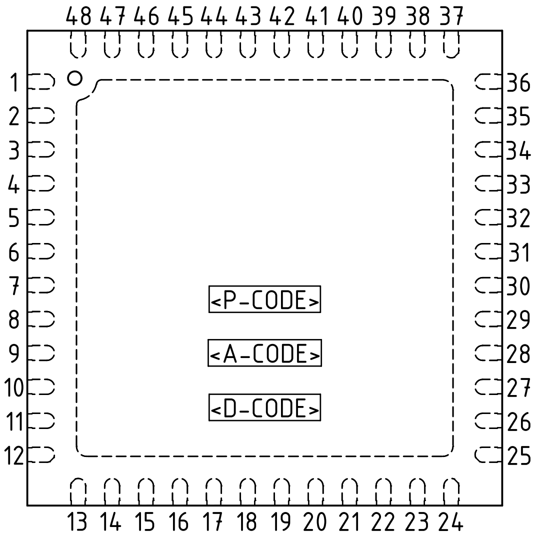


PIN FUNCTIONS

No.	Name	Function
1	W1	Wiegand Module Pin 1
2	W2	Wiegand Module Pin 2
3	VDD	Supply Voltage for Singleturn Hall
4	VCC	Supply Voltage (5V)
5	CP	Cap CD Pin P
6	CN	Cap CD Pin N
7	GND	Ground
8	C0	Configuration
9	C1	Configuration
10	C2	Configuration
11	C3	Configuration
12	MISOR	FRAM Interface, Master Data Input
13	NCSR	FRAM Interface, Chip Select
14	NRSTR	FRAM Interface, Reset
15	SCKR	FRAM Interface, Clock
16	MOSIR	FRAM Interface, Master Data Output
17	ADJ	Feedback Voltage for VRAM
18	VRAM	Voltage for FRAM (internally provided)
19	V3	Core Voltage (internally provided)
20	PTP	Thermometer Positive Supply
21	PTS	Thermometer Sense Pin
22	PTN	Thermometer Negative Supply
23	HOP	Hall Output positive (Singleturn Hall)
24	HON	Hall Output negative (Singleturn Hall)
25	SH	Switch Hall MCU (Singleturn Hall)
26	NCS	Serial Interface MCU, Chip Select
27	SCK	Serial Interface MCU, Clock
28	MOSI	Serial Interface MCU, Slave Data Input
29	MISO	Serial Interface MCU, Slave Data Output
30	RDY	Data Ready MCU
31	VUP	Supply Voltage for MCU I/O
32	VWC	Cap CVWC

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes).
The backside pad has to be connected to GND on the PCB.

PIN CONFIGURATION QFN48 7 mm x 7 mm



PIN FUNCTIONS

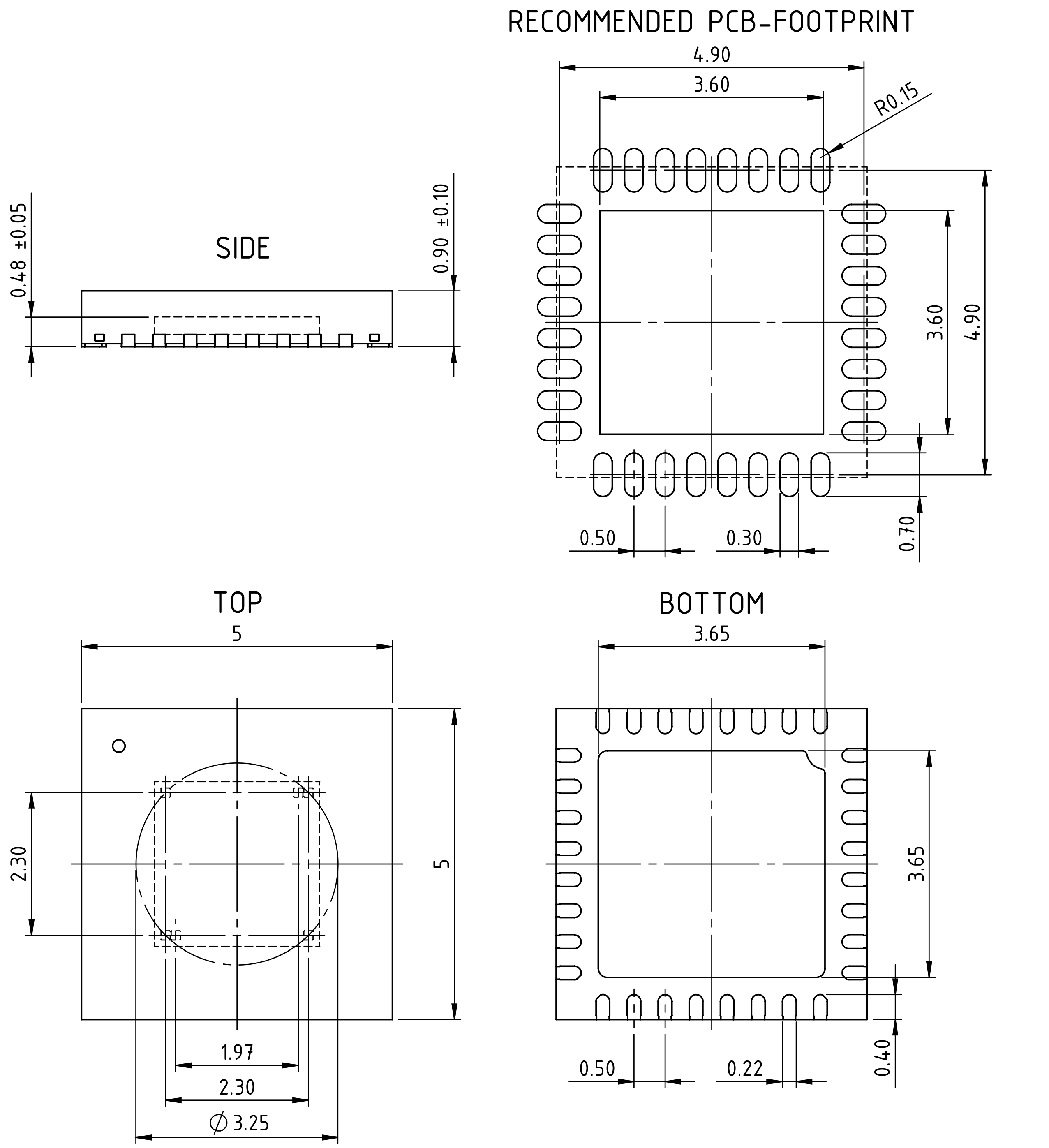
No.	Name	Function
1	n/c [1]	
2	VWC	Cap CVWC
3	W1	Wiegand Module Pin 1
4	W2	Wiegand Module Pin 2
5	VDD	Supply Voltage for Singleturn Hall
6	VCC	Supply Voltage (5V)
7	CP	Cap CD Pin P
8	CN	Cap CD Pin N
9	GND	Ground
10	C0	Configuration
11	n/c [1]	
12	n/c [1]	

PIN FUNCTIONS

No.	Name	Function
13	n/c [1]	
14	n/c [1]	
15	C1	Configuration
16	C2	Configuration
17	C3	Configuration
18	MISOR	FRAM Interface, Master Data Input
19	NCSR	FRAM Interface, Chip Select
20	NRSTR	FRAM Interface, Reset
21	SCKR	FRAM Interface, Clock
22	MOSIR	FRAM Interface, Master Data Output
23	n/c [1]	
24	n/c [1]	
25	n/c [1]	
26	ADJ	Feedback Voltage for VRAM
27	VRAM	Voltage for FRAM (internally provided)
28	V3	Core Voltage (internally provided)
29	PTP	Thermometer Positive Supply
30	PTS	Thermometer Sense Pin
31	PTN	Thermometer Negative Supply
32	HOP	Hall Output positive (Singleturn Hall)
33	HON	Hall Output negative (Singleturn Hall)
34	VUP	Supply Voltage for µP I/O
35	INT	Bias Current
36	n/c [1]	
37	n/c [1]	
38	n/c [1]	
39	n/c [1]	
40	SH	Switch Hall MCU (Singleturn Hall)
41	NCS	Serial Interface MCU, Chip Select
42	SCK	Serial Interface MCU, Clock
43	MOSI	Serial Interface MCU, Slave Data Input
44	MISO	Serial Interface MCU, Slave Data Output
45	RDY	Data Ready MCU
46	VUP	Supply Voltage for MCU I/O
47	n/c [1]	
48	n/c [1]	

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes).
The backside pad has to be connected to GND on the PCB.
[1] Pin numbers marked n.c. are not connected.

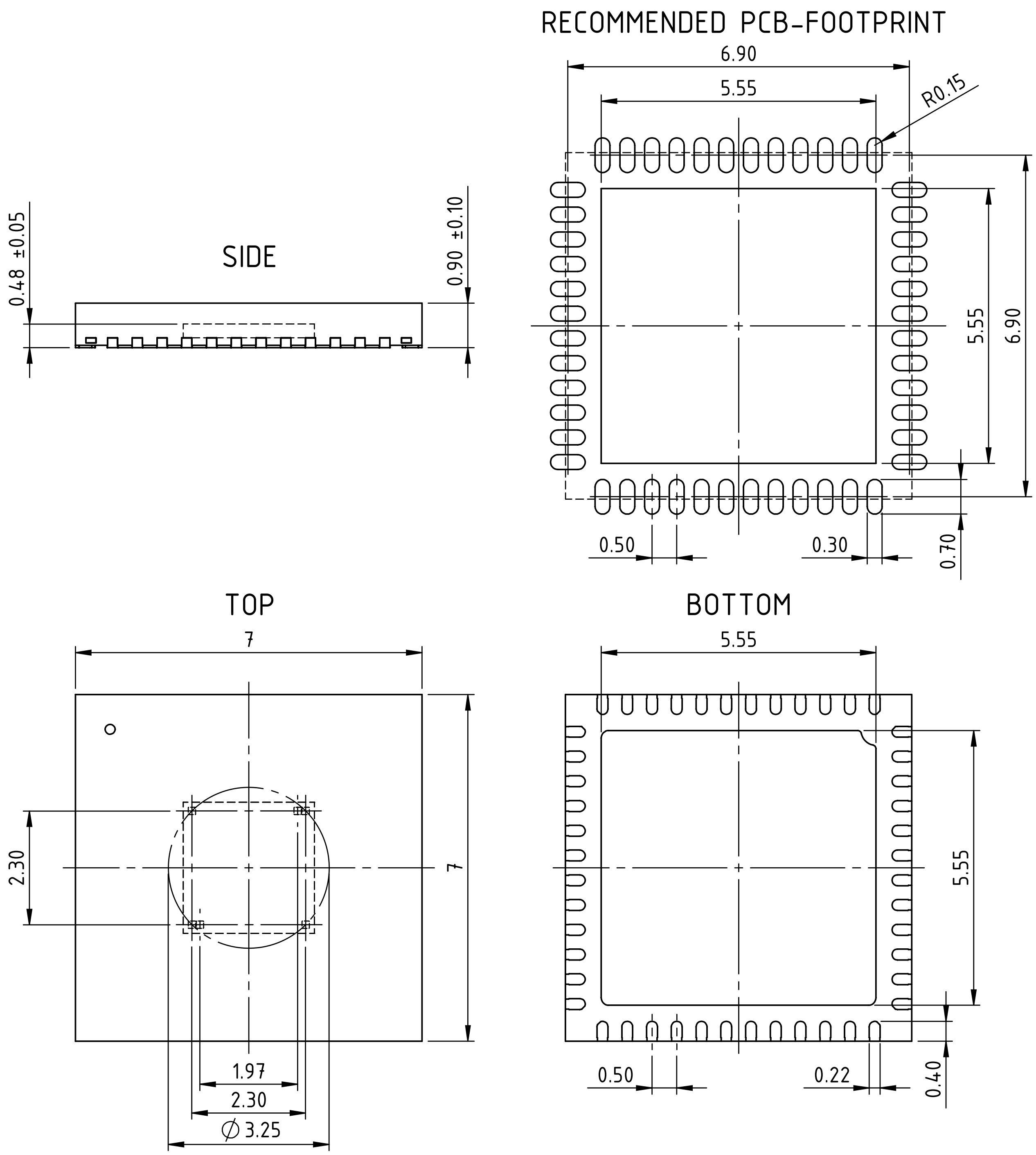
PACKAGE DIMENSIONS QFN32 5 mm x 5 mm



All dimensions given in mm. Size of hall sensors: 140µm x 140µm.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad).
Tolerance of package center: ±0.05mm (with respect to center of backside pad).
Tolerances of form and position according to JEDEC MO-220.

dra_qfn32-5x5-6_pm_pack_1, 10:1

PACKAGE DIMENSIONS QFN48 7 mm x 7 mm



All dimensions given in mm. Size of hall sensors: 140µm x 140µm.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad).
Tolerance of package center: ±0.05mm (with respect to center of backside pad).
Tolerances of form and position according to JEDEC MO-220.

drb_qfn48-2_pm_pack_1, 8:1

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Voltage at VCC		-0.3	6	V
G002	VDD	Voltage at VDD		-0.3	6	V
G003	I(VCC)	Current in VCC		-10	40	mA
G004	I(VDD)	Current in VDD		-10	40	mA
G005	Vd()	ESD Susceptibility	HBM 100 pF discharged through 1.5 kΩ Wiegand sensor pins W1, W2		2 1	kV kV
G006	Tj	Operating Junction Temperature		-40	125	°C
G007	Ts	Storage Temperature Range		-40	150	°C
G008	H()	Magnetic Field Strength		-1000	1000	kA/m
G009	V()	Voltage at VWC, W1, W2, CP		-0.3	12	V
G010	V()	Voltage at CN, C0-C3, ADJ, V3, VRAM, PTP, PTS, NRSTR, NCSR, SCKR, MOSIR, MISOR, INT, HOP, HON, SH, NCS, SCK, MOSI, MISO, RDY, VUP		-0.3	6	V
G011	I()	Current in W1, W2, CP, CN		-40	40	mA
G012	I()	Current in PTP, PTS, PTN, INT, HOP, HON, VWC, V3, VRAM, ADJ, C0-C3, NRSTR, NCSR, SCKR, MOSIR, MISOR, VUP, NCS, SCK, MISO, MOSI, SH, RDY		-10	10	mA

THERMAL DATA

Operating Conditions: VCC = 4.5...5.5 V, VUP = 3.0...VCC

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Rthja	Thermal Resistance Chip/Ambient	thermal pad connected to GND plane thermal pad connected to GND pin		60 100		K/W K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 4.5...5.5 V, VUP = 3.0...VCC, Tj = -40 °C...125 °C, INT calibrated to 100 µA, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
101	V(VCC)	Permissible Supply Voltage		4.5	5.0	5.5	V
102	I(VCC)	Supply Current	singleturn Hall sensors enabled, current ramp off		4	6	mA
103	I_0(VCC)	Standby Current I(VCC)	singleturn Hall sensors disabled, current ramp off		1	2	mA
104	V(VUP)	Permissible Supply Voltage		3.0		5.5	V
105	I(VUP)	Supply Current	SCK, MOSI, SH = 0V, NCS = V(VUP)		30	100	µA
107	Vc()hi	Clamp-Voltage hi at Inputs NCS, SCK, MOSI, SH	Vc()hi = V() - V(VUP), I() = 1 mA	0.3		1.2	V
108	Vc()hi	Clamp-Voltage hi at Inputs PTP, PTS, C0-C3, NRSTR, NCSR, SCKR, MOSIR, MISOR	Vc()hi = V() - V(VRAM), I() = 1 mA	0.3		1.2	V
109	Vc()lo	Clamp-Voltage lo at all Pins	I() = -4 mA	-1.2		-0.3	V
110	I(V3)	Permissible Load Current V3				-1	mA
111	I(VRAM)	Permissible Load Current VRAM				-1	mA
113		Max. Voltage on W1, W2, VWC, CP	CVWC = 6.8nF			11	V
114	Qwc()	Charge Consumption for Wiegand Pulse Processing	VDD < VDDOK C1 = 0, C0 = 0 (period counter mode)		6.5	8	nC
115	V(VRAM)	Permissible FRAM Supply Voltage	programmed by the voltage divider at pin ADJ	1.5		3.3	V
Active Rectifier							
201	V(VWC)	Voltage	V(W1,W2) = +- 3 V, I(VWC) = 5 mA V(W1,W2) = +- 5.5 V, I(VWC) = 5 mA	2.8 5.3			V V
202		Required Slew Rate for Activating the Active Rectifier		84			mV/µs
204		Allowed Slew Rate During Switched Current Ramp				19	mV/µs
209		Required Delay between Alternating Wiegand Pulses		1			ms

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 4.5...5.5 V, VUP = 3.0...VCC, Tj = -40 °C...125 °C, INT calibrated to 100 µA, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Current Ramp W1, W2							
301	Imax(Wx)		WI(1:0) = 00 WI(1:0) = 01 WI(1:0) = 10 WI(1:0) = 11	-9.6 -14 -18 -22	-8.1 -12 -15.5 -19	-6.6 -10 -13 -16	mA mA mA mA
302	sl	Slewrate of Current Ramp	WI(1:0)=00, RAMP(3:2)=00 WI(1:0)=01, RAMP(3:2)=00 WI(1:0)=10, RAMP(3:2)=00 WI(1:0)=11, RAMP(3:2)=00 WI(1:0)=00, RAMP(3:2)=01 WI(1:0)=01, RAMP(3:2)=01 WI(1:0)=10, RAMP(3:2)=01 WI(1:0)=11, RAMP(3:2)=01 WI(1:0)=00, RAMP(3:2)=10 WI(1:0)=01, RAMP(3:2)=10 WI(1:0)=10, RAMP(3:2)=10 WI(1:0)=11, RAMP(3:2)=10 WI(1:0)=00, RAMP(3:2)=11 WI(1:0)=01, RAMP(3:2)=11 WI(1:0)=10, RAMP(3:2)=11 WI(1:0)=11, RAMP(3:2)=11			13 19 24 29 20 29 37 45 25 37 48 59 39 57 74 90	µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs µA/µs
303	tr(), tf()	Rise and Fall Time Current Ramp	10% to 90% RAMP(3:2) = 00 RAMP(3:2) = 01 RAMP(3:2) = 10 RAMP(3:2) = 11	 560 360 290 180	 750 480 370 240	 940 600 450 300	 µs µs µs µs
304	t()	Duration of Current Ramp	from end of SPI current ramp command, to current ramp disconnection from W1, W2 RAMP(3:2) = 00 RAMP(3:2) = 01 RAMP(3:2) = 10 RAMP(3:2) = 11	 1600 1100 800 500	 2150 1500 1100 750	 2700 1900 1400 1000	 µs µs µs µs
Phase Sequence Hall Switch (The sensor positions are specified in chapter PACKAGE DIMENSIONS)							
401	Ht()pos	Differential Magnetic Field Strength Threshold pos	at the surface of the sensors C2 = 1 (absolute field strength at sensor H4) C2 = 0 (differential field strength between H4 and H5)	 2 5		 20 40	 kA/m kA/m
402	Ht()	Magnetic Field Strength Threshold [1]	at the surface of the sensors; C2 = 1 (absolute field strength at sensor H4) C2 = 0 (differential field strength between H4 and H5)	 -10 -10		 10 10	 kA/m kA/m
403	Ht()neg	Differential Magnetic Field Strength Threshold neg	at the surface of the sensors C2 = 1 (absolute field strength at sensor H4) C2 = 0 (differential field strength between H4 and H5)	 -20 -40		 -2 -5	 kA/m kA/m
404	H()	Tolerated Magnetic DC Field Strength	common magnetic field strength at the surface of both sensors	-200		200	kA/m
A/D Converter for Temperature Sensor							
501	TR	Measurement Range		-25		55	°C

[1] For iC-PMX 4: Please read the design review on page 30.

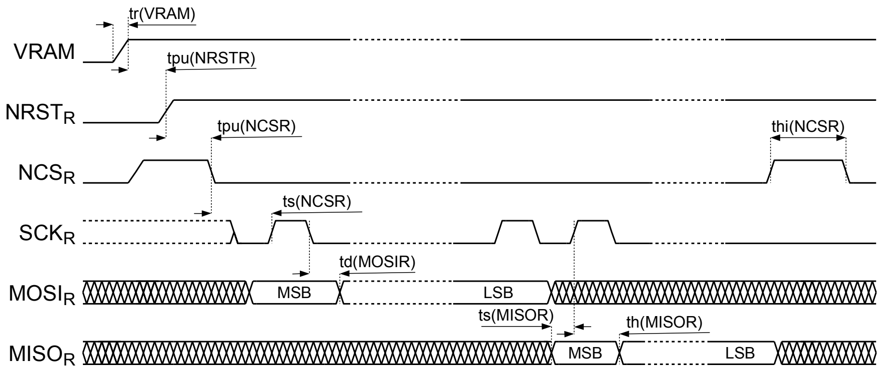
ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 4.5...5.5 V, VUP = 3.0...VCC, Tj = -40 °C...125 °C, INT calibrated to 100 µA, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Bias, Power-on Wiegand (Self-Sustained Mode)							
601	V(V3)	Core Voltage	V(VWC) > 3.5V; I(VRAM) < 1 mA V(VDD) > 4.5V; I(VRAM) < 1 mA	2.7 2.7	3.3 3.3	3.6 3.6	V V
603	VWCOK	Required Voltage on VWC at Start of FRAM Access	measured during Wiegand pulse, during first falling edge of NCSR	2.7		3.0	V
606	VRAMoff	Turn-off Threshold VRAM	decreasing voltage at V3			1.5	V
608	V(ADJ)	Feedback Voltage of VRAM Source	feedback loop closed, V(VRAM) stable	1.17	1.23	1.29	V
Bias, Power-on (VCC powered)							
701	NPORon	Power-on-Reset Threshold VDD (digital logic)	increasing voltage at VDD	1.9		3.1	V
702	NPORoff	Power-off-Reset Threshold VDD (digital logic)	decreasing voltage at VDD	1.7		2.8	V
703	NPORHys	Hysteresis		0.15	0.3		V
705	VDDOK	Brownout Detection Threshold Voltage		3.9		4.4	V
711	I(INT)	Bias Current	I(INT) vs. VDD BIAS = 0x0 BIAS = 0xF I(INT) calibrated at T = 25 °C	 100 90	 77 140 100	 100 110	 µA µA µA
Low Noise Hall Sensors and Analog Outputs HOP, HON (The sensor positions are specified in chapter PACKAGE DIMENSIONS)							
801	V(HOP) – V(HON)	Magnetic Field Sensitivity	Gain = 0x0, H = 10kA/m, T = -40°C Gain = 0x0, H = 10kA/m, T = 27°C Gain = 0x0, H = 10kA/m, T = 125°C Gain = 0x1, H = 10kA/m, T = 27°C Gain = 0x2, H = 10kA/m, T = 27°C Gain = 0x3, H = 10kA/m, T = 27°C Gain = 0x4, H = 10kA/m, T = 27°C Gain = 0x5, H = 10kA/m, T = 27°C Gain = 0x6, H = 10kA/m, T = 27°C Gain = 0x7, H = 10kA/m, T = 27°C		54 37 22 56 81 125 187 275 387 544		mV mV mV mV mV mV mV mV mV mV
806	fg()ana	Cut-off Frequency	C = 25 pF to GND	900			kHz
807	SR	Slew Rate	C = 25 pF to GND, Gain = 0x7	2.5			V/µs
808	I()buf	Permissible Output Current		-1		1	mA
809	Vs()hi	Saturation Voltage hi	Vs() = V(VDD)-V(), I() = -0.8mA			0.5	V
810	Vs()lo	Saturation Voltage lo	I() = 0.8mA			0.5	V

ELECTRICAL CHARACTERISTICS

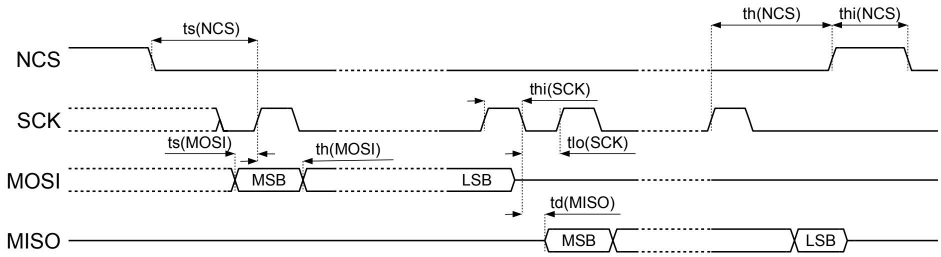
Operating Conditions: VCC = 4.5...5.5 V, VUP = 3.0...VCC, Tj = -40 °C...125 °C, INT calibrated to 100 µA, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Inputs C0, C1, C2, C3, MOSIR, MISOR							
901	Vt()lo	Threshold Voltage lo		20			%VRAM
902	Vt()hi	Threshold Voltage hi				80	%VRAM
Outputs MISOR, NCSR, NRSTR, SCKR, MOSIR							
A01	Vs()hi	Saturation Voltage hi	Vs() = VRAM - V();I()= -1mA			350	mV
A02	Vs()lo	Saturation Voltage lo	I()= 1mA			350	mV
A03	tr()	Rise Time	V(V3) > 2.7V; C = 5 pF to GND V(V3) > 2.7V; C = 10 pF to GND			10 20	ns ns
A04	tf()	Fall Time	V(V3) > 2.7V; C = 5 pF to VRAM V(V3) > 2.7V; C = 10 pF to VRAM			10 20	ns ns
Timing Parameter SPI-FRAM							
							
C02	tpu(NRSTR)	$NRST_R$: Hold Time at Power-on		1			µs
C03	tpu(NCSR)	NCS_R: Hold Time after Rising Edge of $NRST_R$	C0 = 0	1			µs
C04	thi(NCSR)	NCS_R High Time		40			ns
C05	f()	SCK_R: Clock Frequency	sending opcode SPI data transmission DSPI data transmission dummy clocks (POS0-POS3 processing)			15 15 7.5 5	MHz MHz MHz MHz
C06	ts()	$MISO_R$, NCS_R: Setup Time to Rising Edge of SCK_R		10			ns
C07	th(MISOR)	$MISO_R$: Hold Time after Rising Edge of SCK_R		0			ns
C08	td(MOSIR)	$MOSI_R$: Data Valid after Falling Edge of SCK_R		-20		20	ns
C09	td(VWC, NRSTR)	Delay between End of Rising Edge(VWC) and Falling Edge(NRSTR)	VCC = 0V C1 = 0, C0 = 0 (period counter mode)			20	µs

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 4.5...5.5 V, VUP = 3.0...VCC, Tj = -40 °C...125 °C, INT calibrated to 100 µA, unless otherwise noted

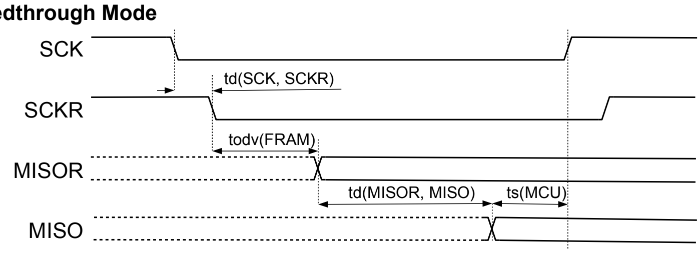
Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Inputs NCS, SCK, MOSI, SH							
D01	Vt()lo	Threshold Voltage lo		20			%VUP
D02	Vt()hi	Threshold Voltage hi				80	%VUP
D03	Vt()hys	Threshold Voltage Hysteresis		200			mV
D04	Ipd()	Pull-Down Current	V() = 1.5V...VUP	4	35	70	µA
D05	Ipu()	Pull-Up Current for NCS	V() = 0V...VUP-1.5V	-70	-35	-5	µA
Outputs MISO, RDY							
E01	Vs()hi	Saturation Voltage hi	Vs() = VUP - V();I() = -2.8 mA			400	mV
E02	Vs()lo	Saturation Voltage lo	I() = 2.8 mA			400	mV
E03	tr()	Rise Time	C = 50 pF to GND (20% to 80% V(VUP)			30	ns
E04	tf()	Fall Time	C = 50 pF to VUP (80% to 20% V(VUP)			30	ns
E05	Ipd()	Pull-Down Current MISO	MISO inactive, V() = 1.5V...VUP	4	35	70	µA
Timing Parameter SPI Slave Interface							



Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F01	tpu()	Hold Time at Power-on			10		µs
F02	f()	SCK: Clock Frequency				20	MHz
F03	ts()	MOSI,NCS: Setup Time to Rising Edge of SCK		25			ns
F04	th(MOSI)	MOSI: Hold Time after Rising Edge of SCK		3			ns
F05	td(MISO)	MISO: Data Valid after Falling Edge of SCK	C = 50 pF to GND	0		75	ns
F06	tlo(SCK)	SCK Low Time		25			ns
F07	thi(SCK)	SCK High Time		25			ns
F08	th(NCS)	NCS: Hold Time after Rising Edge of SCK		25			ns
F09	thi(NCS)	NCS High Time		200			ns
F10	tlo(SH)	SH Low Time		100			ns
F11	thi(SH)	SH High Time		100			ns
F12	th(SH)	SH: Hold Time after Rising Edge of NCS		100			ns
F13	th(NCS,SH)	NCS: Hold Time after Change of SH		100			ns

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 4.5...5.5 V, VUP = 3.0...VCC, Tj = -40 °C...125 °C, INT calibrated to 100 µA, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Timing Parameter FRAM Feedthrough Mode							
							
I01	td(SCK, SCKR)	Transport Delay from SCK to SCKR	C = 10 pF to GND			25	ns
I02	td(MISOR, MISO)	MISO: Data Valid after a Change at MISOR	C = 10 pF to GND			240	ns
I03	td(VWC, SH)	Required Falling Edge of SH after Occurrence of a Wiegand Pulse	feedthrough mode active C1 = 0, C0 = 0 (period counter mode)			100	us

OPERATION AT POWER-UP

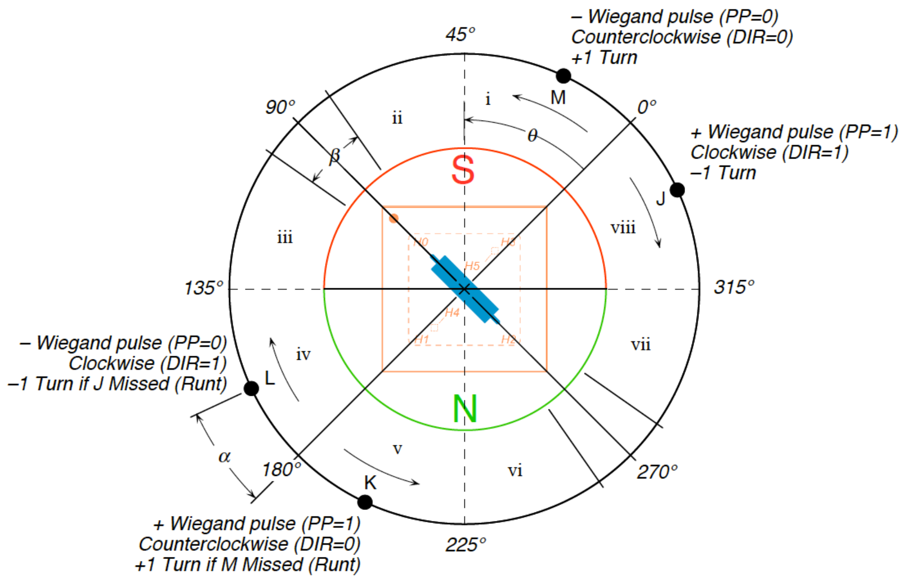


Figure 1: Power-up Octants

At power-up, the accompanying MCU (e.g. iC-TW14) reads the accumulated multiturn position (including the last PP and DIR values) from the iC-PMX (see Tab. 15 in chapter FRAM ACCESS) and calculates the angle (θ) of the magnet. This information allows the MCU to determine whether the multiturn position is correct as read or needs to be adjusted due to runt pulses immediately prior to power-up.

When the power-up angle of the magnet θ is near a Wiegand pulse point and the last pulse polarity and direction indicate that a runt pulse may have occurred, the switched current ramp generator in the iC-PMX is used to determine rotation direction and whether the multiturn position must be corrected.

The switched current ramp generator works by injecting current into the coil of the Wiegand sensor to induce a pulse. Both positive and negative currents can be specified, depending on the power-up angle.

Fig. 2 shows a current ramp to test for a positive Wiegand pulse. The blue trace is the Wiegand coil voltage (W1) and the yellow trace is the pulse-produced voltage (VWC).

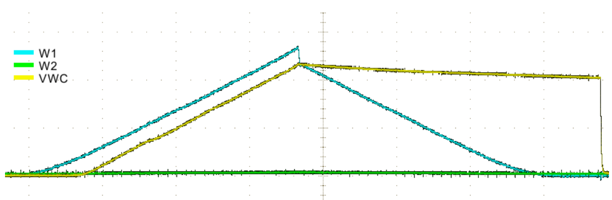


Figure 2: Positive Switched Current Ramp

The peak voltage of the current ramp is determined by the WI(1:0) register value and the electrical characteristics of the Wiegand module coil. The duration of the ramp is determined by the RAMP(3:2) parameter. All of these parameters are explained in chapter WIEGAND MODULE EXCITATION and must be set to match the Wiegand module used and the specific application requirements.

In an end-of-shaft application, the power-up angle of the magnet θ can be calculated by using the singleturn Hall sensors as explained in chapter POSITION OF THE HALL SENSORS AND SIGNAL PROCESSING. It is convenient to divide the angle θ into octants. Fig. 1 shows the power-up octants labeled in lower-case Roman numerals.

The Wiegand pulse points are in octant i, iv, v and viii, and the blackout area of the phase sequence Hall switch is around 90° and 270° (octant ii, iii, vi and vii).

The switched current ramp generator is used when the power-up angle is in octants i, iv, v, and viii - and is not used in octants ii, iii, vi, and vii, to avoid the phase sequence Hall switch blackout area (see Tab. 1).

The recommended power-up logic for the MCU is shown in Fig. 3. After any required correction, the multiturn position will then be correct as of the power-up instant.

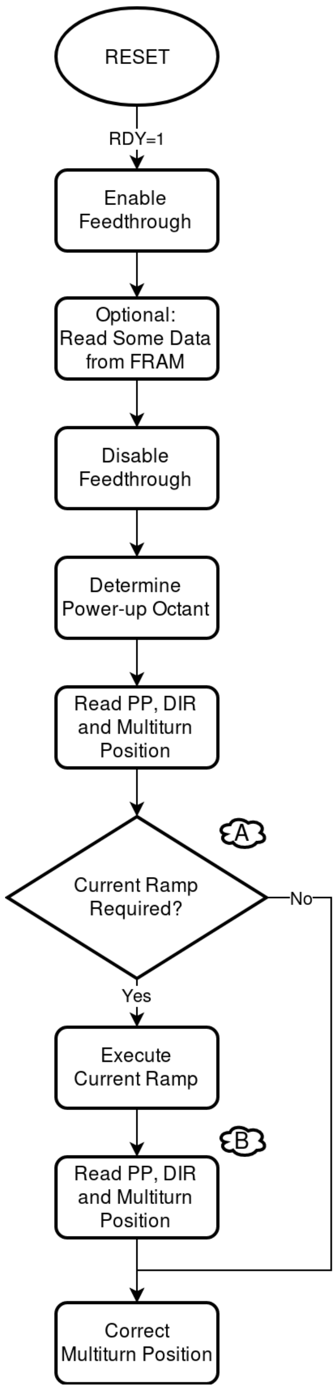


Figure 3: MCU Power-up Logic

(A) When the power-up position of the magnet is in one of the octants opposite the last pulse point, the switched current ramp generator is used to determine the past rotation direction and adjust the multiturn count accordingly, as shown in Tab. 1.

Switched Current Ramp Usage				
Last Pulse			**Power-up Octant**	**Ramp Polarity**
Point	**PP**	**DIR**		RAMP(0)
J	1	1	iv v	0 1
K	1	0	i viii	0 1
L	0	1	i viii	0 1
M	0	0	iv v	0 1

Table 1: Switched Current Ramp Usage

(B) After the current ramp is over, the multiturn position is read again and corrected if necessary. In some cases, inducing a Wiegand pulse using the switched current ramp generator causes the necessary multiturn position correction in the FRAM. In other cases the multiturn position must be corrected by the MCU, as shown in Tab. 2. When the switched current ramp generator is not necessary, the multiturn position does not need to be read again, but it still must be corrected according Tab. 2.

Multiturn Position Correction				
Last Pulse			**Power-up Octant**	
Point	**PP**	**DIR**	**i – iv**	**v – viii**
J	1	1	+1	0
K	1	0	0	0
L	0	1	0	0
M	0	0	0	–1

Table 2: Multiturn Position Correction at Power-up

Note: The multiturn position must only be corrected in the MCU, the iC-PMX/FRAM will automatically adjust its multiturn position at the next Wiegand point as explained previously.

SELF-SUSTAINED OPERATION MODE SELECTION

iC-PMX can save the period information in a standard SPI NVRAM or in a data processing FRAM. The pins C0, C1, C2 and C3 are used to choose between the FRAM interfaces and the operating modes of iC-PMX. The pins must be tied to VRAM or GND.

Pin C0	
Value	Description
0	iC-RMF / MB85RDP16LX
1	Standard SPI NVRAM[1]

Table 3: FRAM Selection

Pin C1	
Value	Description
0	Period counter mode
1	Gas gauge mode[1]

Table 4: Counter Operating Mode

Pin C2	
Value	Description
0	Differential magnetic field measurement (H4-H5)
1	Absolute magnetic field measurement (H4)

Table 5: Magnetic Field Measurement

Pin C3	
Value	Description
0	Single threshold (see Elec.Char. 402, page 10): distinguish negative and positive magnetic fields
1	Two thresholds (see Elec.Char. 401, 403, page 10): distinguish negative, insufficient and positive magnetic fields[2]

Table 6: Magnetic Field Evaluation

[1] Detailed information available on request.
[2] For iC-PMX 4: Please read the design review on page 30.

SPI SLAVE INTERFACE

iC-PMX SPI Configuration Register Overview								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	GAIN(2:0)			DIS7	SENSOR(1:0)		PHASE(1:0)	
0x01	RAMP(7:0)							
0x02	BIAS(3:0)				0	0	WI(1:0)	
0x03	TEST1(7:0)							
0x04	TEST2(7:0)							
0x05	TEST3(7:0)							
0x06	STATUS(7:0)							
0x07	REV(7:0)							

Table 7: iC-PMX SPI Configuration Register Overview

Register Map, Overview

BIAS:	Bias calibration value
GAIN:	Gain of the singleturn Hall amplifier
DIS7:	Disable singleturn sensors
SENSOR:	Hall sensor selection
PHASE:	Hall sensor measurement phase
RAMP:	Switched current ramp command
WI:	Max. current selection for the switched current ramp
TEST1:	Reserved for device test
TEST2:	Reserved for device test
TEST3:	Reserved for device test
STATUS:	Device status
REV:	Device revision

General Protocol Description

SPI modes 0 and 3 are supported, i.e. data is captured on the rising edge of SCK and the idle polarity of SCK is insignificant. Data is sent byte-by-byte with the MSB first. Each data transmission begins with the master sending an opcode. MISO is in high impedance state if NCS is high and it stays in high impedance state until a read command is received. This allows to connect MISO and MOSI to realize a 3-wire SPI interface.

The opcodes 0x20 to 0x24 are used to set configuration parameters in iC-PMX. This is done by sending the opcode followed by 8 bit configuration data as shown in Fig. 4. The 3 least significant bits of the opcode are used to select the address in the configuration memory. The parameter values are stored when the 16th rising edge of SCK is received.

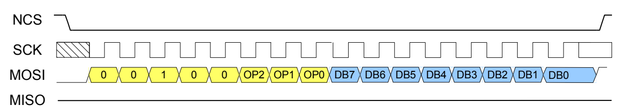


Figure 4: 16-bit Set Commands

The opcodes 0x28 to 0x2f are used to read data from iC-PMX. This is done by sending the opcode and providing 8 additional clocks on SCK as shown in Fig. 5. The 3 least significant bits of the opcode are used to select the address in the configuration memory. Output pin MISO leaves its high impedance state on the first falling edge of SCK after the opcode was received.

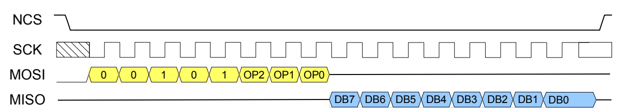


Figure 5: 16-bit Read Commands

The opcodes 0x10 to 0x1f are single byte commands to configure the most important singleturn Hall sensor parameters (see Fig. 6).

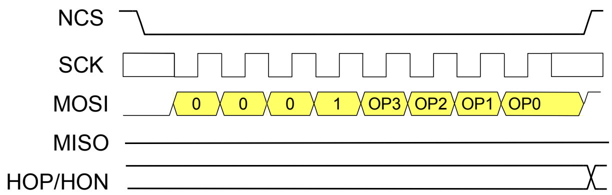


Figure 6: Singleturn Hall Output Selection

The opcode 0x30 is used to read the revolution counter data from the FRAM. The available data is explained in chapter FRAM ACCESS on page 27.

OPCODES	
Code	Description
0x10-0x1f	SELH (Select Hall Output Signal for Differential Output HOP/HON)
0x20	Set Singleturn Configuration
0x21	Set Switched Current Ramp Parameter
0x22	Set BIAS and WI Parameter
0x23	Set TEST1 Parameter
0x24	Set TEST2 Parameter
0x28	Read Singleturn Configuration
0x29	Read Switched Current Ramp Status
0x2a	Read BIAS and WI Parameter
0x2b	Read TEST1 Parameter
0x2c	Read TEST2 Parameter
0x2e	Read Status
0x2f	Read Device Revision
0x30	Read POS

Table 8: OPCODE Summary

DEVICE CALIBRATION AND SYSTEM DIAGNOSIS

BIAS Parameter

The BIAS parameter in each iC-PMX device should be calibrated to ensure accurate switched current ramp parameters and optimal operation of the singleturn sensors. It may vary from device to device. The best fitting BIAS parameter should be stored in the MCU's nonvolatile memory for later usage.

Opcode 0x22 is used to set the BIAS parameter. Valid values are shown in Tab. 9. The current source I(INT) is driving pin INT of the QFN48 packages and can also be connected to pin HOP. The nominal value of the current source is 100 µA. Its value is measured with a 10kΩ resistor against pin VDD.

Send opcode 0x23 with parameter 0x18 to connect I(INT) with pin HOP. Send opcode 0x23 with parameter 0x00 to quit this test mode.

The current setting of the BIAS parameter can be read with opcode 0x2a.

BIAS Parameter	
Value	Description
0x0	-23%
0x1	-20%
0x2	-17%
0x3	-14%
0x4	-12%
0x5	-9%
0x6	-6%
0x7	-3%
0x8	0%
0x9	+6%
0xA	+11%
0xB	+17%
0xC	+23%
0xD	+28%
0xE	+34%
0xF	+40%

Table 9: BIAS Parameter

Device Revision

Opcode 0x2f is used to read the device revision.

Device Revisions	
Value	Description
0x08	iC-PMX 0
0x0A	iC-PMX 1
0x0D	iC-PMX 4
0x0E	iC-PMX 5
0x10	iC-PMX 7

Table 10: Device Revision

Notification of Wiegand Pulses

iC-PMX can send a notification of Wiegand pulses via the SPI slave interface. This is realized by sending a 16-bit read command which is paused after the 11th clock cycle. The required opcode is 0x2e. The default state of the pin MISO is low and it changes to high during each Wiegand pulse.

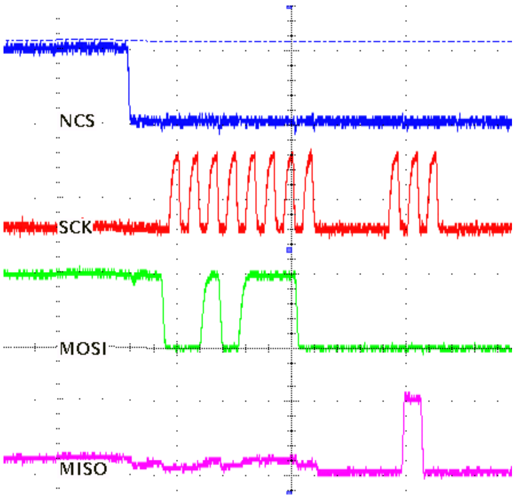


Figure 7: SPI Communication to Enable Wiegand Pulse Notification

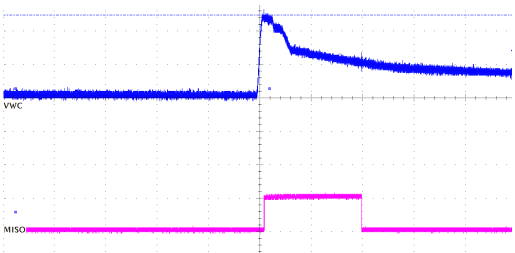


Figure 8: Wiegand Pulse Notification Through MISO Pin

End of Switched Current Ramp Detection

The status of the switched current ramp generator can be read through the SPI slave interface. This can be used to detect when the current ramp has finished.

See chapter WIEGAND MODULE EXCITATION on page 24 for details.

Pin RDY: Data Ready

Pin RDY results in high state when V(VDD) and V(VCC) are above the brownout detection threshold voltage, and the power-up startup routine has finished, and the FRAM feedthrough mode is not enabled.
When pin RDY is low, the output drivers for the single-turn sensors are in high-impedance state.
When RDY is low (or high impedance), data obtained with the SPI command Read POS shall be disregarded.

See section Singleturn Sensors on page 23 and chapter WIEGAND PULSE PROCESSING on page 25 for details.

POSITION OF THE HALL SENSORS AND SIGNAL PROCESSING

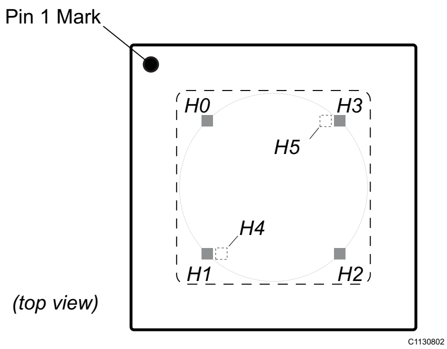


Figure 9: Position of the Hall Sensors

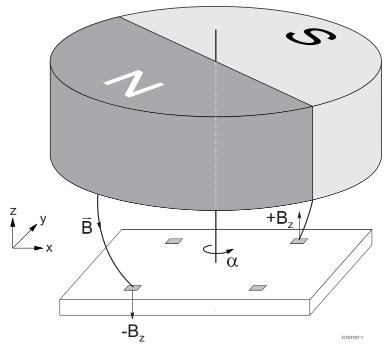


Figure 10: Sensor Principle

Phase Sequence Hall Switch
Hall data for the Wiegand pulse evaluation is acquired with the sensors H4 and H5 (see Fig. 9). Dimensional drawings for the two packages can be found on page 6 and 7. Those Hall sensors are evaluated when a Wiegand pulse occurs to detect the rotation direction.

The customer can not observe the magnetic field strength at sensor H4 and H5 directly, but the field strength can be derived from the magnetic field strength of the singleturn Hall sensors H0 to H3:

$$H_4 = H_1 + \frac{H_3 - H_1 + H_2 - H_0}{28}$$

$$H_5 = H_3 - \frac{H_3 - H_1 + H_2 - H_0}{28}$$

iC-PMX can measure the differential magnetic field strength between the Hall sensors H4 and H5 or the absolute magnetic field strength at Hall sensor H4. Pin C2 is used to choose between those two options. (See page 17: Set C2=0 for differential measurement.)

The magnetic field strength is amplified and compared against three internal thresholds (see Elec. Char. 401, 402, 403). Pin C3 is used to select the desired magnetic polarity thresholds.[1]

The rotation direction depends on the Wiegand pulse polarity and the threshold Ht() if pin C3 is low. (See Fig. 11, the magnetic field strength during the sensor evaluation must be outside of the specified threshold limits, otherwise the signal has an arbitrary value.)

If pin C3 is high, the rotation direction depends on the thresholds Ht()pos, Ht()neg and the Wiegand pulse polarity. The threshold Ht()neg is used to determine the rotation direction while the Wiegand pulse polarity is negative (PP = 0). The threshold Ht()pos is used to determine the rotation direction while the Wiegand pulse polarity is positive (PP = 1). Fig. 12 shows the required magnetic field strength for pin C2=0 and pin C3=1.

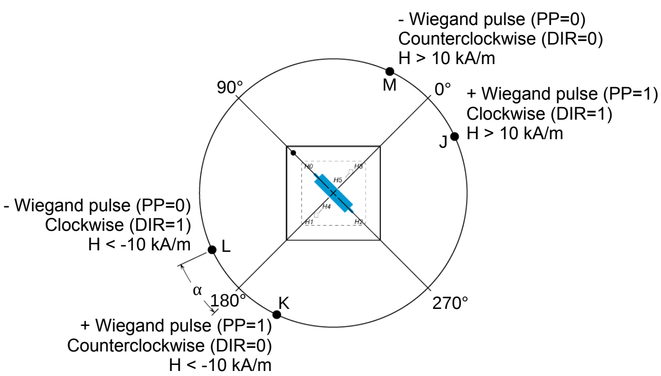


Figure 11: Required Magnetic Field Strength during Wiegand Pulses for Pin C3=0 (see Elec. Char. 402)

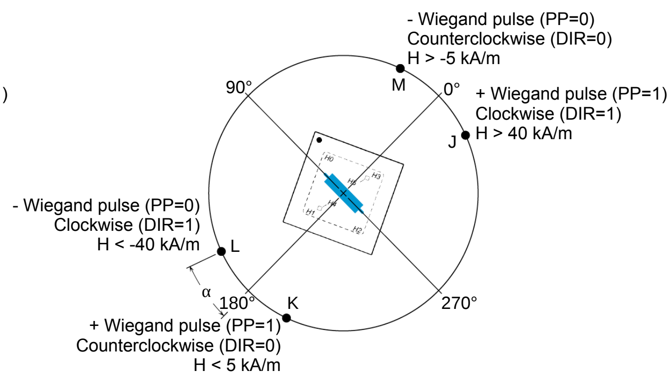


Figure 12: Required Magnetic Field Strength during Wiegand Pulses for Pin C2=0, pin C3=1 (see Elec. Char. 401, 403)

[1] For iC-PMX 4: Please read the design review on page 30.

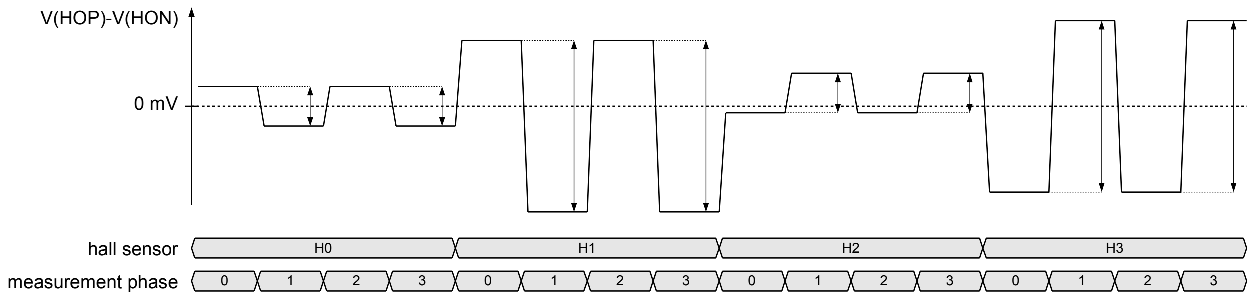


Figure 13: Hall Amplifier Output Voltages

Singleturn Sensors
The singleturn Hall sensors (H0, H1, H2, H3) are arranged in a circle with a diameter of 3.25 mm, which is placed in the center of the package as shown on page 6 and on page 7. Fig. 9 shows the position of the Hall sensors with respect to the Pin 1 mark.

The singleturn sensors are temporarily disabled while VDD or VCC are below VDDOK (brownout protection).

If a magnetic south pole comes close to the surface of the package, the resulting magnetic field has a positive component in the +z direction (i.e. from the top of the package). This results in an increase of the voltage difference between HOP and HON during the measurement phases 0 and 2. In the measurement phases 1 and 3 it results in a decrease of the voltage difference (see Fig. 13). The common mode voltage of HOP and HON is V(VUP)/2.

Four measurements with constant amplifier gain should be done for each Hall sensor to remove first and second order offset errors. This results in 16 A/D values which can be reduced to two linearly independent quantities:

$$Q_0 = (H0,0 - H0,1) + (H0,2 - H0,3) - ((H2,0 - H2,1) + (H2,2 - H2,3))$$
$$Q_1 = (H3,0 - H3,1) + (H3,2 - H3,3) - ((H1,0 - H1,1) + (H1,2 - H1,3))$$

Q_0 is proportional to $\sin(\alpha)$ and Q_1 is proportional to $\cos(\alpha)$ if the magnetic field is generated by a diametrically magnetized, cylindrical permanent magnet as shown in Fig. 10.

Singleturn Hall Output Selection
The opcodes 0x10 to 0x1f can be used to choose the singleturn Hall sensor voltage which can be measured between the pins HOP and HON.

These commands are executed when the rising edge of NCS is received. This is visualized in Fig. 6 by the signal change on HOP/HON. The value of OP1 and OP0 selects the measurement phase, the value of OP3 and OP2 selects the Hall sensor (see Tab. 11).

OPCODE 0x10...0x1f	
OP3...OP2	Select Hall sensor (0...3)
OP1...OP0	Select measurement phase (0...3)

Table 11: Fast Hall Sensor Selection

Combined Singleturn Gain and Output Selection
Opcode 0x20 must be used if the Hall amplifier should be disabled or its gain has to be changed. Tab. 12 shows the coding of the singleturn parameters within the data byte. The gain is changed straightaway with the 16th rising edge of SCK, the output selection is changed when the rising edge of NCS is received.

Singleturn Parameters	
DB7...DB5	GAIN(2:0); gain of the singleturn Hall amplifier (0...7)
DB4	DIS7; disable singleturn sensors, default value: 0
DB3...DB2	SENSOR(1:0); select Hall sensor (0...3)
DB1...DB0	PHASE(1:0); select measurement phase (0...3)

Table 12: Singleturn Parameters

Switching the Singleturn Output Selection via Pin SH
Pin SH can be used to change the singleturn output selection, if pin NCS is high.

An internal state machine switches to the next output selection whenever the voltage on pin SH changes. The sequence of output selections is fixed and documented in Fig. 13. The minimum delay between switching commands is 100 ns, as documented in Elec. Char., section Timing Parameter SPI Slave Interface. The active output selection can be read with opcode 0x28. It is also possible to set an arbitrary start value with the SPI commands.

WIEGAND MODULE EXCITATION

A Wiegand wire is a ferromagnetic material with hysteresis. Its behavior during the switched current ramp is slightly different depending on the previously applied magnetic field. The slew rate of the current ramp accentuates this nonlinearity. Fig. 14 shows such a nonlinearity excited by a high current slew rate.

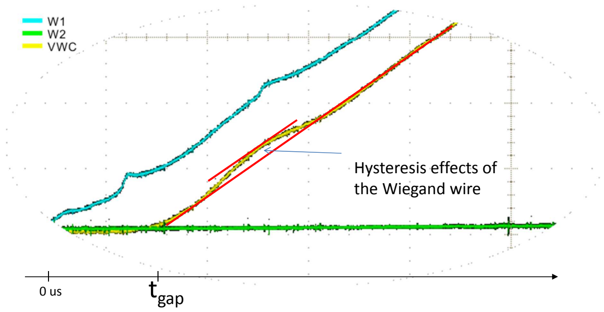


Figure 14: Nonlinearity of V(VWC) during a Current Ramp

However, since the switched current ramp parameters are usually calculated based on the resistance of the Wiegand module, some margin should be provided to compensate for the nonlinearity.

Switched Current Ramp Parameters

Opcode 0x21 is used to start a Wiegand wire excitation. Valid parameters are described in Tab. 13 and Tab. 14. This function is used to determine if the Wiegand wire is pre-charged. A current ramp is applied to the coil around the Wiegand wire. This generates an additional magnetic field, which can trigger a Wiegand pulse if the Wiegand wire is pre-charged. The current direction determines the polarity of the additional magnetic field (see Fig. 15).

The duration of the switched current ramp and the maximum current must be selected suitable for the chosen Wiegand module. The voltage slew rate during the current ramp is determined by the above parameters and the Wiegand module's electrical properties. Its worst case value should be below the allowed slew rate during current ramps (see Elec. Char. 204, page 9).

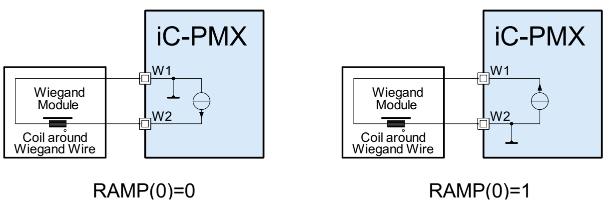


Figure 15: Switched Current Ramp Direction

WI(1:0)	
Bit	Description
1...0	Select max. current (see Elec.Char. 301, page 10), default value: 0x0

Table 13: Switched Current Ramp Parameters 1/2

RAMP(7:0)	
Bit	Description
7..4	0x7: Start current ramp, default mode 0xF: Start current ramp with disabled Hall sensor evaluation, value of MP is defined by bit 1
3...2	Select duration of current ramp (0...3) (see Elec.Char. 304, page 10)
1	Value of MP if bit 7 = 0x1
0	0: Set current direction to test for a negative Wiegand pulse (PP = low) 1: Set current direction to test for a positive Wiegand pulse (PP = high)

Table 14: Switched Current Ramp Parameters 2/2

Note: During the execution of the switched current ramp, Wiegand pulses of same polarity as the ramp are detected by iC-PMX. The switched current ramp must not be executed when a pulse with the opposite polarity may occur, which is dependent on the system design and application, i.e. its magnetic fields, programming, speed and acceleration.

Recommended Values for the Capacitors CB and CD

The capacitor CB between Pin VDD and Pin GND should be large enough to ensure that the voltage drop during the switched current ramp is less than 1V. That's an important concern during a power loss event. The brownout protection is used to continue the switched current ramp and the capacitor CB is calculated for the worst case: Power loss at the start of the switched current ramp. The voltage drop can be calculated based on the Elec. Char. 103, 301 and 304.

Calculation of CB for a Wiegand module which needs RAMP(3:2)="10" and WI(1:0)="01":

$$\begin{aligned} min(CB) &= 1400\,\mu s * (0.5 * 14\,mA + 2\,mA)\,/\,(1\,V) \\ &= 12.6\,\mu F \end{aligned}$$

The capacitor CD between Pin CP and Pin CN should also be larger than min(CB).

End of Switched Current Ramp Detection

Opcode 0x29 can be used to read the status of the switched current ramp generator. The result is equal to the values in Tab. 14 if the switched current ramp is active. The bits 4 to 6 of the status are set to zero when the switched current ramp has finished.

WIEGAND PULSE PROCESSING

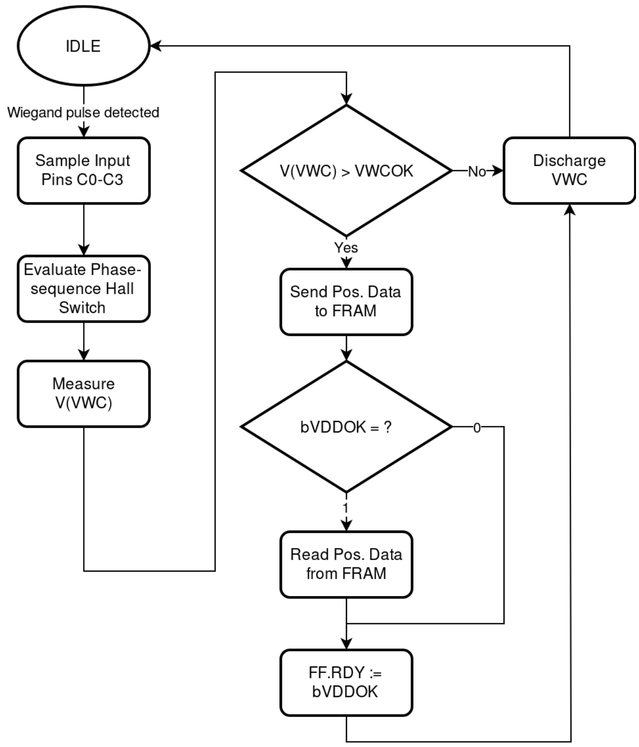


Figure 16: Wiegand Pulse Processing for C0=0, C1=0

The flowchart in Fig. 16 shows the sequence of the work steps which are performed during the Wiegand pulse processing in period counter mode.

The Wiegand pulse detection circuit is part of the active rectifier. It measures the voltage slew rate on pin VWC and signals *Wiegand pulse detected* if the required slew rate is reached. (see Elec. Char. 202)

The voltage on the capacity at pin VWC (CVWC) is measured after the evaluation of the magnetic field strength and before the communication with the FRAM is started. It is assumed that a runt pulse has occurred which can be discarded if the voltage is below the threshold voltage VWCOK. (see Elec. Char. 603)

The allowed charge consumption for the communication with the FRAM is limited by the capacity of CVWC, the minimum value of VWCOK and the maximum value of VRAMoff or the minimum power supply voltage of the FRAM. (see Elec. Char. 603 and 606) In typical applications, the minimum power supply of the FRAM is higher as VRAMoff, therefore its value must be used to calculate the allowed charge consumption for the FRAM communication. However, the consumed charge in typical real world applications is much less than the allowed charge consumption.

Note: The energy harvested from the Wiegand sensor must be high enough to ensure reliable Wiegand pulse processing.

This can be verified by measuring the voltage at pin VWC during the Wiegand pulse processing when the first falling edge at pin NCSR occurs. The measurement results must be above the maximum value of VWCOK (Elec. Char. 603) for all Wiegand pulses which are not classified as runt pulses.

The voltage at pin VWC at the beginning of the Wiegand pulse processing is higher as its value when the voltage is measured. Based on measurements in typical implementations, exemplary values for the required minimum voltages at the beginning of the Wiegand pulse processing are documented in Tab. 15.

Reading back the position data from the FRAM is optional during the Wiegand pulse processing to minimize the charge consumption in the self-sustained operating mode (Elec. Char. 114). The brownout protection circuit monitors the voltage at pin VCC and pin VDD. Reading back the position data is enabled when both voltages are above the VDDOK threshold (Elec. Char. 705). Thus the data available with the Read POS command is not changed while the brownout protection circuit detects a power loss condition - which is also signaled on pin RDY (see page 21).

Note: When the brownout protection switches to power good after sending the position data to the FRAM and before FF.RDY is updated, it is possible that the position data is not read back, but the pin RDY is allowed to switch to high. It is necessary to observe pin RDY and to explicitly trigger a readout of the position data when pin RDY switches to high, e.g. by toggling through the feedthrough mode.

Whether the brownout protection circuit signals the end of a power loss condition is checked in the IDLE state when FF.RDY is low. If that happens the position data from the FRAM is read before pin RDY is allowed to switch to high.

Item No.	Symbol	Parameter	Conditions	Min.
602	VWCon	Required Voltage on VWC	max. voltage, measured during the Wiegand pulse C1=0, C0=0, CVWC = 6.8 nF C1=0, C0=0, CVWC = 8.2 nF C1=0, C0=0, CVWC = 10 nF	 4.4 V 4.2 V 4.1 V

Table 15: Exemplary Values for Required Wiegand Pulse Voltages

FRAM ACCESS

Read POS

iC-PMX reads the position data from the FRAM as part of the Wiegand pulse processing whenever external power is available (see chapter WIEGAND PULSE PROCESSING on page 25). The revolution counter data in iC-RMF / MB85RDP16LX is optimized against imprint effects of FRAM. iC-PMX reads the data of the FRAM with the RDTS command to get a decoded data set.

The acquired information is available for the MCU by using the Read POS command (Opcode 0x30). The available data is explained in Tab. 15. It is provided byte-by-byte, starting with byte 0x0.

Position Data in Period Counter Mode with iC-RMF / MB85RDP16LX								
Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	POS(5:0)						LDIR	LPP
0x01	POS(13:6)							
0x02	POS(21:14)							
0x03	POS(29:22)							
0x04	POS(37:30)							
0x05	EFLAG(1:0)		INVALID	POS(42:38)				
0x06 ⋮ 0x0E	—							
0x0F	—				C3	C2	C1	C0

Table 16: Position Data in Period Counter Mode with iC-RMF / MB85RDP16LX (pin C0 = 0, pin C1 = 0)

Register Map, Overview

POS: Revolution counter value

LDIR: Direction of last POS change (0 = incremented, 1 = decremented)

LPP: Polarity of last Wiegand pulse (1 = positive, 0 = negative)

EFLAG(1:0): Error information (0 = no error, 1 = Overflow, 2 = uncorrectable FRAM error, 3 = incomplete write access)

INVALID: Error information (0=data is valid, 1=position data changed during read access, please discard the data and read it again)

C3, C2, C1, C0: Value of the pins C3-C0, sampled during the last wiegand pulse processing

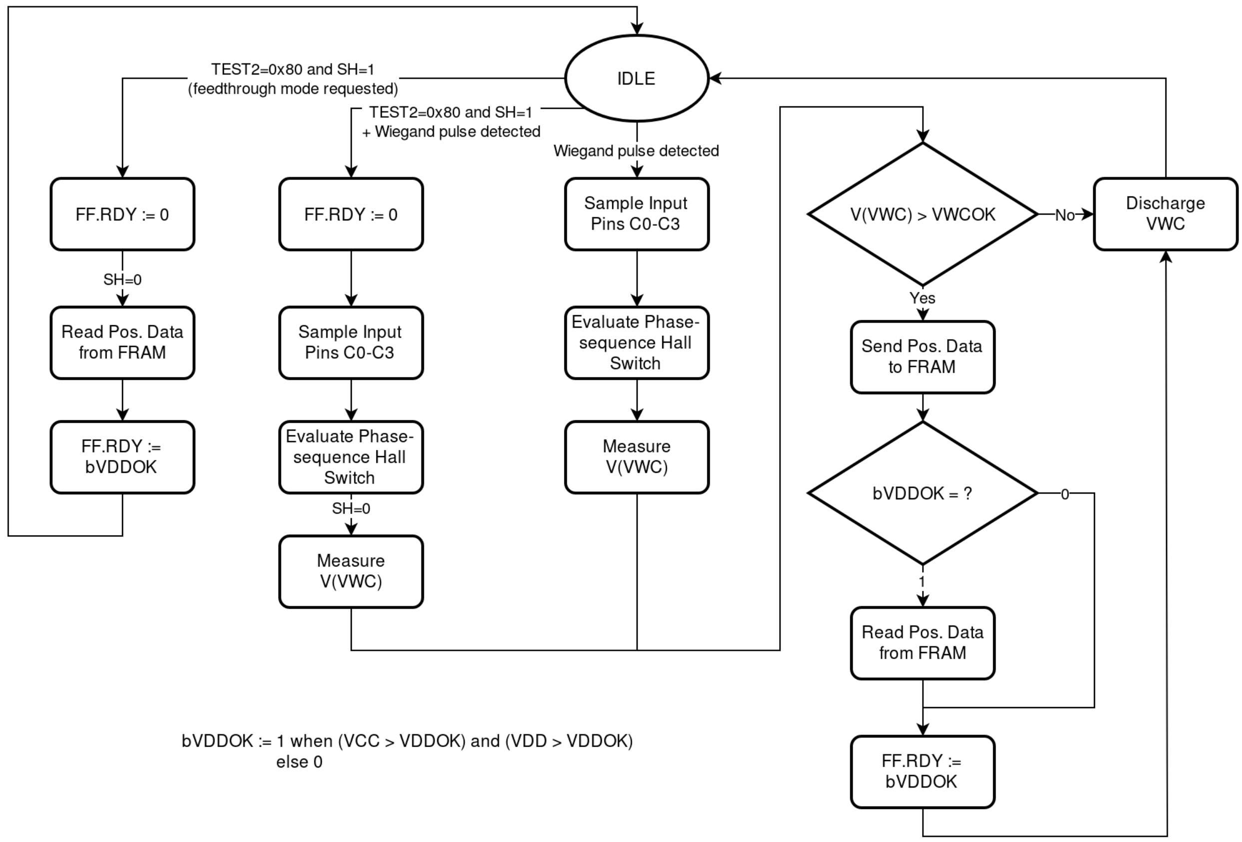


Figure 17: Flowchart Describing Feedthrough Mode and Wiegand Pulse Processing for C0=0, C1=0

FRAM Feedthrough Access

iC-PMX has a feedthrough mode to allow direct access to the FRAM. iC-PMX gives exclusive access to the FRAM once the feedthrough mode is activated. The FRAM access is delayed, if iC-PMX itself is using the FRAM. Pin RDY is pulled low as soon as the feedthrough mode can by used.

The feedthrough mode is activated if *TEST2* is programmed with 0x80 and pin SH is high. Pin SH must be set to low to disable the feedthrough mode. Code examples to enable and disable the feedthrough mode are available on page 29.

In feedthrough mode the data at pins NCS, SCK and MOSI is used to drive NCSR, SCKR and MOSIR. The data at MISOR is sampled with an internal clock and those values are used to drive MISO.[1] The data is not interpreted in iC-PMX.

The flowchart in Fig. 17 shows the interaction of Wiegand pulse processing and feedthrough mode. A request to enter feedthrough mode is only evaluated in IDLE state and the exception handling for concurrently detected Wiegand pulses is also shown in the flowchart.

Note: The duration of the feedthrough mode must be kept short in applications in which Wiegand pulses can occur during the feedthrough mode.

Fig. 17 indicates that switching the pin SH to low is enough to end the feedthrough mode. It is suggested to split complex communications in short self-contained parts and to allow for Wiegand pulse processing between these parts by toggling the pin SH appropriately. The maximum duration of the feedthrough mode after the occurrence of a Wiegand pulse (Elec. Char. I03) is limited by the hold time of the Wiegand pulse detection.

iC-PMX reads the position data from the FRAM when the feedthrough mode is deactivated if the brownout protection does not signal a power loss condition.

[1] Corresponding timing parameters are documented as Elec. Char. I01 and I02 on page 14

Code Example to Enable the Feedthrough Mode

```
uint32_t pmxEnableFeedthrough(void)
{
  if (INPUT_VALUE(PMX_RDY_PIN)==0) {   // if pin RDY = low
    pmxStatus->PMX_NOT_READY = 1;
    return 1;
  }
  OUTPUT_CLEAR(PMX_SH_PIN);                 //   set pin SH low
  OUTPUT_CLEAR(PMX_NCS_PIN);                //   set pin NCS low
  pmxSpiSend(0x24);                         // send opcode 0x24
  pmxSpiSend(0x80);                         //   send TEST2=0x80
  OUTPUT_SET(PMX_NCS_PIN);                  // set pin NCS high
  OUTPUT_SET(PMX_SH_PIN);                   //   set pin SH high
  pmxWait4Rdy(0,100);                 // wait until pin RDY = 0
                                // (but not longer than 100 us)
  if (INPUT_VALUE(PMX_RDY_PIN)==1) { // if pin RDY = high
    // (this should never happen)
    pmxStatus->FRAM_ACCESS_DENIED = 1;
    return 1;
  }
  usleep(1);          // wait for tpu(NCSR) (el. char. C03)
  // The pin MISO of the FRAM is sampled with an internal
  // clock of at least 7.5 MHz. The frequency of the
  // following SPI communications is reduced to 1.5 MHz
  // to take the resulting added latency into account.
  pmxSpiFrq(1.5);             // set SPI frequency to 1.5 MHz
  return 0;
}
```

Code Example to Disable the Feedthrough Mode

```
uint32_t pmxDisableFeedthrough(void)
{
  OUTPUT_CLEAR(PMX_SH_PIN);                //     set pin SH low
  pmxWait4Rdy(1,100);              // wait until pin RDY = 1
                               // (but not longer than 100 us)
  // set SPI frequency to its default value (e.g. 6 MHz):
  pmxSpiFrq(6);
  OUTPUT_CLEAR(PMX_NCS_PIN);               //    set pin NCS low
  pmxSpiSend(0x24);                        //   send opcode 0x24
  pmxSpiSend(0x00);                        //    send TEST2=0x00
  OUTPUT_SET(PMX_NCS_PIN);                 //   set pin NCS high
  return 0;
}
```

DESIGN REVIEW: Notes on Chip Functions

iC-PMX 4		
No.	Function, Parameter/Code	Description and Application Hints
1	Pin C3	Pin C3 must tied to GND
2	Elec. Char. 402	Different limits for the magnetic field strength threshold with pin C2=0, pin C3=0: limits are -20 kA/m . . . +20 kA/m
3	Mode TEST2 (FRAM Feedthrough Mode)	During feedthrough mode the readout of pin MISO might be disturbed by internal crosstalk and should be secured by repetition.

Table 17: Notes on chip functions regarding chip release iC-PMX 4.

iC-PMX 5		
No.	Function, Parameter/Code	Description and Application Hints
1	Mode TEST2 (FRAM Feedthrough Mode)	During feedthrough mode the readout of pin MISO might be disturbed by internal crosstalk and should be secured by repetition.

Table 18: Notes on chip functions regarding chip release iC-PMX 5.

iC-PMX 7		
No.	Function, Parameter/Code	Description and Application Hints
		None at time of release.

Table 19: Notes on chip functions regarding chip release iC-PMX 7.

REVISION HISTORY

Rel.	Rel. Date[1]	Chapter	Modification	Page
A1	2014-12-05	ABSOLUTE MAXIMUM RATINGS	G005	7
		ELECTRICAL CHARACTERISTICS	114, 204, 301, 303, 304, 601, 603, 608	8-11
		DEVICE CALIBRATION AND SYSTEM DIAGNOSIS	Added information that the BIAS calibration is needed to ensure accurate switched current ramp parameters	14
		POSITION OF THE HALL SENSORS AND THE SENSOR SIGNAL PROCESSING	Corrected the formula for Q_1.	16
		WIEGAND MODULE EXCITATION	Corrected page references in Tab. 14 and Tab. 15	17
		WIEGAND MODULE EXCITATION	Modified calculation example for min(CB)	17
		FRAM ACCESS	Added information that pin RDY is pulled low during feedthrough mode Improved programming sequence for feedthrough mode	18
		FRAM ACCESS	Added information about INVALID and C3-C0 in the Read POS data sets and for period counter mode with standard FRAM and for gas gauge mode	18-22

Rel.	Rel. Date[1]	Chapter	Modification	Page
A2	2017-03-17	ELECTRICAL CHARACTERISTICS	402	8
		ELECTRICAL CHARACTERISTICS	Removed 401, 403, C10	
		SELF-SUSTAINED OPERATION MODE SELECTION	Tab. 6: Pin C3 must be 0	12
		SPI SLAVE INTERFACE	Tab. 9: Minor changes	13
		DEVICE CALIBRATION AND SYSTEM DIAGNOSIS	Added device revision of iC-PMX 5	14
		POSITION OF THE HALL SENSORS AND THE SENSOR SIGNAL PROCESSING	Extended the description for the 'Phase sequence Hall switch'	15
		WIEGAND MODULE EXCITATION	Added information on nonlinearities of a Wiegand wire, added Fig. 'Switched Current Ramp Direction'	17

Rel.	Rel. Date[1]	Chapter	Modification	Page
A3	2017-05-02	ELECTRICAL CHARACTERISTICS	302, 401-403	10
		SELF-SUSTAINED OPERATION MODE SELECTION	Tab. 6: allowed C3=1	17
		POSITION OF THE HALL SENSORS AND THE SENSOR SIGNAL PROCESSING	Extended the description for the 'Phase sequence Hall switch'	22
		DESIGN REVIEW: Notes on Chip Functions	Chapter added	30

Rel.	Rel. Date[1]	Chapter	Modification	Page
A4	2018-06-07	PACKAGES	PIN CONFIGURATION QFN48 7 mm x 7 mm, pin 1-10: corrected misalignment of column 'Function'	4
		ELECTRICAL CHARACTERISTICS	602	10
		DEVICE CALIBRATION AND SYSTEM DIAGNOSIS	Added device revision	20
		FRAM ACCESS	Extended information about INVALID in the Read POS data sets	27

Rel.	Rel. Date[1]	Chapter	Modification	Page
A5	2019-07-17	PACKAGES	Added RoHS compliant statement	1
		ELECTRICAL CHARACTERISTICS	Corrected parameter name of F06 and F07	13
		DEVICE CALIBRATION AND SYSTEM DIAGNOSIS	Added device revision of iC-PMX 7	20
		POSITION OF THE HALL SENSORS AND THE SENSOR SIGNAL PROCESSING	Added note hint on Wiegand pulses during the switched current ramp	24
		FRAM ACCESS	Added C code examples to enable and disable the feedthrough mode	29

		DESIGN REVIEW: Notes on Chip Functions	Updated design review for iC-PMX 4, iC-PMX 5 and iC-PMX 7	30

Rel.	Rel. Date[1]	Chapter	Modification	Page
A6	2019-09-25	ELECTRICAL CHARACTERISTICS	Added timing parameters for FRAM feedthrough mode (I01, I02)	14
		FRAM ACCESS	Changed the C code example to enable the feedthrough mode. The SPI frequency is set to 1.5 MHz, since many SPI masters sample the input data with the rising edge of SCK.	29

Rel.	Rel. Date[1]	Chapter	Modification	Page
B1	2020-03-04	DESCRIPTION	Added information	2
		Contents	Table of Contents added	3
		PACKAGING INFORMATION	Description added for IC top marking	4, 5
		ABSOLUTE MAXIMUM RATINGS	G010, G012	8
		ELECTRICAL CHARACTERISTICS	Removed 503, 504, 508, 602	9-14
		ELECTRICAL CHARACTERISTICS	108, 204, I03	9-14
		OPERATION AT POWER-UP	Chapter added	15
		DEVICE CALIBRATION AND SYSTEM DIAGNOSIS	Extended information about pin RDY	21
		WIEGAND PULSE PROCESSING	Chapter added	25
		FRAM ACCESS	Extended information about feedthrough mode	27
			Removed information that is not relevant for period counter applications	

Rel.	Rel. Date[1]	Chapter	Modification	Page
B2	2024-02-14	FEATURES	Modified the footnote about basic patents	1
		WIEGAND MODULE EXCITATION	Corrected formula for min(CB)	24

Rel.	Rel. Date[1]	Chapter	Modification	Page
B3	2024-08-14	FEATURES	Modified footnote about patents.	1
		DESCRIPTION	Added note on patent situation.	2

[1] Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-PMX	QFN32 5 mm x 5 mm	iC-PMX QFN32-5x5
iC-PMX	QFN48 7 mm x 7 mm	iC-PMX QFN48-7x7

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