iC-NG
8-BIT Sin/D CONVERTER-PROCESSOR

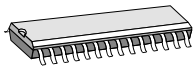
FEATURES

- Real-time interpolator with a programmable resolution of up to 256 steps/period
- Calibration features permit adaptation of distorted sine/cosine signals
- Output with A/B/Z incremental signals of up to 400kHz, as a parallel 8-bit absolute vector or via a serial interface
- Error messaging with excessive input frequency
- Programmable index position
- Fast 24-bit multiturn counting (position capture with target position interrupt)
- 8-bit µP interface
- Interrupt controller
- Adjustable clock oscillator
- Front-end amplifiers configurable externally
- Chip setup can be loaded from a serial EEPROM
- TTL-compatible inputs, TTL-/CMOS-compatible outputs
- Inputs and outputs protected against destruction by ESD

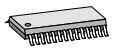
APPLICATIONS

- Absolute and incremental angle interpolation from orthogonal sinusoidal input signals
- Interpolating interface for MR sensors and optical analog encoders

PACKAGES

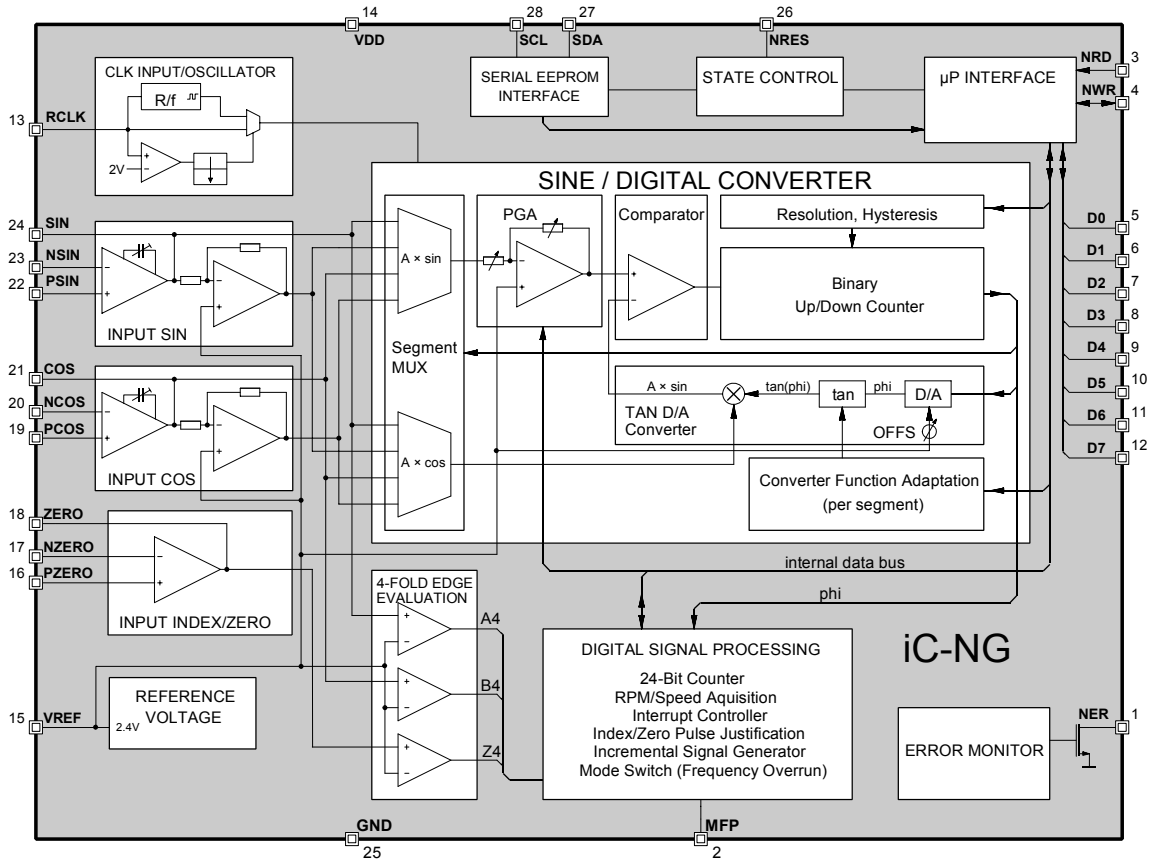


SO28



SSOP28

BLOCK DIAGRAM



DESCRIPTION

iC-NG is a monolithic A/D converter which determines the angle value of two sinusoidal input signals phase-shifted at 90° with a given resolution and hysteresis. In this process a cycle is divided into 8 segments; each of these segments can be given a resolution of up to 32 angular steps. Resolutions of 1 to 256 divisions per cycle are possible.

The converter can be adjusted for each individual segment to suit various types of input signal, meaning that even distorted sine signals or triangular signals, for example, can be converted. In addition, the direction of rotation can be inverted and the zero position can be set in steps of 45°.

Output values and parameters are stored in registers connected to the internal 8-bit data bus. A parallel microcontroller interface gives read and write access to these registers. If an EEPROM is connected to the serial interface, the chip setup can be automatically read in following a reset.

The output value consists of an 8-bit word for interpolation within a cycle and a 24-bit position counter which logs the number of turns. In addition to normal accessibility, the output value can also be transferred serially.

The position counter can be reset via the zero pulse or stopped and started using the bi-directional MFP pin. When programmed as an output, pin MFP shows the change in output value or indicates when a certain position has been reached (interrupt output). After a reset, the interpolation result is correct after just a few clock cycles, even with static input signals.

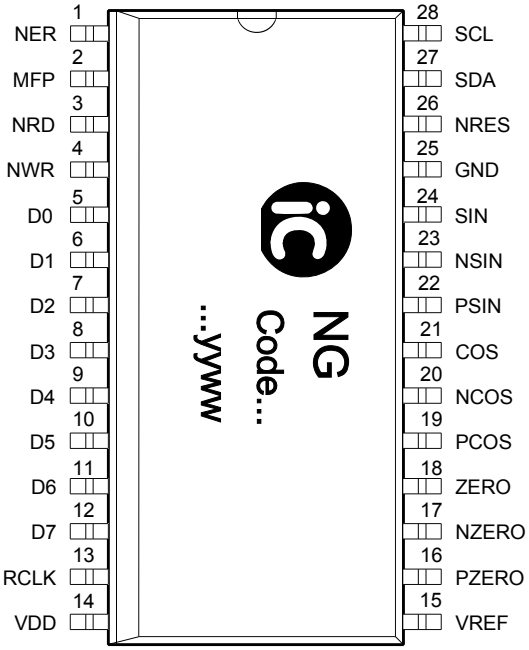
If incremental mode is selected, the changes in angle are output as square-wave signals phase-shifted at 90° at pins D0(AX) and D1(BX) with a selected resolution and at pins D3(A4) and D4(B4) with a resolution of four. The suitably prepared zero signal is at D2(ZX) and D5(Z4). Pin D6(ROT) shows the direction of rotation. Tracks AX and BX are EX-OR-gated at pin D7(AXB).

The front-end amplifier connections are all lead out, enabling current or voltage inputs to be made. Complementary input signals can also be connected. The front-end amplifiers are compensated internally; the value of compensation can be programmed.

The internal clock frequency can be adjusted using an external resistor or can be fed in via pin RCLK. The clock pulses which occur between two changes in output are counted in order to calculate the number of revolutions. Low voltage and excessive input frequency errors are signaled at output NER (open drain). These error codes are stored in the relevant register.

PACKAGE SO28, SSOP28 to JEDEC Standard

PIN CONFIGURATION SO28
(top view)

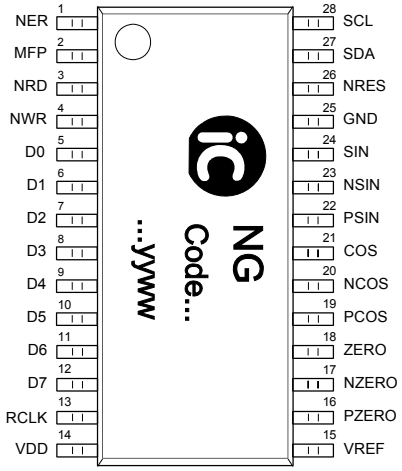


PIN FUNCTIONS

No.	Name	Function
1	NER	Error Message Output, low active
2	MFP	Multi-Functional I/O Pin
3	NRD	Read Signal, low active [1] / SSI Clock
4	NWR	Write Signal, low active [1] / SSI Output
5	D0	Data Bus / Incremental Output A (AX)
6	D1	Data Bus / Incremental Output B (BX)
7	D2	Data Bus / Index Output Z (ZX)
8	D3	Data Bus / Sine-to-Square Output A (A4)
9	D4	Data Bus / Cosine-to-Square Output B (B4)
10	D5	Data Bus / Index-to-Square Output Z (Z4)
11	D6	Data Bus / CW-CCW Signal (ROT)
12	D7	Data Bus / AX EXOR BX (AXB)
13	RCLK	Clock Input / Clock Oscillator Setting
14	VDD	+5V Supply Voltage
15	VREF	Reference Center Voltage
16	PZERO	Zero Amplifier Positive Input
17	NZERO	Zero Amplifier Negative Input
18	ZERO	Zero Amplifier Output
19	PCOS	Cosine Amplifier Positive Input
20	NCOS	Cosine Amplifier Negative Input
21	COS	Cosine Amplifier Output
22	PSIN	Sine Amplifier Positive Input
23	NSIN	Sine Amplifier Negative Input
24	SIN	Sine Amplifier Output
25	GND	Ground
26	NRES	Reset, low active
27	SDA	Mode Select / Data (Serial Interface)
28	SCL	Mode Select / Clock (Serial Interface)

Notes: 1) wiring to VDD recommended when not in use.

PIN CONFIGURATION SSOP28 5.3mm
(top view)



ABSOLUTE MAXIMUM RATINGS

Values beyond which damage may occur; device operation is not guaranteed.

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VDD	Supply Voltage			-0.3	6.0	V
G002	V()	Voltage at SIN, NSIN, PSIN, COS, NCOS, PCOS, ZERO, NZERO, PZERO, VREF, MFP, RCLK, NER, D0..7, NRD, NWR, NRES, SCL, SDA			-0.3	VDD+0.3	V
G003	Imx(VDD)	Current in VDD			-50	50	mA
G004	Imx(GND)	Current in GND			-50	50	mA
G005	Ic()	Current in Clamping Diodes SIN, NSIN, PSIN, COS, NCOS, PCOS, ZERO, NZERO, PZERO, VREF, MFP, RCLK, NER, D0..7, NRD, NWR, NRES, SCL, SDA	MFP, D0..7, NWR with input function		-5	5	mA
G006	I()	Current in SIN, COS, ZERO, VREF, MFP, NER, D0..7, NWR, SCL	MFP, D0..7, NWR with output function		-10	10	mA
G007	Ilu()	Pulse Current in all Pins (Latch-Up Strength)	pulse duration ≤ 10µs		-100	100	mA
E001	Vd()	ESD Susceptibility at all Pins	MIL-STD-883, Method 3015, HBM; 100pf discharged through 1.5kΩ			2	kV
TG1	Tj	Junction Temperature			-40	150	°C
TG2	Ts	Storage Temperature			-40	150	°C

THERMAL DATA

Operating conditions: VDD= 5V ±10%

Item	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T1	Ta	Operating Ambient Temperature Range (extended temperature range on request)			-20		70	°C

All voltages are referenced to ground unless otherwise noted.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD= 5V ±10%, Tj= -40..125°C, unless otherwise noted.

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VDD	Permissible Supply Voltage				4.5		5.5	V
002	I(VDD)	Supply Current	outputs not active			5		25	mA
003	Vt()hi	Input Threshold Voltage hi at D0..D7, MFP,NRD,NWR,NRES						2	V
004	Vt()lo	Input Threshold Voltage lo at D0..D7, MFP,NRD,NWR,NRES				0.8			V
005	Vt()hys	Input Hysteresis at D0..D7, MFP,NRD,NWR,NRES	Vt()hys= Vt()hi -Vt()lo			100			mV
006	Iin()	Input Current at D0..D7, MFP,NRD,NWR,NRES				-1		+1	µA
7	Vs()lo	Saturation Voltage lo at D0..D7, MFP	I()= 4mA					0.4	V
8	Vs()hi	Saturation Voltage hi at D0..D7, MFP	Vs()hi= VDD -V(); I()= -4mA					0.4	V
E001	Vc()hi	Clamp Voltage hi at all Pins	Vc()hi= V() -VDD; I()= 1mA, other pins open			0.3		1.5	V
E002	Vc()lo	Clamp Voltage lo at all Pins	I()= -1mA, other pins open			-1.5		-0.3	V
Input Amplifiers SIN, COS, INDEX/ZERO									
101	Vin()	Recommended Input Voltage Range				1		3.5	Vpp
102	Vos()	Input Offset Voltage	Vin()= 1V..VDD -1V			-10		+10	mV
103	Iin()	Input Current				-50		+50	nA
104	Vcm()	Common Mode Voltage Range	Iout()= 0..±5mA			0.1		VDD-1.0	V
105	Vs()hi	Saturation Voltage hi	Vs()hi= VDD -V(), Iout()= -5mA					0.5	V
106	Vs()lo	Saturation Voltage lo	Iout()= 5mA					0.5	V
107	SR0	Slew-Rate	CL= 0, C_C= 0 (C_C programmed)				4		V/µs
108	SR1	Slew-Rate	CL= 300pF, C_C= 4pF				2		V/µs
109	SR2	Slew-Rate	CL= 800pF, C_C= 6.4pF				1.2		V/µs
110	SR3	Slew-Rate	CL= 1.5nF, C_C= 12pF				0.8		V/µs
111	GBW0	Gain Bandwidth Product	CL= 0, C_C= 0 (C_C programmed)				4.1		MHz
112	GBW1	Gain Bandwidth Product	CL= 300pF, C_C= 4pF				1		MHz
113	GBW2	Gain Bandwidth Product	CL= 800pF, C_C= 6.4pF				0.75		MHz
114	GBW3	Gain Bandwidth Product	CL= 1.5nF, C_C= 12pF				0.4		MHz
Reference VREF									
115	V(VREF)	Reference Voltage	I(VREF)= 0..-1mA			2.2	2.4	2.6	V
Error Monitor NER									
201	Vs()lo	Saturation Voltage lo at NER	I(NER)= 5mA				0.2	0.7	V
202	Isc()lo	Short-Circuit Current lo in NER	V(NER)= 0.4..VDD+0.3V			5		21	mA
203	I0()	Leakage Current in NER	V(NER)= 0..VDD+0.3V, NER= hi oder VDD< 0.3V					10	µA
204	VDDon	Turn-on Threshold VDD					4.7		V
205	VDDoff	Undervoltage Threshold VDD	decreasing voltage VDD				4.5		V
206	VDDhys	Hysteresis	VDDhys= VDDon -VDDoff				200		mV
207	VDDerr	Supply Voltage VDD for Monitor Operation				2.2		5.5	V

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD= 5V ±10%, Tj= -40..125°C, unless otherwise noted.

Item	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Oscillator RCLK									
301	fmax	Permissible Oscillator Frequency						5	MHz
302	fosc	Oscillator Frequency	Rosc= 56kΩ Rosc= 18.2kΩ			550 1.6	670 1.8	800 2.0	kHz MHz
303	R(RCLK)	Permissible Resistor				5		500	kΩ
304	Vt()hi	Threshold Voltage hi						3	V
305	Vt()lo	Threshold Voltage lo	tw()lo< 10µs			0.8			V
306	Vt()hys	Hysteresis	Vt()hys= Vt()hi -Vt()lo			100			mV
307	tmx()lo	Permissible Pulse Width lo when applying external clock signals						10	µs
Serial EEPROM Interface SCL, SDA									
401	Vt()hi	Threshold Voltage hi						2	V
402	Vt()lo	Threshold Voltage lo				0.8			V
403	Vt()hys	Input Hysteresis	Vt()hys= Vt()hi -Vt()lo			300			mV
404	Vs()lo	Saturation Voltage lo	I()= 4mA				0.26	0.4	V
405	Vs()hi	Saturation Voltage hi	Vs()hi= VDD -V(); I()= -4mA					0.4	V
406	Rpu()	Pull-up Resistor				5	10	20	kΩ
Converter Accuracy									
501	AAabs	Absolute Angular Accuracy	referred to 360° input signal; VDD= 5V, V(SIN,COS)= 3Vpp, RES= 256, ADAP= 0, FREQ= 1; Rosc= 56kΩ, Tj= -20..70°C Rosc= 18.2kΩ, Tj= -20..70°C Rosc= 18.2kΩ, Tj= -40..125°C			 -0.8 -1.6 -2.8		 +0.8 +1.6 +2.8	 DEG DEG DEG
502	AArel	Relative Angular Accuracy	see 501, referred to period of AX output signal; Rosc= 56kΩ, Tj= -20..70°C Rosc= 18.2kΩ, Tj= -20..70°C Rosc= 18.2kΩ, Tj= -40..125°C			 -20 -30 -30		 +20 +30 +30	 % % %

ELECTRICAL CHARACTERISTICS DIAGRAMS

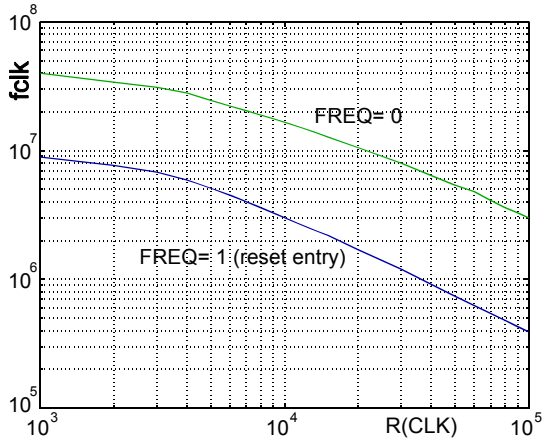


Fig. 1: oscillator frequency characteristics.

OPERATING REQUIREMENTS: Logic

Operating conditions: VCC= 5V ±10%, Ta= -20..70°C, CL()= 150pF,
input levels lo= 0..0.45V, hi= 2.4V..VCC, see Fig. 2 for reference levels and waveforms

Item	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
Read cycle							
I1	t_{RD}	Read Data Access Time: data valid after NRD hi→lo	1st access with latching NG and COUNT data ongoing access	3		1.5x td(CLK) 120	ns
I2	t_{DF}	Read Data Hold Time: ports high impedance after NRD lo→hi		3		65	ns
I3	t_{RL}	Required Read Signal Duration at NRD	 SSI signal	3	200	 2.5x td(CLK)	ns
Write cycle							
I4	t_{DW}	Write Data Setup Time: data valid before NWR lo→hi		3	100		ns
I5	t_{WD}	Write Data Hold Time: data valid after NWR lo→hi		3	10		ns
I6	t_{WL}	Required Write Signal Duration at NWR		3	200		ns
Write / read timing							
I7	t_{cyc}	Recovery Time between Cycles: NRD lo→hi to NRD hi→lo, NRD lo→hi to NWR hi→lo, NWR lo→hi to NWR hi→lo, NWR lo→hi to NRD hi→lo		3	2× td(CLK)		ns

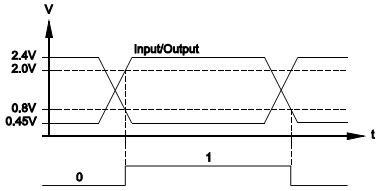


Fig. 2: reference levels

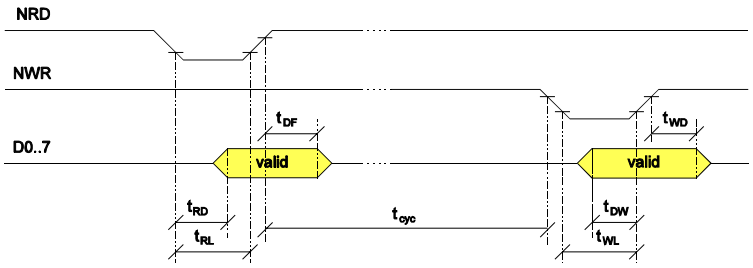


Fig. 3: read / write timing

DESCRIPTION OF FUNCTIONS

Converter principle

iC-NG is an analog-digital tracking-type converter (compensation process). The output value is stored in an up/down counter. This is converted to analog voltage by a D/A converter and compared to the input signal by a comparator. The comparator output controls the direction input of the counter. The count direction is maintained until the output voltage of the D/A converter, which is proportional to the output value, corresponds to the value of the input voltage.

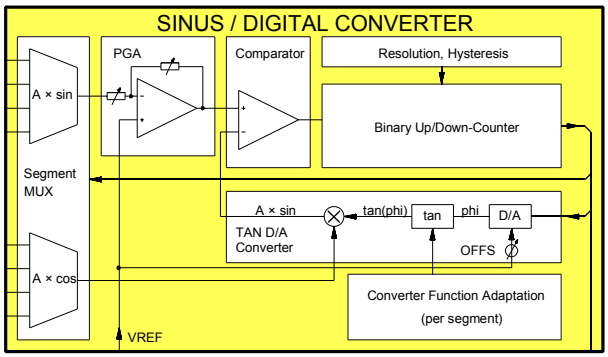


Fig. 4: core of the TAN D/A converter

In contrast to conventional A/D converters, the output value in the sine/digital converter is proportional not to the input voltage but to its phase. In the following, the input value is referred to as “PHI“ and the output value as “phi“.

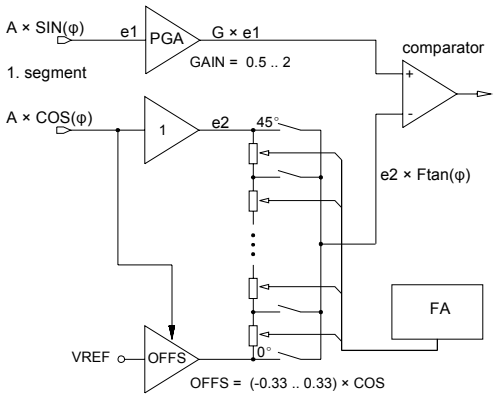


Fig. 5: converter principle

The phase is available at the input in the form A x SIN(PHI) and A x COS(PHI). From the output value, the tangent function is formed in the feedback loop and multiplied by COS(PHI). The result is compared to SIN(PHI). The rule for regulation is as follows:

$$A*SIN(\Phi) = A*COS(\Phi) \times TAN(\varphi)$$

Since the tangent function has pole points and cannot be formed over a whole cycle, a cycle is divided into eight segments. For certain segments the input signals are reversed and the cotangent function is formed in the feedback loop. The segment changeover function is indicated in the following table:

Segments		Comparator Inputs	
1	phi= 0°..45°	A×SIN(PHI)	A×COS(PHI) × |TAN(phi)|
2	phi= 45°..90°	A×COS(PHI)	A×SIN(PHI) × |COT(phi)|
3	phi= 90°..135°	–A×COS(PHI)	A×SIN(PHI) × |COT(phi)|
4	phi= 135°..180°	A×SIN(PHI)	–A×COS(PHI) × |TAN(phi)|
5	phi= 180°..225°	–A×SIN(PHI)	–A×COS(PHI) × |TAN(phi)|
6	phi= 225°..270°	–A×COS(PHI)	–A×SIN(PHI) × |COT(phi)|
7	phi= 270°..315°	A×COS(PHI)	–A×SIN(PHI) × |COT(phi)|
8	phi= 315°..360°	–A×SIN(PHI)	A×COS(PHI) × |TAN(phi)|

Fig. 6: segmentation

The sine/digital converter automatically runs via the shortest route into the correct segment and thus, with a static input signal, reaches its operating point after a maximum of n/2 clock cycles (n corresponds to the resolution).

A converter of the type described above will never reach a quiescent state. With a constant input signal, the counter would continuously increment or decrement one LSB, which is prevented here by hysteresis. A range is set up by the programmable hysteresis on both sides of the counter value and the input signal is checked over two clock cycles as to whether it is still within this range. The output frequency is therefore only half the clock frequency.

Interfaces

The chip must be configured for the application in use after being switched on and after every reset. The settings and output values are stored in registers in iC-NG.

There are various ways of accessing these registers. If a serial EEPROM (e.g. SDA 2516, ST24CO2) is con-nected to pins SDA and SCL, all parameters will be read in automatically from there. The access mode is also determined by the EEPROM (ACCMOD(1:0)).

In the absence of an EEPROM, the access mode is set directly by pins SDA and SCL, which are equipped with internal pull-up resistors. Three modes are supported:

SDA	SCL	Access Mode (no EEPROM)
0	0	Parallel absolute mode
1	0	Serial mode
1	1	Incremental mode

Fig. 7: access modes

1. Parallel-absolute mode

This mode is suitable for using iC-NG as peripheral chip in an 8-bit bus system. The registers can be accessed via the data ports D0 to D7, controlled by read / write access inputs NWR and NRD. The two pins should not simultaneously receive low level.

Addressing is controlled via an internal address register and a status machine. The internal status (A or B) determines whether write access affects the address register or a data register addressed by it. The chip is in status A after a reset and each read, and in status B after each write (Figure 8).

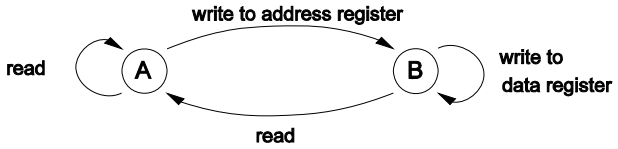


Fig. 8: status control.

Write access

The data to be written is applied to pins D0 to D7 and a low pulse to NWR. The data is accepted with the rising edge at NWR. A write cycle consists of at least two accesses. The register address is given by the first access and the date by the second. The internal address register is automatically increased by one after each write. The registers of successive addresses can thus be easily written without having to reload the address register. A write cycle to address 10 and a subsequent read out are indicated in Figure 9.

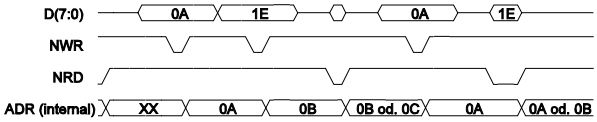


Fig. 9: write access to address 10 and subsequent read out.

Read access

For a read cycle, the register address is also given first (write access), the data content then being read out with NRD at low.

The length of the output value is set to 1..4 bytes with the OUTSEL(1:0) registers. OUTSEL also influences the content of the internal address counter after a read. It is not increased if the length of the output value is set to one byte. Other settings reset the address counter to zero after the highest byte of the output value has been read, otherwise it is increased by one.
The outputs remain constant during the read process, even if the relevant register changes (except incremental signals and interrupt and error status).

The NG, COUNT and TACHO registers are again stored with the falling edge at NRD if OUTSEL has been programmed to zero or the address counter is at zero. It is thus possible to read a 4-byte output value in four accesses.

The interval between two consecutive pulses to NRD or NWR must be at least 3 clock cycles. The cyclic read out of a 2-byte output value (OUTSEL(1:0)= 1) is shown in Figure 10.

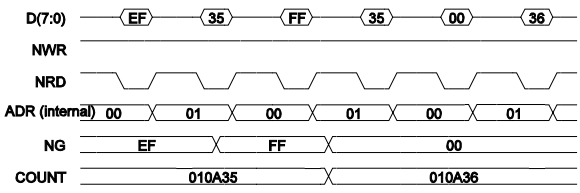


Fig. 10: cyclic read out of the output value (16-bit).

2. Synchronous-serial mode with 33-bit format

In this mode, communication is via a synchronous two-wire connection. The registers cannot be accessed; only the output value and the error bit are transmitted.

The two-wire connection exists of a clock input (NRD) and a data output with driver at NWR. Data transmission is controlled externally by the clock line.
The output value is latched with the first falling edge at NRD. With every subsequent rising edge the output value is serially output to NWR in binary code, beginning with the MSB set by OUTSEL. The error bit is transmitted after the output value.

In this mode, pin SDA can be used as serial data input. The data read in here at the beginning of the data transmission is output after the error bit.

A cyclic read out can be achieved by linking NWR to SDA. A one is output after the error bit as a stop bit.

To store the output value for a new data transmission, an interval of at least 64 clock pulses must be maintained at the clock input.

Fig. 11: synchronous-serial data transmission.

3. Incremental mode

Here, every change of angle with respect to the set resolution is signaled as a change in output on track DO(AX) or D1(BX). The square-wave signals produced have a phase shift of plus or minus 90°, depending on the direction of rotation.

In addition, the input signals are compared to reference voltage VREF and output to pins D3(A4) and D4(B4). This corresponds to a resolution of four.

The zero signals, suitably prepared, are available at pins D2(ZX) and D5(Z4). A direction signal is also output to D6(ROT) and signals AX and BX are EX-OR-gated at D7(AXB).

Incremental mode can be emulated in parallel-absolute mode by reading address 4.

Resolution RES(4:0) and RES(6,5)

One period of the input signal is internally divided into eight segments. The following segments [45°..90°, 90°..135°, 135°..180° etc. to 360°] are mapped on the first segment [0°..45°]. The resulting output resolution thus amounts to 8 times that of the TAN D/A converter.

The converter resolution per segment can be set to all whole-number values between 17 and 32. Subresolutions result only if every nth subdivision is used. A further decrease is possible by effecting a right shift by n-bit of the output value.

The following table shows all possible settings and resulting resolutions. With equal values, settings with more favorable characteristics are shown in bold type.

Resolution		TAN D/A Converter Resolution (per segment)															
		32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
all n-th subdivisions used	1 "00"	**256** [1F]	**248** [1E]	**240** [1D]	**232** [1C]	**224** [1B]	**216** [1A]	**208** [19]	**200** [18]	**192** [17]	**184** [16]	**176** [15]	**168** [14]	**160** [13]	**152** [12]	**144** [11]	**136** [10]
	2 "00"	**128** [0F]		**120** [0E]		**112** [0D]		**104** [0C]		**96** [0B]		**88** [0A]		**80** [09]		**72** [08]	
	4 "00"	**64** [07]				**56** [06]				**48** [05]				**40** [04]			
	8 "00"	**32** [03]								**24** [02]							
	16 "00"	**16** [01]															
	32 "00"	**8** [00]															
right shift by n-bit	1 "01"	128 64 32 16 8 **4**	**124**	120 **60**	**116**	112 56 **28**	**108**	104 **52**	**100**	96 48 24 **12**	**92**	88 **44**	**84**	80 40 **20**	**76**	72 **36**	**68**
	2 "10"	64 32 16 8 4 **2**	**62**	60 **30**	**58**	56 28 **14**	**54**	52 **26**	**50**	48 24 12 **6**	**46**	44 **22**	**42**	40 20 **10**	**38**	36 **18**	**34**
	3 "11"	32 16 8 4 2 **1**	**31**	30 **15**	**29**	28 14 **7**	**27**	26 **13**	**25**	24 12 6 **3**	**23**	22 **11**	**21**	20 10 **5**	**19**	18 **9**	**17**

Fig. 12: programming the resolution: hexadecimal [1F] for RES(4:0), binary "00" for RES(6:5).

Hysteresis

If the maximum possible converter resolution is not used, hysteresis can be obtained from free resolution steps. In so doing, the resolution chosen determines the number of possible hysteresis settings.
The following are possible in compliance with the upper half of the table of resolution printed above:

HYS	Hysteresis given in % (resistive)																
	0	6.25	12.5	18.75	25	31.25	37.5	43.75	50	56.25	62.5	68.75	75	81.25	87.5	93.75	100
1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	30
2	20	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	30
4	20	-	-	-	-	-	-	-	28	-	-	-	-	-	-	-	30
8	20	-	-	-	24	-	-	-	28	-	-	-	2C	-	-	-	30
16	20	-	22	-	24	-	26	-	28	-	2A	-	2C	-	2E	-	30
32	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30

Fig. 13: resistive hysteresis.
'-' indicates unauthorized programming.

When setting high converter resolutions which use all resolution steps, to produce hysteresis the resolution of the converter is increased in an intermediate step by switching on a capacitive voltage divider.

Hysteresis can be set in intervals of 5% from 0..95% in conjunction with the output values given in the upper half of the above table of resolution (output values are without a right shift).

HYS	Hysteresis given in % (capacitive)																		
	0	5	10	15	20	25	30	35	40	45	50	55	60	65	70	75	80	85	90	95
	00	01	02	03	04	05	06	07	10	11	12	13	14	15	16	17	1C	1D	1E	1F

Fig. 14: capacitive hysteresis.

Programming the zero position

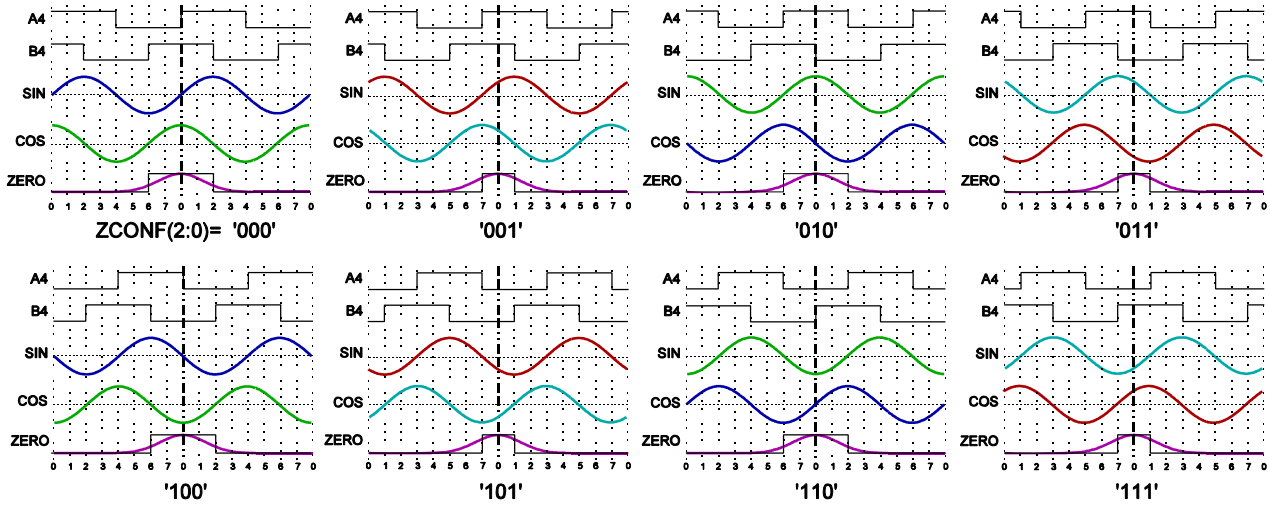


Fig. 15: programming the zero position.

A zero crossing can be set to multiples of 45° via register ZCONF(2:0) (Figure 15). If the value is an even number (ZCONF0= 0), then each of the zero pulses (ZX and Z4) are 1/2 period in width; otherwise their width is only 1/4 period.

Z4 remains ungated when ZCONF3= 1. ROT inverts the direction of rotation referred to the zero point set by ZCONF.

Converter adaptation to non-sinusoidal input signals

Adaptation is carried out in two steps and is performed separately for each of the eight segments.

In the **first step**, the offset and gain of the programmable gain amplifier (PGA) are set. The offset is corrected so that at the beginning of the first segment the signal at the PGA output is zero (sin0°= 0). The signal at the end of the first segment is then adapted to the cosine signal (sin45°= cos45°) with the gain setting. This adjustment should be tested by changing the direction of rotation and also by increasing the resolution.

In the **second step**, the transfer function in the TAN D/A converter is set to the value e_1/e_2 (e= input signal). In the basic setting (e_1 = sin, e_2 = cos), the PGA has a gain of one and an offset of zero. The tangent function is formed in the feedback loop.

This two-step adaptation procedure is performed accordingly in all segments. To activate converter adaptation, bit ADAP must be set and the entire storage area of the adaptation parameters written in one write cycle.

Restrictions: read access to the signal adaptation registers is not permitted. The internal address register must not point to the adaptation register during converter operation (addresses 16..127 are not permitted during operation).

The following diagram shows how the transfer function must be adapted in the feedback loop in the first segment should triangular signals be available at the input.

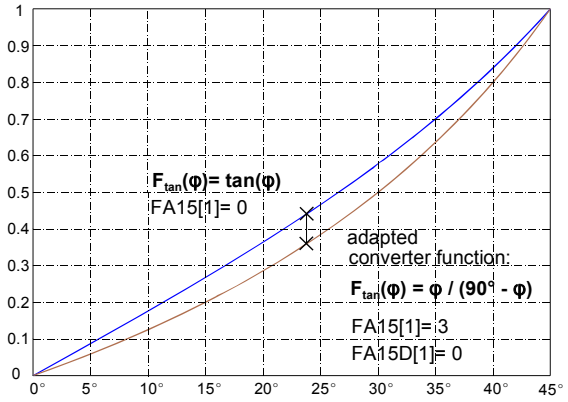


Fig. 16: transfer function in feedback loop (1st segment). The transfer function is more sharply curved for triangular input signals.

Period counter

The 24-bit position counter can be read via the COUNT registers (addresses 1..3). Write access is not possible, yet the counter can be reset by CLC.

Under normal circumstances (SIC= 0), the counter is increased or decreased by an overflow of the 8-bit interpolation register NG (address 0), according to the direction of run. Together with register NG, the output value is 4 bytes.

The counter stimulus is monitored by the separate fourfold edge evaluation feature and guarantees that the count functions perform properly even when input frequencies are excessively high, provided the phase does not step by more than 90°. If this is the case, error flag STEPINP is set.

CBZ must be set should the counter be reset by the zero pulse. Counting is enabled by pin MFP (SLCNTEN= 1) or alternatively by register COUNTEN (SLCNTEN= 0).

For measurement applications, the position counter input can also be switched to the interpolated output pulse (SIC= 1).

Interrupt and error messages

The occurrence of an interrupt or error is indicated in the interrupt and error status register at address 6.
Using registers LATINT and LATERR (address 11), the user can decide whether the information is to be displayed only as long as the interrupt or error persists or whether this information should be stored.

Pins MFP for interrupts (active high) and NER for errors (active low) are available for message outputs; authorization for signaling must be granted. Pin MFP must have output function (SLCNTEN= 0) to enable displaying.

RPM/Speed acquisition

The TACHO speed data register can be used to access a very simple RPM/speed log. The number of clock pulses between two consecutive output values is recorded here as a ones complement. The register is updated with each change in output value. No digital filtering is performed.

System clock

An internal oscillator is available as a clock generator. The frequency is determined by an external resistor.

In addition, register FREQ can be used to increase the clock rate tenfold. This is prudent with a high input frequency if merely the number of revolutions is to be determined.

Alternatively, the system clock can be fed in externally. The frequency should be between 0Hz and fmax and should not exceed the maximum low pulse duration (see characteristics), as otherwise the internal clock oscillator switches in.

PROGRAMMING

Register Configuration

Adr	read	write
0-3	Data Output Register	Target Position
4	Incremental Signals	-
5	Speed Data	-
6	Interrupt / Error Messages	-
7	Rotation Direction, Resolution Setting	Rotation Direction, Resolution Setting
8	Data Shift, PGA Bypass, Converter Hysteresis	Data Shift, PGA Bypass, Converter Hysteresis
9	Operation Mode, Counter Depth, Z Index Position	Operation Mode, Counter Depth, Z Index Position
10	Counter Settings	Counter Settings
11	Interrupt / Error Message Enable	Interrupt / Error Message Enable
12	Input Amplifier Compensation	Input Amplifier Compensation
13	Clock Frequency Select	Clock Frequency Select
16-23	-	Gain / Fullscale Calibration
24-31	-	Offset Adjustment
32-127	-	TAN Function Adaptation

Register Configuration

	Name								**Reset entry**
Adr	7	6	5	4	3	2	1	0	7:0
0	NG(7:0) resp. TPOS(7:0)								00
3-1	COUNT(23:0) resp. TPOS(31:8)								00 00 00
4	AXB	ROT	Z4	B4	A4	ZX	BX	AX	-
5	TACHO(7:0)								-
6				ERRV	STEPINP	MAXFREQ	POSCOMP	NGUPDT	-
7	ROT	RES(6:0)							1F
8	NGLJ	ADAP	HYS(5:0)						30 (B0)[1]
9	ACCMOD(1:0)		OUTSEL(1:0)		ZCONF(3:0)				00 (01)[2]
10				CLC	CBZ	COUNTEN	SLCNTEN	SIC	00
11		LATERR	LATINT	EN4	EN3	EN2	EN1	EN0	05
12	CZERO(3:0)				CSIN(3:0)				FF
13					FREQ	reserved[3]	reserved[3]	reserved[3]	08
16-23	Gain / Fullscale Calibration								FF
24-31	Offset Adjustment								FF
32-127	TAN Function Adaptation								FF

[1] Synchronous-serial mode
[2] Incremental mode
[3] Register programming to 1 is not permitted

Data Output Register Interpolation (read only)								**Adr: 0**
Bit Name	7 NG7	6 NG6	5 NG5	4 NG4	3 NG3	2 NG2	1 NG1	0 NG0
Period Count 1.Byte (write only)								**Adr: 1**
Bit Name	7 COUNT7	6 COUNT6	5 COUNT5	4 COUNT4	3 COUNT3	2 COUNT2	1 COUNT1	0 COUNT0
Period Count 2.Byte (write only)								**Adr: 2**
Bit Name	7 COUNT15	6 COUNT14	5 COUNT13	4 COUNT12	3 COUNT11	2 COUNT10	1 COUNT9	0 COUNT8
Period Count 3. Byte (write only)								**Adr: 3**
Bit Name	7 COUNT23	6 COUNT22	5 COUNT21	4 COUNT20	3 COUNT19	2 COUNT18	1 COUNT17	0 COUNT16

ADR 0, NG(7:0)	
ADR 3:1, COUNT(23:0)	

Target Position 1. Byte (write only)								**Adr: 0**
Bit Name	7 TPOS7	6 TPOS6	5 TPOS5	4 TPOS4	3 TPOS3	2 TPOS2	1 TPOS1	0 TPOS0
2. Byte (write only)								**Adr: 1**
Bit Name	7 TPOS15	6 TPOS14	5 TPOS13	4 TPOS12	3 TPOS11	2 TPOS10	1 TPOS9	0 TPOS8
3. Byte (write only)								**Adr: 2**
Bit Name	7 TPOS23	6 TPOS22	5 TPOS21	4 TPOS20	3 TPOS19	2 TPOS18	1 TPOS17	0 TPOS16
4. Byte (write only)								**Adr: 3**
Bit Name	7 TPOS31	6 TPOS30	5 TPOS29	4 TPOS28	3 TPOS27	2 TPOS26	1 TPOS25	0 TPOS24

ADR 3:0, TPOS(31:0)	

Incremental Signals (read)								**Adr: 4**
Bit Name	7 AXB	6 ROT	5 Z4	4 B4	3 A4	2 ZX	1 BX	0 AX

Bit 0, AX		Incremental track A (with the set resolution)
Bit 1, BX		Incremental track B (with the set resolution)
Bit 2, ZX		Zero signal (gated with AX, BX in accordance with ZCONF(2:0) definition)
Bit 3, A4		Incremental track A (with a resolution of 4)
Bit 4, B4		Incremental track B (with a resolution of 4)
Bit 5, Z4		Zero signal (gated with A4, B4 in accordance with ZCONF(3:0) definition)
Bit 6 ROT	0 1	Counterclockwise. Output value decreases. Sine is 90° ahead of cosine Clockwise. Output value increases. Sine is 90° behind cosine
Bit 7, AXB		Incremental tracks AX and BX EX-OR-gated

Speed Data (read only)								**Adr: 5**
Bit	7	6	5	4	3	2	1	0
Name	TACHO7	TACHO6	TACHO5	TACHO4	TACHO3	TACHO2	TACHO1	TACHO0

Adr 5, TACHO(7:0)	

Interrupt / Error Messages (active high, read only)								**Adr: 6**
Bit	7	6	5	4	3	2	1	0
Name				ERRV	STEPINP	MAXFREQ	POSCOMP	NGUPDT

This register is always set even if the necessary interrupts or errors are not enabled to be displayed.	
Data Output Change (Interrupt)	
Bit 0, NGUPDT	Output value has changed (message is set over a clock cycle)
Target Position Check (Interrupt)	
Bit 1, POSCOMP	Output value matches target position (depth of comparison in accordance with OUTSEL(1:0) definition)
Frequency Error 1 (Error)	
Bit 2, MAXFREQ	Input frequency is to high for the set resolution. COUNT(23:0) valid, AX/BX invalid (monitoring prudent in incremental mode)
Frequency Error 2 (Error)	
Bit 3, STEPINP	The input signal phase has turned 90°-270° during a clock cycle, i.e. A4 and B4 have changed simultaneously. COUNT(23:0) invalid (monitoring prudent in parallel-absolute mode)
Undervoltage (Error)	
Bit 4, ERRV	Supply voltage too low

Resolution Setting, Rotation Direction								**Adr: 7**
Bit	7	6	5	4	3	2	1	0
Name	ROT	RES6	RES5	RES4	RES3	RES2	RES1	RES0

Resolution Setting		
Bit 4..0 RES(4:0)	'00'h .. '1F'h	TAN D/A converter resolution per segment = 1 .. TAN D/A converter resolution per segment = 32
Bit 6,5 RES(6:5)	0 0 0 1 1 0 1 1	Resolution equals 8 times the TAN D/A converter resolution Output value shifted 1 bit to the right (resolution halved) Output value shifted 2 bits to the right Output value shifted 3 bits to the right
Rotation Direction		
Bit 7 ROT	0 1	Output value increases if cosine before sine (mathematically positive) Output value decreases if cosine before sine

Hysteresis, Data Shift, PGA Bypass								**Adr: 8**
Bit	7	6	5	4	3	2	1	0
Name	NGLJ	ADAP	HYS5	HYS4	HYS3	HYS2	HYS1	HYS0

Hysteresis		
Bit 5:0 HYS(5:0)	'00'h .. '3F'h	Hysteresis according to the tables on page 11
Data Shift		
Bit 6 ADAP	0 1	Programmable gain amplifier (PGA) deactivated Programmable gain amplifier (PGA) activated
PGA Bypass		
Bit 7 NGLJ	0 1	Output value is justified right Output value is shifted left (only practical in synchronous-serial mode for resolutions smaller than 136)

Z Index Position, Counter Depth, Operation Mode								**Adr: 9**
Bit	7	6	5	4	3	2	1	0
Name	ACCMOD1	ACCMOD0	OUTSEL1	OUTSEL0	ZCONF3	ZCONF2	ZCONF1	ZCONF0

Z Index Position				
Bit 2:0 ZCONF(2:0)	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	Zero crossing at 0° Zero crossing at 45° Zero crossing at 90° Zero crossing at 135° Zero crossing at 180° Zero crossing at 225° Zero crossing at 270° Zero crossing at 315°	(Sin = 0, COS = 1) (Sin = COS > 0) (Sin = 1, COS = 0) (Sin = -COS > 0) (Sin = 0, COS = -1) (Sin = COS < 0) (Sin = -1, COS = 0) (Sin = -COS < 0)	(ZX, Z4 both ½ cycle wide) (ZX,Z4 both ¼ cycle wide) (ZX,Z4 both ½ cycle wide) (ZX,Z4 both ¼ cycle wide) (ZX,Z4 both ½ cycle wide) (ZX,Z4 both ¼ cycle wide) (ZX,Z4 both ½ cycle wide) (ZX,Z4 both ¼ cycle wide)
		If the ZERO inputs do not receive a true zero signal from the sensor, different wiring is necessary to produce ZERO = 1 (via V(PZERO) > V(NZERO)).		
Bit 3 ZCONF3	0 1	Z4 gated with A4 and B4 (width of Z4 = ¼), Z4 gated with A4 or B4 (width of Z4 = ½) Z4 not gated		
Counter Depth				
Bit 5:4 OUTSEL(1:0)	0 0 0 1 1 0 1 1	Output value consists of NG(7:0) Output value consists of COUNT(7:0) & NG(7:0) Output value consists of COUNT(15:0) & NG(7:0) Output value consists of COUNT(23:0) & NG(7:0)		
		This setting affects target position evaluation and sets the MSB to synchronous-serial mode		
Operation Mode				
Bit 7:6 ACCMOD(1:0)	0 0 1 0 1 1 0 1	Parallel mode Synchronuous-serial mode Incremental mode not permitted		
		The access mode is determined when the configuration is loaded from the serial EEPROM and cannot be altered during operation. If no EEPROM is available, the access mode can be set via pins SDA and SCL.		

Position Counter Settings								**Adr: 10**
Bit Name	7	6	5	4 CLC	3 CBZ	2 COUNTEN	1 SLCNTEN	0 SIC

Input Select		
Bit 0 SIC	0 1	The position counter is increased/decreased with each zero crossing The position counter is increased/decreased with each interpolation step
Enable Select		
Bit 1 SLCNTEN	0 1	Count operation is enabled via the COUNTEN register; MFP is an output pin Count operation is enabled via pin MFP; MFP is an input pin
Enable		
Bit 2 COUNTEN	0 1	Position counter is stopped (with SLCNTEN = 0) Position counter enabled (with SLCNTEN = 0)
Reset Enable		
Bit 3 CBZ	0 1	Position counter is not reset with a zero pulse Position counter is reset with every zero pulse
Reset		
Bit 4 CLC	0 1	Position counter is not reset Position counter is reset

Interrupt / Error Message Enable (active high)								**Adr: 11**
Bit Name	7	6 LATERR	5 LATINT	4 EN4	3 EN3	2 EN2	1 EN1	0 EN0

Interrupts are shown active high at pin MFP if this is programmed as an output. Errors are shown active low at pin NER.		
Bit 0, EN0	0 1	Disabled NGUPDT enabled. Status following a reset (message to pin MFP)
Bit 1, EN1	0 1	Disabled POSCOMP enabled (message to pin MFP)
Bit 2, EN2	0 1	Disabled MAXFREQ enabled. Status following a reset (Message to pin NER)
Bit 3, EN3	0 1	Disabled STEPINP enabled (message to pin NER)
Bit 4, EN4	0 1	Disabled ERRV enabled (message to pin NER)
Bit 5, LATINT	0 1	Interrupts are only shown while the cause for the interrupt persists Interrupt status is saved (programming 1-0-1 resets the registers of address 6)
Bit 6, LATERR	0 1	Errors are only shown while the cause for the error persists Error status is saved (programming 1-0-1 resets the registers of address 6)

Input Amplifier Compensation								**Adr: 12**
Bit	7	6	5	4	3	2	1	0
Name	CZERO3	CZERO2	CZERO1	CZERO0	CSIN3	CSIN2	CSIN1	CSIN0

SIN, COS Inputs		
Bit 3:0 CSIN(3:0)	'0'h .. 'F'h	0.0pF 0.8pF / LSB 12.0pF
ZERO Input		
Bit 7:4 CZERO(3:0)	'0'h .. 'F'h	0.0pF 0.8pF / LSB 12.0pF

Clock Frequency Select								**Adr: 13**
Bit	7	6	5	4	3	2	1	0
Name					FREQ	reserved	reserved	reserved

Bit 3 FREQ	0 1	Clock frequency has increased ca. tenfold (only valid when no external clocking pulse is fed in) Clock frequency not multiplied
Bit 2:0 reserved	0	Registers must always be programmed to 0

PGA Gain (write only)								**Adr: 16-23 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	G7[i]	G6[i]	G5[i]	G4[i]	G3[i]	G2[i]	G1[i]	G0[i]

Bit 7:0 G(7:0)[i]	'00'h '01'h .. '7F'h 'FF'h .. '81'h '80'h	255/128 ≈ 1.992 ≈ 1.984 1/128 pro LSB ≙0.0078 128/128 = 1 255/255 = 1 ≈ 0.50592 1/255 pro LSB ≙0.00392 128/255 ≈ 0.502

PGA Offset (write only)								**Adr: 24-31 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	O7[i]	O6[i]	O5[i]	O4[i]	O3[i]	O2[i]	O1[i]	O0[i]

Bit 7:0 O(7:0)[i]	'00'h .. '7F'h 'FF'h .. '80'h	-127/384×A ≈ -0.33×A -1/384×A pro LSB -0/384×A = 0 0/384×A = 0 1/384×A pro LSB 127/384×A ≈ 0.33×A A = input signal amplitude

TAN Function Adaptation			**base 1-4** (write only)					**Adr: 32-39 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	FA4H[i]	FA4L[i]	FA3H[i]	FA3L[i]	FA2H[i]	FA2L[i]	FA1H[i]	FA1L[i]
				base 5-8 (write only)				**Adr: 40-47 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	FA8H[i]	FA8L[i]	FA7H[i]	FA7L[i]	FA6H[i]	FA6L[i]	FA5H[i]	FA5L[i]
				base 9-12 (write only)				**Adr: 48-55 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	FA12H[i]	FA12L[i]	FA11H[i]	FA11L[i]	FA10H[i]	FA10L[i]	FA9H[i]	FA9L[i]
				base 13-16 (write only)				**Adr: 56-63 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	FA16H[i]	FA16L[i]	FA15H[i]	FA15L[i]	FA14H[i]	FA14L[i]	FA13H[i]	FA13L[i]
				base 17-20 (write only)				**Adr: 64-71 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	FA20H[i]	FA20L[i]	FA19H[i]	FA19L[i]	FA18H[i]	FA18L[i]	FA17H[i]	FA17L[i]
				base 21-24 (write only)				**Adr: 72-79 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	FA24H[i]	FA24L[i]	FA23H[i]	FA23L[i]	FA22H[i]	FA22L[i]	FA21H[i]	FA21L[i]
				base 25-28 (write only)				**Adr: 80-87 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	FA28H[i]	FA28L[i]	FA27H[i]	FA27L[i]	FA26H[i]	FA26L[i]	FA25H[i]	FA25L[i]
				base 29-31 (write only)				**Adr: 88-95 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	K1[i]	K0[i]	FA31H[i]	FA31L[i]	FA30H[i]	FA30L[i]	FA29H[i]	FA29L[i]

FajH[i], FAjL[i]	0 0	No adaptation of function at base J
	1 0	Adaptation of function at base J with an intensity of 1
	0 1	Adaptation of function at base J with an intensity of 2
	1 1	Adaptation of function at base J with an intensity of 3, always in segment i
K1[i], K0[i]	1 1	Reserved; register must stay set at 1

TAN Function Adaptation				**base 1-8** (write only)				**Adr: 96-103 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	FA8D[i]	FA7D[i]	FA6D[i]	FA5D[i]	FA4D[i]	FA3D[i]	FA2D[i]	FA1D[i]
				base 9-16 (write only)				**Adr: 104-111 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	FA16D[i]	FA15D[i]	FA14D[i]	FA13D[i]	FA12D[i]	FA11D[i]	FA10D[i]	FA9D[i]
				base 17-24 (write only)				**Adr: 112-119 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name	FA24D[i]	FA23D[i]	FA22D[i]	FA21D[i]	FA20D[i]	FA19D[i]	FA18D[i]	FA17D[i]
				base 25-31 (write only)				**Adr: 120-127 (1.-8. Segment)**
Bit	7	6	5	4	3	2	1	0
Name		FA31D[i]	FA30D[i]	FA29D[i]	FA28D[i]	FA27D[i]	FA26D[i]	FA25D[i]

FajD[i]	0	Upward adaptation of function at base J
	1	Downward adaptation of function at base J

APPLICATIONS NFORMATION

Application notes for iC-NG and details on the demo board are available separately.

ORDERING INFORMATION

Type	Package	Order Designation
iC-NG	SO28	iC-NG SO28
iC-NG	SSOP28 5.3mm	iC-NG SSOP28
Evaluation board		iC-NG EVAL NGD

The evaluation board includes:
- board 100 mm x 160 mm
- interface cable for the serial interface
- 3.5" floppy disk containing the control program
- iC-NG data sheet
- description

Information on prices, delivery dates, possible deliveries of other packages etc. are available from:

iC-Haus GmbH
Am Kuemmerling 18
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