iC-MSB^{SAFETY}, iC-MSB2
SIN/COS SIGNAL CONDITIONER WITH 1Vpp DRIVER

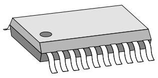
FEATURES

- PGA inputs to 500 kHz for differential and single-ended sensor signals
- Selectable adaptation to voltage or current signals
- Flexible pin assignment due to signal path multiplexers
- Sine/Cosine signal conditioning for offset, amplitude and phase
- Separate index signal conditioning
- Short-circuit-proof and reverse polarity tolerant output drivers (1 Vpp to 100 Ω)
- Stabilized output signal levels due to sensor control
- Signal and system monitoring with configurable alarm output
- Supply voltage monitoring with integrated switches for reversed-polarity-safe systems
- Excessive temperature protection with sensor calibration
- I^{2}C multimaster interface
- Supply from 4.3 to 5 V, operation within -25(-40) to +100 °C
- Suitable for *SAFETY* applications
- Verifyable chip release code
- Version **iC-MSB2** with output multiplexer (not for *SAFETY*)

APPLICATIONS

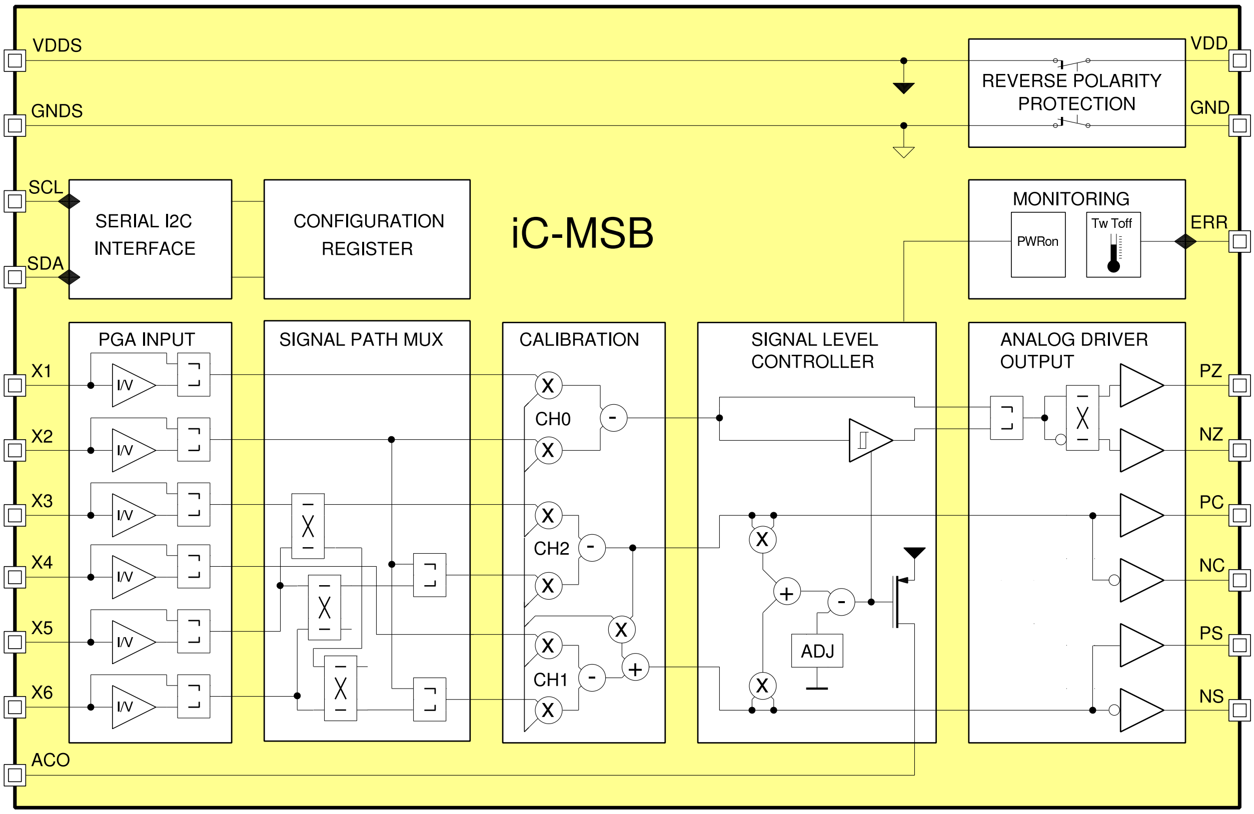
- Programmable sensor interface for optical and magnetic position sensors
- Linear gauges and incremental encoders
- Linear scales

PACKAGES



TSSOP20, TSSOP20-TP

BLOCK DIAGRAM



DESCRIPTION

iC-MSB is a signal conditioner with line drivers for sine/cosine sensors which are used to determine positions in linear and angular encoders, for example.

Programmable instrumentation amplifiers with selectable gain levels permit differential or referenced input signals; at the same time the modes of operation differentiate between high and low input impedance. This adaptation of the iC to voltage or current signals enables MR sensor bridges or photosensors to be directly connected up to the device.

The integrated signal conditioning unit allows signal amplitudes and offset voltages to be calibrated accurately and also any phase error between the sine and cosine signals to be corrected. Separate zero signal conditioning settings can be made for the gain and offset; data is then output either as an analog or a differential square-wave signal (low/high level analogous to the sine/cosine amplitude).

For the stabilization of the sine and cosine output signal levels a control signal is generated from the conditioned and calibrated input signals which can power the transmitting LED of optical systems via the integrated 50 mA driver stage (output ACO). If MR sensors are connected this driver stage also powers the measuring bridges.

By tracking the sensor energy supply any signal variations and temperature and aging effects can be compensated for and the set signal amplitude maintained with absolute accuracy. At the same time the control circuitry monitors both whether the sensor is functioning correctly and whether it is properly connected; signal loss due to wire breakage, short circuiting, dirt or aging, for example, is recognized when control thresholds are reached and indicated at alarm output ERR.

iC-MSB is protected against a reversed power supply voltage; the integrated voltage switch for loads of up to 20 mA extends this protection to cover the overall system. The analog output drivers are directly cable-compatible and tolerant to false wiring; if supply voltage is connected up to these pins, the device is not destroyed.

The device configuration and calibration parameters are CRC protected and stored in an external EEPROM; they are loaded automatically via the I2C interface once the supply voltage has been connected up.

A safety-technical analysis of iC-MSB on device level with the inclusion of layout and internal/external circuitry has been carried out together with the BGIA, St. Augustin. The result proved iC-MSB’s capability for safety oriented applications with Siemens Sinumerik Controls.

CONTENTS

PACKAGES 4

ABSOLUTE MAXIMUM RATINGS 5

THERMAL DATA 5

ELECTRICAL CHARACTERISTICS 6

PROGRAMMING 10

SERIAL CONFIGURATION INTERFACE (EEPROM) 13
- Example of CRC Calculation Routine 13
- EEPROM Selection 13
- I^{2}C Slave Mode (ENSL = 1) 14

BIAS SOURCE AND TEMPERATURE SENSOR CALIBRATION 15

OPERATING MODES 16
- Calibration Op. Modes 16
- Special Device Test Functions 16
- Signal Filter 16

TEST MODE 17

INPUT CONFIGURATIONS 18
- Input Configurations 18

SIGNAL PATH MULTIPLEXING: iC-MSB*SAFETY* 18

EXTENDED SIGNAL PATH MULTIPLEXING: iC-MSB2 *(not for safety applications)* 19

SIGNAL CONDITIONING CH1, CH2 21
- Gain Settings CH1, CH2 21
- Offset Calibration CH1, CH2 22
- Phase Correction CH1 vs. CH2 22

SIGNAL CONDITIONING CH0 23
- Gain Settings CH0 23
- Offset Calibration CH0 23

SIGNAL LEVEL CONTROL and SIGNAL MONITORING 24

ERROR MONITORING AND ALARM OUTPUT 25
- Error Protocol 25
- I/O pin ERR 25

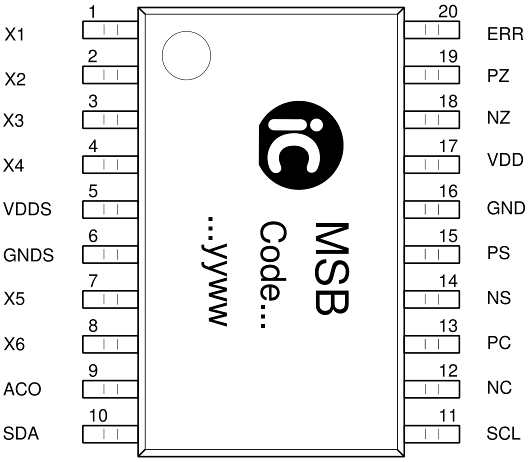
TEMPERATURE MONITORING 26

REVERSE POLARITY PROTECTION 26

APPLICATION HINTS 27
- Connecting MR sensor bridges for safety-related applications 27
- PLC Operation 27

PACKAGES

PIN CONFIGURATION TSSOP20, TSSOP20-TP



PIN FUNCTIONS

No.	Name	Function
1	X1	Signal Input 1 (Index +)
2	X2	Signal Input 2 (Index -)
3	X3	Signal Input 3
4	X4	Signal Inout 4
5	VDDS	Switched Supply Output (reverse polarity proof, load to 20 mA max.)
6	GNDS	Switched Ground (reverse polarity proof)
7	X5	Signal Input 5
8	X6	Signal Input 6
9	ACO	Signal Level Controller, high-side current source output
10	SDA	Serial Configuration Interface, data line
11	SCL	Serial Configuration Interface, clock line
12	NC	Neg. Cosine Output
13	PC	Pos. Cosine Output
14	NS	Neg. Sine Output
15	PS	Pos. Sine Output
16	GND	Ground
17	VDD	+4.5 to +5.5 V Supply Voltage
18	NZ	Neg. Index Output
19	PZ	Pos. Index Output
20	ERR	Error Signal (In/Out), Test Mode Trigger Input

To improve heat dissipation the *thermal pad* of the TSSOP20-TP package (bottom side) should be joined to an extended copper area which must have GNDS potential.

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	**Symbol**	**Parameter**	**Conditions**	**Min.**	**Max.**	**Unit**
G001	V()	Voltage at VDD, GND, PC, NC, PS, NS, PZ, NZ, ACO		-6	6	V
G002	V()	Voltage at ERR		-6	8	V
G003	V()	Pin-To-Pin Voltage between VDD, GND, PC, NC, PS, NS, PZ, NZ, ACO, ERR			6	V
G004	V()	Voltage at X1...X6, SCL, SDA		-0.3	VDDS + 0.3	V
G005	I(VDD)	Current in VDD		-100	100	mA
G006	I()	Current in VDDS, GNDS		-50	50	mA
G007	I()	Current in X1...X6, SCL, SDA, ERR, PC, NC, PS, NS, PZ, NZ		-20	20	mA
G008	I(ACO)	Current in ACO		-100	20	mA
G009	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G010	Ptot	Permissible Power Dissipation	TSSOP20 TSSOP20-TP		300 400	mW mW
G011	Tj	Junction Temperature		-40	150	°C
G012	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Item No.	**Symbol**	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
T01	Ta	Operating Ambient Temperature Range	iC-MSB TSSOP20, iC-MSB2 TSSOP20 iC-MSB TSSOP20-TP	-25 -40		100 115	°C °C
T02	Rthja	Thermal Resistance Chip to Ambient	TSSOP20 surface mounted to PCB according to JEDEC 51		80		K/W
T03	Rthja	Thermal Resistance Chip to Ambient	TSSOP20-TP surface mounted to PCB according to JEDEC 51		35		K/W

All voltages are referenced to Pin GNDS unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage	Load current I(VDDS) < -10 mA	4.3 4.5		5.5 5.5	V V
002	I(VDD)	Supply Current in VDD	Tj = 27 °C, no load		25	50	mA
003	I(VDDS)	Permissible Load Current VDDS		-20		0	mA
004	Vcz()hi	Clamp Voltage hi at all pins				11	V
005	Vc()hi	Clamp Voltage hi at inputs SCL, SDA	Vc()hi = V() – V(VDDS), I() = 1 mA	0.4		1.5	V
006	Vc()hi	Clamp Voltage hi at inputs X1...X6	Vc()hi = V() – V(VDDS), I() = 4 mA	0.3		1.2	V
007	Vc()lo	Clamp Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
Signal Conditioning, Inputs X3...X6							
101	Vin()sig	Permissible Input Voltage Range	RIN12(3:0) = 0x01 RIN12(3:0) = 0x09	0.75 0		VDDS – 1.5 VDDS	V V
102	Iin()sig	Permissible Input Current Range	RIN12(0) = 0, BIAS12 = 0 RIN12(0) = 0, BIAS12 = 1	-300 10		-10 300	µA µA
103	Iin()	Input Current	RIN12(3:0) = 0x01	-10		10	µA
104	Rin()	Input Resistance vs. VREFin	Tj = 27 °C; RIN12(3:0) = 0x09 RIN12(3:0) = 0x00 RIN12(3:0) = 0x02 RIN12(3:0) = 0x04 RIN12(3:0) = 0x06	16 1.1 1.6 2.2 3.2	20 1.6 2.3 3.2 4.6	24 2.1 3.0 4.2 6.0	kΩ kΩ kΩ kΩ kΩ
105	TCRin()	Temperature Coefficient Rin			0.15		%/K
106	VREFin12	Reference Voltage	RIN12(0) = 0, BIAS12 = 1 RIN12(0) = 0, BIAS12 = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
107	G12	Selectable Gain Factors	RIN12(3:0) = 0x01, GR12 and GF12 = 0x0 RIN12(3:0) = 0x01, GR12 and GF12 = max. RIN12(3:0) = 0x09, GR12 and GF12 = 0x0 RIN12(3:0) = 0x09, GR12 and GF12 = max.		2 100 0.5 25		
108	∆Gdiff	Differential Gain Accuracy	calibration range 11 bit	-0.5		0.5	LSB
109	∆Gabs	Absolute Gain Accuracy	calibration range 11 bit, guaranteed monotony	-1		1	LSB
110	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(CHPx) - V(CHNx), RUIN12(3) = 0 RUIN12(3) = 1	10 40		500 2000	mVpp mVpp
111	Vin()os	Input Offset Voltage	refered to side of input	0	20		µV
112	VOScal	Offset Calibration Range	referenced to the selected source (VOS12); ORx = 00 ORx = 01 ORx = 10 ORx = 11		±100 ±200 ±600 ±1200		%V() %V() %V() %V()
113	∆VOSdiff	Differential Linearity Error of Offset Correction	calibration range 11 bit	-0.5		0.5	LSB
114	∆VOSint	Integral Linearity Error of Offset Correction	calibration range 11 bit	-1		1	LSB
115	PHIkorr	Phase Error Calibration Range	CH1 versus CH2		±10.4		°
116	∆PHIdiff	Differential Linearity Error of Phase Calibration	calibration range 10 bit	-0.5		0.5	LSB
117	∆PHIint	Integral Linearity Error of Phase Calibration	calibration range 10 bit	-1		1	LSB
119	fin()max	Permissible Input Frequency		500			kHz
120	fhc()	Input Amplifier Cut-off Frequency (-3dB)		250			kHz

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Signal Conditioning, Inputs X1, X2							
201	Vin()sig	Permissible Input Voltage Range	RIN0(3:0) = 0x01 RIN0(3:0) = 0x09	0.75 0		VDDS – 1.5 VDDS	V V
202	Iin()sig	Permissible Input Current Range	RIN0(0) = 0, BIAS0 = 0 RIN0(0) = 0, BIAS0 = 1	-300 10		-10 300	µA µA
203	Iin()	Input Current	RIN0(3:0) = 0x01	-10		10	µA
204	Vout(X2)	Output Voltage at X2	BIASEX = 10, I(X2) = 0, referenced to VREFin12	95	100	105	%
205	Vin(X2)	Permissible Input Voltage at X2	BIASEX = 11	0.5		VDDS – 2	V
206	Rin(X2)	Input Resistance at X2	BIASEX = 11, RIN0(3:0) = 0x01, RIN12(3:0) = 0x01	20	27	30	kΩ
207	Rin()	Input Resistance vs. VREFin	Tj = 27 °C; RIN0(3:0) = 0x09 RIN0(3:0) = 0x00 RIN0(3:0) = 0x02 RIN0(3:0) = 0x04 RIN0(3:0) = 0x06	 16 1.1 1.6 2.2 3.2	 20 1.6 2.3 3.2 4.6	 24 2.1 3.0 4.2 6.0	 kΩ kΩ kΩ kΩ kΩ
208	TCRin()	Temperature Coefficient Rin			0.15		%/K
209	VREFin0	Reference Voltage	RIN0(0) = 0, BIAS0 = 1 RIN0(0) = 0, BIAS0 = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
210	G0	Selectable Gain Factors	RIN0(3:0) = 0x01, GR0 and GF0 = 0x0 RIN0(3:0) = 0x01, GR0 and GF0 = max. RIN0(3:0) = 0x09, GR0 and GF0 = 0x0 RIN0(3:0) = 0x09, GR0 and GF0 = max		2 100 0.5 25		
211	ΔGdiff	Differential Gain Accuracy	calibration range 5 bit	-0.5		0.5	LSB
212	ΔGabs	Absolute Gain Accuracy	calibration range 5 bit, guaranteed monotony	-1		1	LSB
213	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(CHP0) - V(CHN0), RIN0(3:0) = 0x01 RIN0(3:0) = 0x09	 10 40		 500 2000	 mVpp mVpp
214	Vin()os	Input Offset Voltage	referred to side of input	0	75		µV
215	VOScal	Offset Calibration Range	referenced to the selected source (REFVOS); OR0 = 00 OR0 = 01 OR0 = 10 OR0 = 11		 ±100 ±200 ±600 ±1200		 %V() %V() %V() %V()
216	ΔVOSdiff	Differential Linearity Error of Offset Correction	calibration range 6 bit	-0.5		0.5	LSB
217	ΔVOSint	Integral Linearity Error of Offset Correction	calibration range 6 bit	-1		1	LSB
Signal Filter							
301	fg	Cut-off Frequency				4000	kHz
302	phi	Phase Shift	fin 500 kHz for sine/cosine			10	°
Index Pulse Comparator Output PZ, NZ							
401	Vpk()	Output Amplitude With Sensor Tracking via ACO	EAZ = 1, ADJ(4:0) = 0x19	225	250	275	mV
402	SR()	Output Slew Rate	EAZ = 1		1		V/µs
Line Driver Outputs PS, NS, PC, NC, PZ, NZ							
501	Vpk()max	Permissible Output Amplitude	VDD = 4.5 V, DC level = VDD / 2, RL = 50 Ω vs. VDD / 2			300	mV
502	Vpk()	Output Amplitude With Sensor Tracking via ACO	ADJ (8:0) = 0x19	225	250	275	mV
503	fg	Cut-off Frequency	CL = 250 pF	500			kHz
504	Vos	Offset Voltage			±200		µV
505	Isc()	Short-circuit Current	pin shorten to VDD or GND	10	30	50	mA
506	Ilk()	Tristate Leakage Current	tristate or reversed supply	-1		1	µA

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Signal Level Controller ACO							
601	Vs()hi	Saturation Voltage hi at ACO vs. VDD	Vs() = VDD - V(); ADJ(8:0) = 0x11F, I() = -5 mA ADJ(8:0) = 0x13F, I() = -10 mA ADJ(8:0) = 0x15F, I() = -25 mA ADJ(8:0) = 0x17F, I() = -50 mA			 1 1 1 1	 V V V V
602	Isc()hi	Short-circuit Current hi in ACO	V() = 0 ... VDD - 1 V; ADJ(8:0) = 0x11F ADJ(8:0) = 0x13F ADJ(8:0) = 0x15F ADJ(8:0) = 0x17F	 -10 -20 -50 -100		 -5 -10 -25 -50	 mA mA mA mA
603	tr()	Current Rise Time in ACO	I(ACO): 0 → 90 % setpoint		1		ms
604	tset()	Current Settling Time in ACO	Square control active, I(ACO): 50 → 100 % setpoint		400		µs
605	It()min	Control Range Monitoring 1: lower limit	referenced to range ADJ(6:5)		3		%Isc
606	It()max	Control Range Monitoring 2: upper limit	referenced to range ADJ(6:5)		90		%Isc
607	Vt()min	Signal Level Monitoring 1: lower limit	referenced to Vscq()		40		%Vpp
608	Vt()max	Signal Level Monitoring 2: upper limit	referenced to Vscq()		130		%Vpp
Test Current ERR							
701	I(ERR)	Permissible Test Current	test mode activated	0		1	mA
Bias Current Source and Reference Voltages							
801	IBN()	Bias Current Source	MODE(3:0) = 0x01, I(NC) vs. VDDS	180	200	220	µA
802	VPAH	Reference Voltage VPAH	referenced to GND	45	50	55	%VDD
803	V05	Reference Voltage V05		450	500	550	mV
804	V025	Reference Voltage V025			50		%V05
Power-Down-Reset							
901	VDDon	Turn-on Threshold (power-on release)	increasing voltage at VDD vs. GND	3.7	4	4.3	V
902	VDDoff	Turn-off Threshold (power-down reset)	decreasing voltage at VDD vs. GND	3.2	3.5	3.8	V
903	VDDhys	Threshold Hysteresis	VDDhys = VDDon − VDDoff	0.3			V
Clock Oscillator							
A01	fclk()	Internal Clock Frequency	MODE(3:0) = 0x0A, fclk(NS)	120	160	200	kHz
Error Signal Input/Output, Pin ERR							
B01	Vs()lo	Saturation Voltage lo	vs. GND, I() = 4 mA			0.4	V
B02	Isc()	Short-circuit Current lo	vs. GND; V(ERR) ≤ VDD V(ERR) > VTMon	4 2			mA mA
B03	Vt()hi	Input Threshold Voltage hi	vs. GND			2	V
B04	Vt()lo	Input Threshold Voltage lo	vs. GND	0.8			V
B05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi − Vt()lo	300	500		mV
B06	Ipu()	Input Pull-up Current	V() = 0...VDD − 1 V, EPU = 1	-400	-300	-200	µA
B07	Rpu()	Input Pull-Up Resistor	EPU = 0		500		kΩ
B08	Vpu()	Pull-up Voltage	Vpu() = VDD - V(), I() = -5 µA, EPU = 1			0.4	V
B09	VTMon	Test Mode Activation Threshold	increasing voltage at ERR			VDD + 1.5	V
B10	VTMoff	Test Mode Disabling Threshold	decreasing voltage at ERR	VDD + 0.5			V
B11	VTMhys	Test Mode Hysteresis	VTMhys = VTMon − VTMoff	0.15	0.3		V
B12	Ilk()	Leakage Current	tristate or reversed supply voltage	-1	-10	-50	µA

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...125 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Switch and Reverse Polarity Protection VDDS, GNDS							
C01	Vs()	Saturation Voltage VDDS vs. VDD	Vs(VDDS) = VDD − V(VDDS)				
			I(VDDS) = -10 mA...0 mA			150	mV
			I(VDDS) = -20 mA...-10 mA			250	mV
C02	Vs()	Saturation Voltage GNDS vs. GND	Vs(GNDS) = V(GNDS) − GND				
			I(GNDS) = 0 mA...10 mA			150	mV
			I(GNDS) = 10 mA...20 mA			250	mV
Serial Configuration Interface SCL, SDA							
D01	Vs()lo	Saturation Voltage lo	I() = 4 mA			400	mV
D02	Isc()	Short-circuit Current lo		4		80	mA
D03	Vt()hi	Input Threshold Voltage hi				2	V
D04	Vt()lo	Input Threshold Voltage lo		0.8			V
D05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi − Vt()lo	300	500		mV
D06	Ipu()	Input Pull-up Current	V() = 0...VDDS − 1 V	-600	-300	-60	µA
D07	Vpu()	Input Pull-up Voltage	Vpu() = VDDS − V(), I() = -5 µA			0.4	V
D08	fclk(SCL)	Clock Frequency at SCL	ENFAST = 0	60	80	100	kHz
			ENFAST = 1	240	320	400	kHz
D09	tbusy()cfg	Duration of Startup Configuration	IBN not calibated, EEPROM access without read failure, time to outputs operational;				
			ENFAST = 0		40	55	ms
			ENFAST = 1		25	35	ms
D10	tbusy()err	End Of I2C Communication; Time Until I2C Slave Is Enabled	IBN not calibrated;				
			V(SDA) = 0 V		4	12	ms
			V(SCL) = 0 V or arbitration lost		indef.		ms
			no EEPROM		45	135	ms
			CRC ERROR		95	285	ms
D11	td()	Start Of Master Activity On I2C Protocol Error	SCL without clock signal: V(SCL) = constant;				
			IBN not calibrated	25	80	240	µs
			IBN calibrated to 200 µA	64	80	120	µs
D12	td()i2c	Delay for I2C-Slave-Mode Enable	no EEPROM, V(SDA) = 0 V		4	6.2	ms
Temperature Monitoring							
E01	VTs	Temperature Sensor Voltage	VTs() = VDDS − V(PS), Tj = 27 °C, Calibration Mode 3, no load	600	650	700	mV
E02	TCs	Temp. Co. of Temperature Sensor Voltage			-1.8		mV/K
E03	VTth	Temperature Warning Activation Threshold	VTth() = VDDS − V(NS), Tj = 27 °C, Calibration Mode 3, no load;				
			CFGTA(3:0) = 0x00	260	310	360	mV
			CFGTA(3:0) = 0x0F	470	550	630	mV
E04	TCth	Temp. Co. Temperature Warning Activation Threshold			0.06		%/K
E05	Thys	Temperature Warning Hysteresis		4	12	20	°C
E06	ΔT	Relative Shutdown Temperature	ΔT = Toff − Twarn	4	12	20	°C

PROGRAMMING

Register Map . . . . Page 11

Configuration Interface . . . . Page 13

ENFAST:	I^2C Fast Mode Enable
ENSL:	I^2C Slave Mode Enable
DEVID:	Device ID of EEPROM providing the chip configuration data (e.g. 0x50)
CHKSUM:	CRC of chip configuration data (address range 0x00 to 0x1E)
CHPREL:	Chip Release
NTRI:	Tristate Function and Op. Mode Change

Calibration . . . . Page 15

CFGIBN:	Bias Calibration
CFGTA:	Temperature Sensor Calibration

Operation Modes . . . . Page 16

MODE:	Operation Mode
ENF:	Signal Filtering

Test Mode . . . . Seite 17

TMODE:	Test Mode Functions
TMEM:	Test Mode Memory Selection

Input Configuration and Signal Path Multiplexer . . . . Page 18

INMODE:	Diff./Single-Ended Input Mode
RIN12:	I/V Mode and Input Resistance CH1, CH2
BIAS12:	Reference Voltage CH1, CH2
RIN0:	I/V Mode and Input Resistance CH0
BIAS0:	Reference Voltage CH0
MUXIN:	Input-To-Channel Assignment: X3...X6 to CH1, CH2
INVZ:	Index Signal Inversion
EAZ:	Index Comparator Enable
MUXOUT:	Output Multiplexer (iC-MSB2 only)
BIASEX:	Input Reference Selection
BYP	Input-to-output Feedthrough

Signal Conditioning CH1, CH2 (X3...X6) . . Page 21

GR12:	Gain Range CH1, CH2 (coarse)
GF1:	Gain Factor CH1 (fine)
GF2:	Gain Factor CH2 (fine)
VOS12:	Offset Reference Source CH1, CH2
VDC1:	Intermediate Voltage CH1
VDC2:	Intermediate Voltage CH2
OR1:	Offset Range CH1 (coarse)
OF1:	Offset Factor CH1 (fine)
OR2:	Offset Range CH2 (coarse)
OF2:	Offset Factor CH2 (fine)
PH12:	Phase Correction CH1 vs. CH2

Signal Conditioning CH0 (X1, X2) . . . . Page 23

GR0:	Gain Range CH0 (coarse)
GF0:	Gain Factor CH0 (fine)
VOS0:	Offset Reference Source CH0
OR0:	Offset Range CH0 (coarse)
OF0:	Offset Factor CH0 (fine)

Signal Level Controller . . . . Page 24

ADJ:	Setup of ACO Output Function

Error Monitoring and Alarm Output . . . . . . Page 25

EMTD:	Minimal Alarm Indication Time
EPH:	Alarm Input/Output Logic
EPU:	Alarm Output Pull-Up Enable
EMASKA:	Error Mask For Alarm Indication (pin ERR)
EMASKE:	Error Mask For Protocol (EEPROM)
EMASKO:	Error Mask For Driver Shutdown
ERR1:	Error Protocol: First Error
ERR2:	Error Protocol: Last Error
ERR3:	Error Protocol: History
PDMODE:	Driver Activation After Cycling Power

OVERVIEW

Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Interface								
0x00	ENFAST	DEVID(6:0)						
Calibration								
0x01	CFGIBN(3:0)				CFGTA(3:0)			
Operation Modes								
0x02	NTRI	1	0	–	MODE(3:0)			
Input Configuration and Signal Path Multiplexer: iC-MSB								
0x03	EAZ	0	0	0	INVZ	INMODE	MUXIN(1:0)	
Input Configuration and Signal Path Multiplexer: iC-MSB2								
0x03	EAZ	MUXOUT(2:0)			INVZ	INMODE	MUXIN(1:0)	
Signal Conditioning CH1, CH2								
0x04	GF2(4:0)					GR12(2:0)		
0x05	GF1(7:0)							
0x06	VDC1(4:0)					GF1(10:8)		
0x07	VDC2(2:0)			VDC1(9:5)				
0x08	OR1(0)	VDC2(9:3)						
0x09	OF1(6:0)							OR1(1)
0x0A	OF2(1:0)		OR2(1:0)		OF1(10:7)			
0x0B	OF2(9:2)							
0x0C	PH12(6:0)							OF2(10)
0x0D	BIASEX(1:0)		BYP	1	1	PH12(9:7)		
0x0E	ENF	BIAS12	VOS12(1:0)		RIN12(3:0)			
Signal Level Controller								
0x0F	ADJ(0)	–	0	1	0	0	0	0
0x10	ADJ(8:1)							
Signal Conditioning CH0								
0x11	GF0(4:0)					GR0(2:0)		
0x12	OF0(5:0)						OR0(1:0)	
0x13	0	BIAS0	VOS0(1:0)		RIN0(3:0)			
Error Monitoring and Alarm Output								
0x14	–	EMASKA(6:0)						
0x15	TMODE(1:0)		EMTD(2:0)			EPH	–	–
0x16	–	EMASKO(6:0)						
0x17	EMASKE(3:0)				ENSL	EPU	–	–
0x18	TMEM	PDMODE	–	–	–	EMASKE(6:4)		
0x19.. 0x1A	not defined							
0x1B.. 0x1E	OEM Data							
Check Sum / Chip Release								
0x1F	EEPROM: CHKSUM(7:0) / ROM: CHPREL(7:0)							

OVERVIEW								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Error Register								
0x20	–	ERR1(6:0)						
0x21	ERR2(5:0)						–	–
0x22	ERR3(3:0)				–	–	–	ERR2(6)
0x23	–	–	–	–	–	ERR3(6:4)		

Table 4: Register layout

SERIAL CONFIGURATION INTERFACE (EEPROM)

The serial configuration interface consists of the two pins SCL and SDA and enables read and write access to an EEPROM with I^{2}C interface. The readout speed can be adjusted using register bit ENFAST.

ENFAST	Adr 0x00, bit 7
Code	Function
0	Regular clock rate, f(SCL) approx. 80 kHz
1	High clock rate, f(SCL) approx. 320 kHz
Notes	For in-circuit programming bus lines SCL and SDA require pull-up resistors. For line capacitances to 170 pF, adequate values are: 4.7 kΩ with clock frequency 80 kHz 2 kΩ with clock frequency 320 kHz The pull-up resistors may not be less than 1.5 kΩ. To separate the signals a ground line between SCL and SDA is recommended. iC-MSB requires a supply voltage during EEPROM programming (5 V to VDD).

Table 5: Config. Interface Clock Frequency

Once the supply has been switched on (power down reset) the iC-MSB outputs are high impedance (tristate) until a valid configuration is read out from the EEPROM using device ID 0x50.

Bit errors in the 0x00 to 0x1E memory section are pinpointed by the CRC deposited in register CHKSUM(7:0) (address 0x1F; the CRC polynomial used is "1 0001 1101").

Should no valid configuration data being available (incorrect CRC value or EEPROM missing), the readin process is repeated; the system aborts following a fourth faulty attempt and iC-MSB switches to I^{2}C slave mode.

For devices loading valid configuration data from the EEPROM, the register bit ENSL decides for enabling the I^{2}C slave function.

ENSL	Adr 0x17, bit 3
Code	Function
0	Normal operation
1	I^{2}C Slave Mode Enable (Device ID 0x55)

Table 6: Config. Interface Mode

The device ID for the EEPROM can be entered in register DEVID(6:0) (address 0x00), from which iC-MSB will take its configuration after exiting test mode (see page 17). The DEVID(6:0) stored therein is then accepted.

Example of CRC Calculation Routine

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x11D;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 1; // start value !!!
for (iReg = 0; iReg<31; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

EEPROM Selection

The following minimal requirements must be fulfilled:

- Operation from 3.3 to 5 V, I^{2}C interface
- Minimal 512 bit, 64x8 (address range used is 0x00 to 0x3F)
- Support of *Page Write* with *Pages* of at least 4 bytes. Otherwise error events can not be saved to the EEPROM (EMASKE(9:0) = 0x000).
- Device ID 0x50 "1010 000", no occupation of 0x55 (A2...A0 = 0). Otherwise iC-MSB is not accessible in I^{2}C slave mode via 0x55 (ENSL = 0).

Device recommendation: Atmel AT24C01B, 128x8

I^{2}C Slave Mode (ENSL = 1)

In this mode iC-MSB behaves like an I^{2}C slave with the device ID 0x55 and the configuration interface permits write and read accesses to iC-MSB's internal registers.

For chip release verification purposes an identification value is stored under ROM address 0x1F; a write access to this address is not permitted.

CHPREL	Adr 0x1F, bit 7:0 (ROM)
Code	Chip Release
0x00	Not available
0x04	iC-MSB $^{\text{SAFETY}}$ v4
0x05	iC-MSB $^{\text{SAFETY}}$ v5
0x25	iC-MSB2 v5

Table 7: Chip Release

NTRI	Adr 0x02, bit 7
Code	Function
0	Output drivers disabled
1	Setting the operating mode, output drivers active
Notes	NTRI is evaluated only during I^{2}C slave mode.

Table 8: Tristate Function And Op. Mode Change

Register	Read access in I^{2}C slave mode (ENSL = 1)
Address	Content
0x00-0x18	Configuration: register addresses 0x00-0x18
0x19-0x1A	Not available
0x1B-0x1E	OEM data: register addresses 0x1B-0x1E
0x1F	Chip release (ROM)
0x20-0x23	Configuration: register addresses 0x20-0x23
0x24-0x37	Not available
0x38	Configuration: register address 0x18
0x39-0x3A	Not available
0x3B-0x3E	OEM data: register addresses 0x1B-0x1E
0x3F	Chip release (ROM)
0x40-0x43	Current error memory
0x44-0x7F	Not available

Table 9: RAM Read Access

Register	Write access in I^{2}C slave mode (ENSL = 1)
Address	Access and conditions
0x00	Changes possible, no restrictions
0x01	Changes possible (wrong entries for CFGIBN can limit functions)
0x02	Bit 7 = 0 (NTRI): changes to bits (6:0) permitted A change of operating mode follows only on writing Bit 7 = 1 (NTRI); when doing so changes to bits (6:0) are not permitted.
0x03-0x16	Changes possible, no restrictions
0x17	Bit 3 = 1 (ENSL): changes to bits (7:4) and (2:0) permitted
0x18	Changes possible, no restrictions
0x19-0x1A	Not available
0x1B-0x1E	Changes possible, no restrictions
others	No changes permitted

Table 10: RAM Write Access

BIAS SOURCE AND TEMPERATURE SENSOR CALIBRATION

Bias Source Calibration

The calibration of the bias current source in operation mode *Calibration 1* (Tab. 13) is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. SCL clock frequency). For setup purposes the IBN value is measured using a 10 kΩ resistor by pin VDDS connected to pin NC. The setpoint is 200 µA which is equivalent to a measurement voltage of 2 V.

CFGIBN	Adr 0x01, bit 7:4		
Code k	$IBN \sim \frac{31}{39-k}$	Code k	$IBN \sim \frac{31}{39-k}$
0x0	79 %	0x8	100 %
0x1	81 %	0x9	103 %
0x2	84 %	0xA	107 %
0x3	86 %	0xB	111 %
0x4	88 %	0xC	115 %
0x5	91 %	0xD	119 %
0x6	94 %	0xE	124 %
0x7	97 %	0xF	129 %

Table 11: Bias Current Source Calibration

Temperature Sensor

The temperature monitor is calibrated in operating mode *Calibration Mode 3*.

To set the required warning temperature T_2 the temperature sensor voltage VTs at which the warning is generated is first determined. To this end a voltage ramp from VDDS towards GNDS is applied to pin PS until pin ERR triggers an error message (for EMASKA = 0x20 and EMTD = 0x00).

Example: VTs(T_1) is ca. 650 mV, measured from VDDS versus PS, with T_1 = 25 °C;

The necessary activation threshold voltage VTh(T_1) is then calculated. The required warning temperature T_2, temperature coefficients TCs and TCth (see Electrical Characteristics, Section E) and measurement value VTs(T_1) are entered into this calculation:

$$VTth(T_1) = \frac{VTs(T_1) + TCs \cdot (T_2 - T_1)}{1 + TCth \cdot (T_2 - T_1)}$$

Example: For $T_2 = T_1 + 100\,K$, VTth(T_1) must be programmed to 443 mV.

Activation threshold voltage VTth(T_1) is provided for a high impedance measurement (10 MΩ) at output pin NS (measurement versus VDDS) and must be set by programming CFGTA(3:0) to the calculated value.

Example: Altering VTth(T_1) from 310 mV (measured with CFGTA(3:0)= 0x0) to 443 mV is equivalent to 143 %, the closest value for CFGTA is 0x9;

CFGTA	Adr 0x01, bit 3:0		
Code k	$VTth \sim \frac{65+3k}{65}$	Code k	$VTth \sim \frac{65+3k}{65}$
0x0	100 %	0x8	140 %
0x1	105 %	0x9	145 %
0x2	110 %	0xA	150 %
0x3	115 %	0xB	155 %
0x4	120 %	0xC	160 %
0x5	125 %	0xD	165 %
0x6	130 %	0xE	170 %
0x7	135 %	0xF	175 %
Notes	With CFGTA = 0xF Toff is 80 °C typ., with CFGTA = 0x0 Toff is 155 °C typ.		

Table 12: Calibration of Temperature Monitoring

OPERATING MODES

In order to calibrate iC-MSB, compensate for the input signals and test iC-MSB the mode of operation must be changed. The output function changes according to the various operating modes; the line drivers and protection against reverse polarity facility are only active in normal mode.

MODE(3:0)		Addr. 0x02; bit 3:0						
BYP		Addr. 0x0D; bit 5						
Code	Operating Mode	Pin PS	Pin NS	Pin PC	Pin NC	Pin PZ	Pin NZ	Pin ERR
0x00	Normal operation	PS	NS	PC	NC	PZ	NZ	ERR
0x01	Calibration 1	TANA0(2)	VREFI0	VREFI12	IBN	PZI	NZI	ERR
0x02	Calibration 2	PCH1	NCH1	PCH2	NCH2	VDC1	VDC2	—
0x03	iC-Haus Test 1	VPAH	VPD	—	CGUCK	IPF	V05	IERR
0x04	iC-Haus Test 2	PS_out	NS_out	PC_out	NC_out	PZ_out	NZ_out	IERR
0x05	iC-Haus Test 3	PS_out	NS_out	PC_out	NC_out	PZ_out	NZ_out	ERR
0x06	iC-Haus Test 4, BYP = 0 iC-Haus Test 4, BYP = 1	TANA12(0) X4	TANA12(1) X6	TANA12(2) X3	TANA12(3) X5	TANA12(4) X1	TANA12(5) X2	IERR
0x07	Calibration 3	VTs	VTth	—	—	—	—	ERR
0x08	Saturation low	SCL, SDA and ERR low						
0x09	—	—	—	—	—	—	—	—
0x0A	iC-Haus Test 5	TP	CLK6	—	—	—	—	—
0x0B	—	—	—	—	—	—	—	—
0x0C	—	—	—	—	—	—	—	—
0x0D	—	—	—	—	—	—	—	—
0x0E	IDDQ-Test	All PU/PD resistors, oscillator and supply voltage deactivated						
0x0F	—	—	—	—	—	—	—	—

Table 13: Selection of Operating Modes

Calibration Op. Modes

In *Calibration Mode 1* the user can measure the BIAS current (IBN), input amplifier reference potential VREFI and the analog signals from channel 0 following signal conditioning (PCH0 and NCH0).

In *Calibration Mode 2* the conditioned signals from channels 1 and 2 are output (PCH1, NCH1, PCH2 and NCH2). In addition the intermediate potentials of the compensating circuits are also available for CH1 (VDC1) and CH2 (VDC2).

In *Calibration Mode 3* the internal temperature monitoring signals are provided.

Special Device Test Functions

IDDQ-Test, *Saturation Low*, *Saturation High*, and *Test 1 to 5* are test modes for iC-Haus device tests. With an activated bypass (BYP = 1), mode *iC-Haus Test 4* permits the direct feedthrough of X1 - X6 input signals to the output pins; in this instance the output impedance is high-ohmic. Furthermore, if the input voltage divider is selected (by RINx = 1- -1), it reduces the signal amplitudes to approx. 7/8.

Signal Filter

iC-MSB has a noise limiting signal filter to filter the conditioned analog signals. This can be activated using ENF.

ENF	Adr 0x0E, bit 7
Code	Function
0	Noise limiter deactivated
1	Noise limiter activated

Table 14: Signal Filtering

TEST MODE

iC-MSB switches to test mode when a voltage greater than VTMon is applied to pin ERR (precondition: TMODE(0) = 1). In response iC-MSB transmits its configuration settings as current-modulated data using error signal I/O pin ERR either directly from the RAM (for TMEM = 1) or after re-reading the EEPROM (for TMEM = 0).

TMEM	Adr 0x18, bit 7
0	EEPROM contents
1	iC-MSB RAM contents

Table 15: Test Mode Memory Selection

Should the voltage at the ERR pin fall below VTMoff test mode is terminated and data transmission aborted.

The clock rate for the data output is determined by ENFAST. Two clock rates can be selected: 780 ns for ENFAST = 1 or 3.125 µs for ENFAST = 0 (see Electrical Characteristics, D08, for clock frequency and tolerances).

Data is output in Manchester code via two clock pulses per bit. To this end the lowside current source switches between a Z state (OFF = 0 mA) and an L state (ON = 2 mA).

The bit information lies in the direction of the current source switch:
Zero bit: change of state Z → L (OFF to ON)
One bit: Change of state L → Z (ON to OFF)

Transmission consists of a start bit (a one bit), 8 data bits and a pause interval in Z state (the timing is identical with an EEPROM access via the I^{2}C interface).

Example: byte value = 1000 1010
Transmission including the start bit: 1 1000 1010
In Manchester code: LZ LZZL ZLZL LZZL LZZL

Decoding of the data stream:

ZZZZZZ LZ LZ ZL ZL ZL LZ ZL LZ ZL ZZZZZZ
Pause 1 1 0 0 0 1 0 1 0 Pause

When test mode is quit with TMODE > 0, then iC-MSB again reads out its configuration from the EEPROM, accessible at the device ID filed to DEVID(6:0) of adr 0x00. In TMODE = 0x00 the EEPROM is read completely; in all other cases only the address range 0x00 to 0x21 is read to keep the configuration time for device testing short. When test mode is quit with TMODE = 0x00 iC-MSB continues operation without any interruption.

TMODE	Adr 0x15, bit 7:6	
Code	Function during test mode	Function following test mode
00	Normal operation	Normal operation
01	TMEM = 0: Transmission of EEPROM data, address range 0x1B-0x7F TMEM = 1: Transmission of RAM data, address range 0x3B-0x43	Repeated read out of EEPROM
10	Normal operation	Repeated read out of EEPROM
11	Transmission of EEPROM data, address range 0x0-0x7F	Repeated read out of EEPROM

Table 16: Test Mode Functions

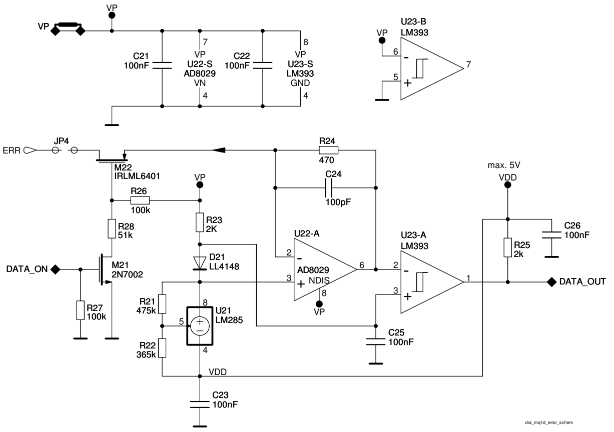


Figure 1: Example circuit for the decoding and conversion of the current-modulated signals to logic levels.

INPUT CONFIGURATIONS

Input Configurations

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Referenced input signals can be processed as an option; in this mode input X2 acts as a reference.

INMODE	Adr 0x03, bit 2
Code	Function
0	Differential input signals
1	Single-ended input signals *
Note	* Input X2 is reference for all inputs.

Table 17: Input Signal Mode

Both current and voltage signals can be processed as input signals, selected using RIN12(0) and RIN0(0).

In I Mode an input resistor Rin() becomes active at each input pin, converting the current signal into a voltage signal. Input resistance Rin() consists of a pad wiring resistor and resistor Rui() which is linked to the adjustable bias voltage source VREFin(). The following table shows the possible selections, with Rin() giving the typical resulting input resistance (see Electrical Characteristics for tolerances). The input resistor should be set in such a way that intermediate potentials VDC1 and VDC2 lie between 125 mV and 250 mV (verifiable in *Calibration Mode 2*).

In V Mode an optional voltage divider can be selected which reduces unacceptably large input amplitudes to ca. 25%. The circuitry is equivalent to the resistor chain in I Mode; the pad wiring resistor is considerably larger here, however.

RIN12 **RIN0**	Adr 0x0E, bit 3:0 Adr 0x13, bit 3:0		
Code	Nominal Rin()	Intern Rui()	I/V Mode
–000	1.7 kΩ	1.6 kΩ	current input
–010	2.5 kΩ	2.3 kΩ	current input
–100	3.5 kΩ	3.2 kΩ	current input
–110	4.9 kΩ	4.6 kΩ	current input
1—1	20 kΩ	5 kΩ	voltage input
0—1	high impedance	1 MΩ	voltage input

Table 18: I/V Mode and Input Resistance

BIAS12 **BIAS0**	Adr 0x0E, bit 6 Adr 0x13, bit 6	
Code	VREFin()	Type of sensor
0	2.5 V)	Lowside sink current (I Mode)
1	1.5 V)	Highside current source (I Mode)

Table 19: Reference Voltage

BIASEX	Adr 0x0D, bit 7:6	
Code	VREFin()	Signal at X2
0-	internal	Neg. Zero Signal (Index -), input
10	internal *	Ref. Voltage VREFin12, output
11	external *	Ref. Voltage VREFin, input
Note	*) The voltage at X2 is reference for all inputs.	

Table 20: Input Reference Selection

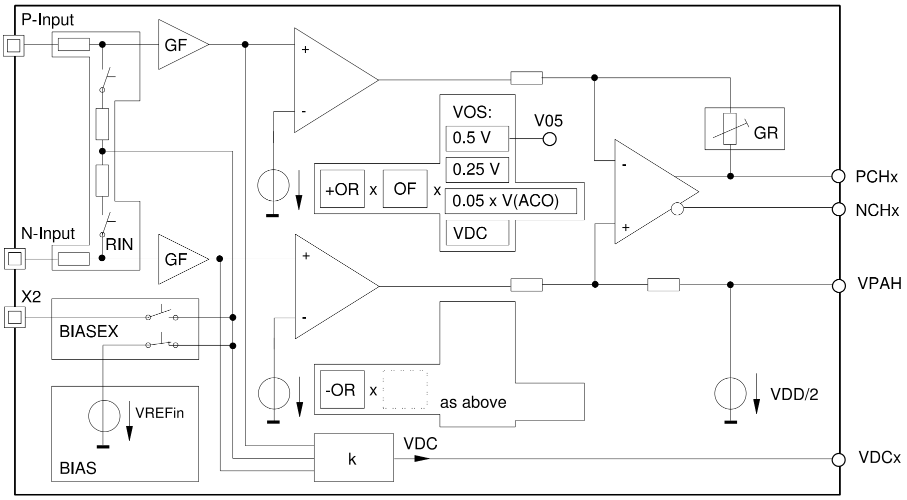


Figure 2: Input instrumentation amplifier and signal conditioning

SIGNAL PATH MULTIPLEXING: iC-MSB*SAFETY*

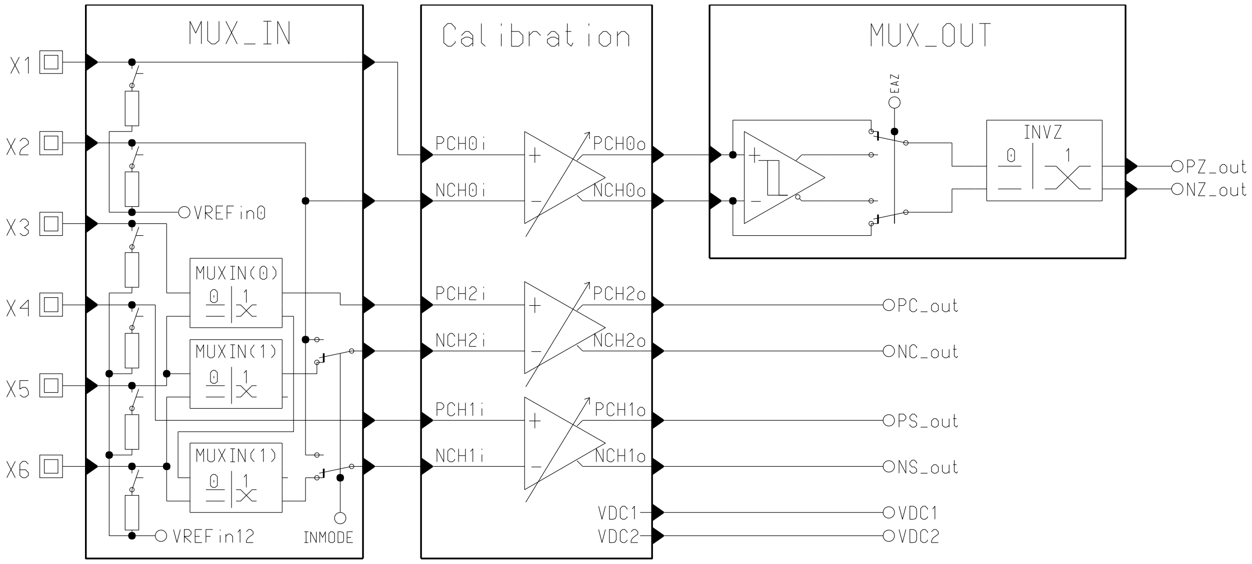


Figure 3: Multiplexer Schematics

The signals for index channel CH0 are connected up to pins X1 and X2. Pins X3 to X6 are allocated to internal channels CH1 and CH2 via MUXIN. INMODE can be activated for referenced input signals; this then selects X2 as the reference input. For output purposes INVZ allows the index signal phase to be inverted.

MUXIN	0x03, bit 1:0			
Code	PCH1i	NCH1i	PCH2i	NCH2i
00	X4	X6	X3	X5
01	X4	X6	X5	X5
10	X4	X5	X3	X6
11	X4	X3	X5	X6

Table 21: Input Multiplexer for INMODE = 0

MUXIN	0x03, bit 1:0			
Code	PCH1i	NCH1i	PCH2i	NCH2i
-0	X4	X2	X3	X2
-1	X4	X2	X5	X2

Table 22: Input Multiplexer for INMODE = 1

EAZ	Adr 0x03, bit 7
Code	Function
0	Comparator bypass
1	Comparator active

Table 23: Index Output

EAZ permits the activation of an analog comparator for index channel CH0.

INVZ	Adr 0x03, bit 3	
Code	PZ_out	NZ_out
0	PCH0o	NCH0o
1	NCH0o	PCH0o

Table 24: Index Signal Inversion

EXTENDED SIGNAL PATH MULTIPLEXING: iC-MSB2 *(not for safety applications)*

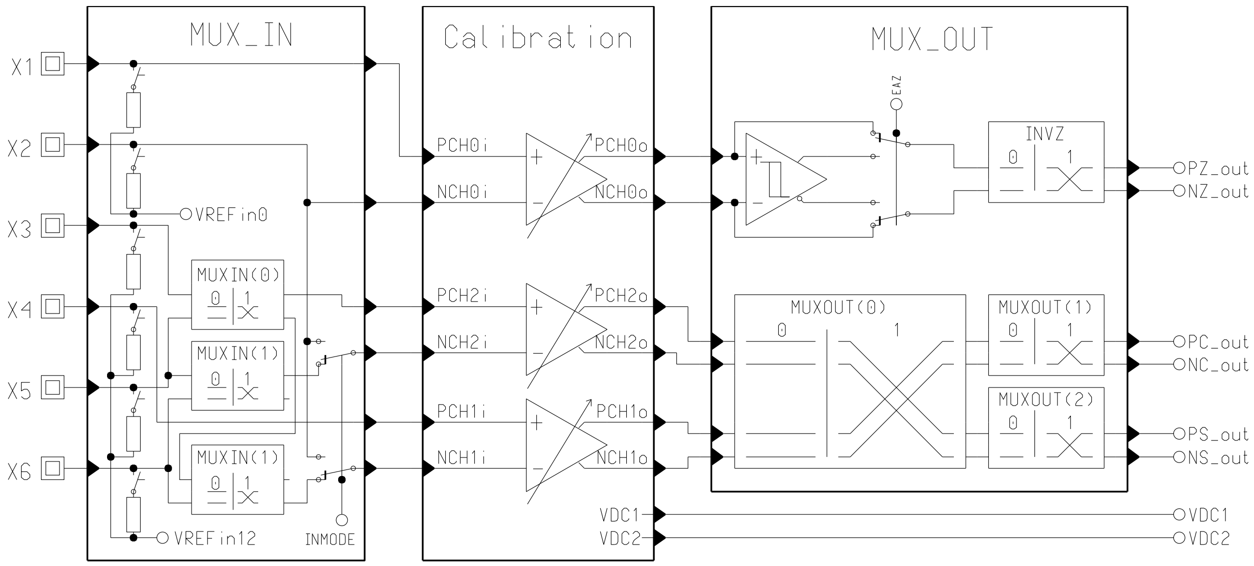


Figure 4: Multiplexer Schematics

The signals for index channel CH0 are connected up to pins X1 and X2. Pins X3 to X6 are allocated to internal channels CH1 and CH2 via MUXIN. INMODE can be activated for referenced input signals; this then selects X2 as the reference input. For output purposes INVZ allows the index signal phase to be inverted.

MUXIN	0x03, bit 1:0			
Code	PCH1i	NCH1i	PCH2i	NCH2i
00	X4	X6	X3	X5
01	X4	X6	X5	X5
10	X4	X5	X3	X6
11	X4	X3	X5	X6

Table 25: Input Multiplexer for INMODE = 0

MUXIN	0x03, bit 1:0			
Code	PCH1i	NCH1i	PCH2i	NCH2i
-0	X4	X2	X3	X2
-1	X4	X2	X5	X2

Table 26: Input Multiplexer for INMODE = 1

INVZ	Adr 0x03, bit 3	
Code	PZ_out	NZ_out
0	PCH0o	NCH0o
1	NCH0o	PCH0o

Table 27: Index Signal Inversion

EAZ permits the activation of an analog comparator for index channel CH0.

EAZ	Adr 0x03, bit 7
Code	Function
0	Comparator bypass
1	Comparator active

Table 28: Index Output

MUXOUT	Adr 0x03, bit 6:4			
Code	PS_Out	NS_Out	PC_Out	NC_Out
000	Channel 1		Channel 2	
010	Channel 1		Channel 2 inverted	
100	Channel 1 inverted		Channel 2	
110	Channel 1 inverted		Channel 2 inverted	
001	Channel 2		Channel 1	
011	Channel 2		Channel 1 inverted	
101	Channel 2 inverted		Channel 1	
111	Channel 2 inverted		Channel 1 inverted	

Table 29: Output Multiplexer

SIGNAL CONDITIONING CH1, CH2

The voltage signals necessary for the conditioning of channels 1 and 2 can be measured in operation mode *Calibration 2*.

Gain Settings CH1, CH2

The gain is set in four stages:

1. The sensor supply tracking is shut down and the constant current source for the ACO output set to a suitable output current (register ADJ; current value close to the later operating point).

2. The coarse gain is selected so that the differential signal amplitudes of ca. 1 Vpp are produced (signal Px vs. Nx, see Figure below).

3. Using fine gain factor GF2 the CH2 signal amplitude is then adjusted to 1 Vpp.

4. The CH1 signal amplitude can then be adjusted to the CH2 signal amplitude via fine gain factor GF1.

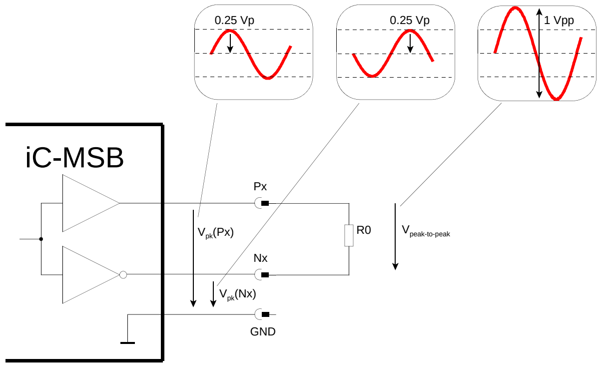


Figure 5: Definition of 1 Vpp signal. Termination R0 must be high-ohmic during all *Test* and *Calibration* modes.

GR12	Adr 0x04, bit 2:0	
Code	Range with RIN12=0x9	Range with RIN12≠0x9
0x0	0.5	2.0
0x1	1.0	4.1
0x2	1.3	5.3
0x3	1.7	6.7
0x4	2.2	8.7
0x5	2.6	10.5
0x6	3.3	13.2
0x7	4.0	16.0

Table 30: Gain Range CH1, CH2

GF2	Adr 0x04, bit 7:3
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25^{\frac{GF2}{31}}$
0x1F	6.25

Table 31: Fine Gain Factor CH2

GF1	Adr 0x06, bit 2:0, Adr 0x05, bit 7:0
Code	Factor
0x000	1.0
0x001	1.0009
...	$6.25^{\frac{GF1}{1984}}$
0x7FF	6.6245

Table 32: Fine Gain Factor CH1

Offset Calibration CH1, CH2

In order to calibrate the offset the reference source must first be selected using VOS12. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which provide stable, self-regulating signals.

So that photosensors can be operated in optical encoders iC-MSB tracks changes in offset voltages via the signal-dependent source VDC when used in conjunction with the controlled sensor current source for LED supply (pin ACO). The VDC potential automatically tracks higher DC photocurrents. To this end intermediate potentials VDC1 and VDC2 must be adjusted to a minimal AC ripple using the selectable k factor (this calibration must be repeated when the gain setting is altered).

The feedback of pin voltage V(ACO) fulfills the same task as source VDC when MR bridge sensors are supplied by the controlled power supply output. In this instance the VDC intermediate voltages do not need adjusting.

VOS12	Adr 0x0E, bit 5:4
Code	Type of source
0x0	0.05 · V(ACO)
0x1	0.5 V
0x2	0.25 V
0x3	VDC (ie. VDC1, VDC2)

Table 33: Offset Reference Source CH1, CH2

VDC1 **VDC2**	Adr 0x07, bit 4:0; Adr 0x06, bit 7:3 Adr 0x08, bit 6:0; Adr 0x07, bit 7:5
Code	$VDC = k \cdot VPi + (1 - k) \cdot VNi$
0x000	$k = 0.33$
0x001	$k = 0.33032$
...	$k = 0.33 + MP2 \cdot 0.00032$
0x3FF	$k = 0.66$

Table 34: Intermediate Voltages CH1, CH2

The calibration range for the CH1/CH2 offset is dependent on the selected VOS12 source and is set using OR1 and OR2. Both sine and cosine signals are then calibrated using factors OF1 and OF2. The calibration target is reached when the DC fraction of the differential signals PCHx versus NCHx is zero.

OR1 **OR2**	Adr 0x09, bit 0; Adr 0x08, bit 7 Adr 0x0A, bit 5:4
Code	Range
0x0	x1
0x1	x2
0x2	x6
0x3	x12

Table 35: Offset Range CH1, CH2

OF1 **OF2**	Adr 0xA, bit 3:0; Adr 0x9, bit 7:1 Adr 0xC, bit 0; Adr 0xB, bit 7:0; Adr 0xA, bit 7:6		
Code	Factor	Code	Factor
0x000	0	0x400	0
0x001	0.00098	0x401	−0.00098
...	$0.00098 \cdot OFx$	...	$-0.00098 \cdot OFx$
0x3FF	1	0x7FF	−1

Table 36: Offset Factors CH1, CH2

Phase Correction CH1 vs. CH2

The phase shift between CH1 and CH2 can be adjusted using parameter PH12. Following phase calibration other calibration parameters may have to be adjusted again (those as amplitude compensation, intermediate potentials and offset voltages).

PH12	Adr 0xD, bit 2:0; Adr 0xC, bit 7:1		
Code	Correction angle	Code	Correction angle
0x000	+0	0x200	−0
0x001	+0.0204	0x201	−0.0204
...	$+0.0204 \cdot PH12$	...	$-0.0204 \cdot PH12$
0x1FF	+10.42	0x3FF	−10.42

Table 37: Phase Correction CH1 vs. CH2

SIGNAL CONDITIONING CH0

The voltage signals needed to calibrate channel 0 are available in *Calibration Mode 1*.

Gain Settings CH0

Parallel to the conditioning process for the CH1 and CH2 signals the CH0 gain is set in the following stages:

1. The sensor supply tracking unit is shut down and the constant current source for the ACO output set to the same output current as in the compensation of CH1 and CH2 (register ADJ; current value close to the later operating point).

2. The coarse gain is selected so that a differential signal amplitude of ca. 1 Vpp is produced internally (signal PCHx versus NCHx).

3. GF0 then permits fine gain adjustment to 1 Vpp.

GR0	Adr 0x11, bit 2:0	
Code	Range with RIN0=0x9	Range with RIN0≠0x9
0x0	0.5	2.0
0x1	1.0	4.1
0x2	1.3	5.3
0x3	1.7	6.7
0x4	2.2	8.7
0x5	2.6	10.5
0x6	3.3	13.2
0x7	4.0	16.0

Table 38: Gain Range CH0

GF0	Adr 0x11, bit 7:3
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25^{\frac{GFZ}{31}}$
0x1F	6.25

Table 39: Fine Gain Factor CH0

Offset Calibration CH0

To calibrate the offset the source of supply must first be selected using VOS0 (see Offset Calibration CH1 and CH2 for further information). For the CH0 path the dependent source VDC is identical to source VDC1.

VOSZ	Adr 0x13, bit 5:4
Code	Source
0x0	0.05 · V(ACO)
0x1	0.5 V
0x2	0.25 V
0x3	VDC (ie. VDC1)

Table 40: Offset Reference Source CH0

OR0	Adr 0x12, bit 1:0
Code	Range
0x0	x1
0x1	x2
0x2	x6
0x3	x12

Table 41: Offser Range CH0

OF0	Adr 0x12, bit 7:2		
Code	Factor	Code	Factor
0x00	0	0x20	0
0x01	0.0322	0x21	-0.0322
...	0.0322 · OFZ	...	-0.0322 · OFZ
0x1F	1	0x3F	-1

Table 42: Offset Factor CH0

SIGNAL LEVEL CONTROL and SIGNAL MONITORING

Via the controlled sensor current source (pin ACO) iC-MSB can keep the output signals for the ensuing sine/digital converter constant regardless of temperature and aging effects by tracking the sensor supply.

Both the controller operating range and input signal amplitude for the controller are monitored and can be enabled for error messaging. A constant current source can be selected for the ACO output when setting the signal conditioning; the current range for the highside current source is adjusted using ADJ(6:5).

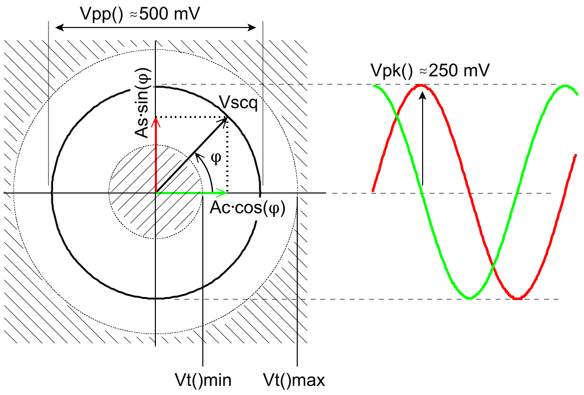


Figure 6: Signal level monitoring with square control (example for ADJ(8:0) = 0x19; see Elec. Char. Nos.607 and 608 regarding Vt()min resp. Vt()max)

ADJ (8:7)	Adr 0x10, bit 7:6
Code	Function
00	Sine/cosine square control
01	Sum control
10	Constant current source
11	Not permitted (device test only)

Table 43: Controller Operating Modes

ADJ (6:5)	Adr 0x10, bit 5:4
Code	Function
00	5 mA - Range
01	10 mA - Range
10	25 mA - Range
11	50 mA - Range

Table 44: ACO Output Current Range (applies for control modes and constant current source)

ADJ (4:0)	Adr 0x10, bit 3:0; Adr 0x0F, bit 7
Code	**Square control** ADJ(8:7) = 00
0x00	Vpp() ca. 300 mV (60 %)
0x01	Vpp() ca. 305 mV (61 %)
...	Vpp() $\approx 300\,mV \frac{77}{77-(1.25*Code)}$
0x19	Vpp() ca. 500 mV (98 %)
...	...
0x1F	Vpp() ca. 600 mV (120 %)

Table 45: Vpp Setpoint For Square Control

ADJ (4:0)	Adr 0x10, bit 3:0; Adr 0x0F, bit 7
Code	**Sum control** ADJ(8:7) = 01
0x00	VDC1 + VDC2 ca. 245 mV
0x01	VDC1 + VDC2 ca. 249 mV
...	VDC1 + VDC2 $\approx 245mV \frac{77}{77-(1.25*Code)}$
0x1F	VDC1 + VDC2 ca. 490 mV

Table 46: DC Setpoint For Sum Control

ADJ (4:0)	Adr 0x10, bit 3:0; Adr 0x0F, bit 7
Code	**Constant current source** ADJ(8:7) = 10
0x00	I(ACO) ca. 3.125% Isc(ACO)
0x01	I(ACO) ca. 6.25% Isc(ACO)
...	I(ACO) $\approx$ 3.125% $* (Code + 1) * Isc(ACO)$
0x1F	I(ACO) ca. 100% Isc(ACO)
Notes	See Elec. Char. No. 602 for Isc(ACO)

Table 47: I(ACO) With Constant Current Source

ERROR MONITORING AND ALARM OUTPUT

The following table gives the errors which can both be recognized by iC-MSB and enabled either for messaging, output shutdown or protocol in the EEPROM. Mask EMASKA stipulates that errors should be signaled at pin ERR, mask EMASKO determines whether the line driver outputs are to be shutdown or not (with PDMODE setting a renewed power-on) and mask EMASKE governs the storage of error events in the EEPROM.

EMASKA	Adr 0x14, bit 6:0
EMASKO	Adr 0x16, bit 6:0
EMASKE	Adr 0x18, bit 2:0; Adr 0x17, bit 7:4
Bit	Error Event
6	Configuration error*: SDA or SCL pin error, no Ack signal from EEPROM or invalid check sum
5	Excessive temperature warning
4	External system error
3	Level controller out of range (max. limit)
2	Level controller out of range (min. limit)
1	Signal clipping (excessive input level)
0	Loss of signal (poor input level or CH1/CH2 phase out of range)
Note	*) The line drivers remain high impedance (tristate) when cycling power.

Table 48: Error Event Masks

Error Protocol

Out of the errors pinpointed by EMASKE both the first (ERR1) and last error (ERR2) which occur after the iC-MSB is turned on are stored in the EEPROM. The EEPROM also has a memory area in which all occurring errors can be stored (ERR3). Only the fact that an error has occurred can be recorded, with no information as to the time and frequency of that error given. The EEPROM memory can be used to statistically evaluate the causes of system failure, for example.

ERR1	Adr 0x20, bit 6:0
ERR2	Adr 0x22, bit 0; Adr 0x21, bit 7:2
ERR3	Adr 0x23, bit 2:0; Adr 0x22, bit 7:4
Bit	Error Event
9:0	Assignation according to EMASKE
Code	Function
0	No event
1	Registered error event

Table 49: Error Protocol

I/O pin ERR

Pin ERR is operated by a current-limited open drain output driver and has an internal pull-up which can be shutdown. The ERR pin also acts as an input for external system error messaging and for switching iC-MSB to test mode for which a voltage of greater than VTMon must be applied. Interpretation of external system error messaging and the phase length of the message output can be set using EPH; the minimum signaling duration for internal errors is adjusted using EMTD(2:0).

EPU	Adr 0x17, bit 2
Code	Function
0	without internal pull-up at ERR
1	internal pull-up at ERR active

Table 50: Alarm Output Pull-up Enable

PDMODE	Adr 0x18, bit 6
Code	Function
0	Line driver active when no error persists
1	Line driver active after power-on

Table 51: Driver Activation

EPH	Adr 0x15, bit 2	
Code	ERR pin function	Ext. error message
0	with error low, otherwise Z	with error low, otherwise pull-up active
1	with error Z, otherwise low	with error pull-up active, otherwise low

Table 52: Alarm Input/Output Logic

EMTD	Adr 0x15, bit 5:3		
Code	Indication Time	Code	Indication Time
0x0	0 ms	0x4	50 ms
0x1	12.5 ms	0x5	62.5 ms
0x2	25 ms	0x6	75 ms
0x3	37.5 ms	0x7	87.5 ms

Table 53: Minimum Alarm Indication Time

TEMPERATURE MONITORING

iC-MSB has an integrated temperature monitor. If the temperature threshold is exceeded an excessive temperature message is generated which is processed in the temperature monitor block. The warning threshold can be signaled at pin ERR or used to shut down the line drivers. If temperature $Toff = Twarn + \Delta T$ is exceeded the line drivers are shut down independent of EMASKO(6:0).

REVERSE POLARITY PROTECTION

The line drivers in iC-MSB are protected against reverse polarity and short-circuiting. A defective device cable or one wrongly connected cause damage neither to iC-MSB nor to the components protected against reverse polarity by VDDS and GNDS. The following pins are also reverse polarity protected: PC, NC, PS, NS, PZ, NZ, ERR, VDD, GND and ACO (as long as GNDS is only loaded versus VDDS). The maximum voltage difference between the pins should not be greater than 6 V, the exception here being pin ERR.

APPLICATION HINTS

Connecting MR sensor bridges for safety-related applications

For safety-related applications iC-MSB*SAFETY* requires an external overvoltage protection of supply VDD (Zener diode with fuse, for instance) and external pull-down resistors at the inputs X3 to X6 towards GNDS (of up to 100 kΩ).

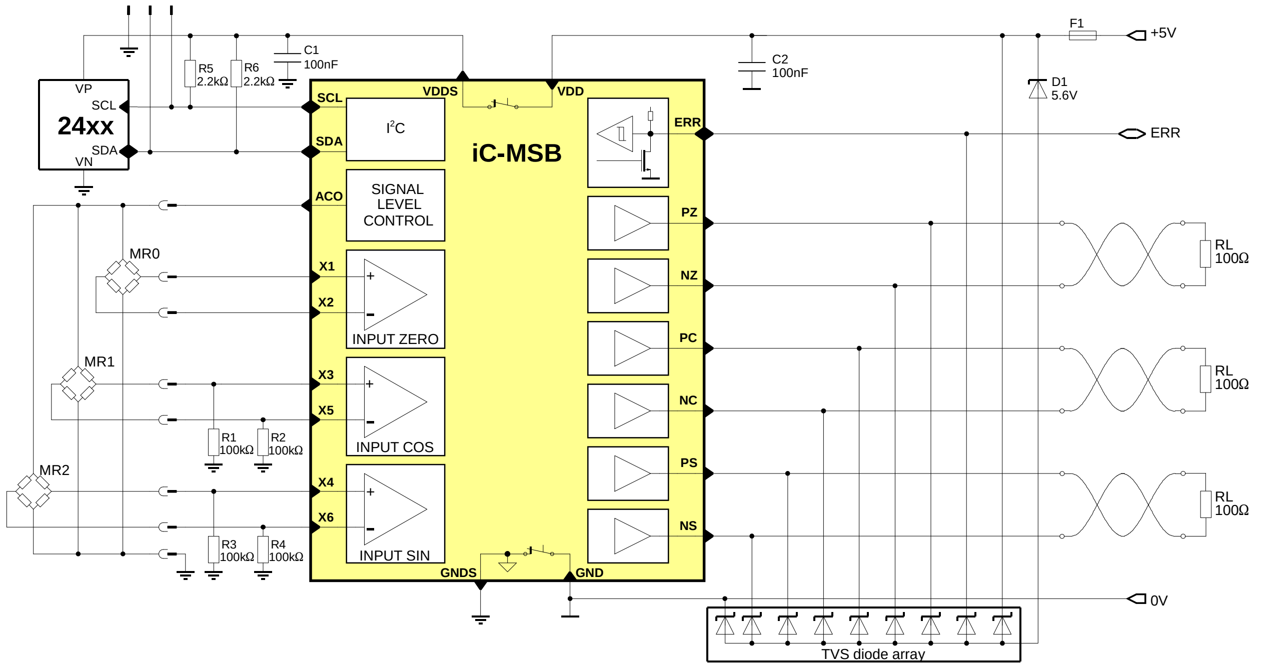


Figure 7: Example circuit for safety-related applications with iC-MSB*SAFETY*.

PLC Operation

There are PLCs with a remote sense supply which require longer for the voltage regulation to settle. At the same time the PLC inputs can have high-impedance resistances versus an internal, negative supply voltage which define the input potential for open inputs.

In this instance iC-MSB's reverse polarity protection feature can be activated as the outputs are tristate during the start phase and the resistances in the PLC determine the pin potential. During the start phase neither the supply VDD nor the output pins, which are also monitored, must fall to below ground potential (pin GND); otherwise the device is not configured and the outputs remain permanently set to tristate.

In order to ensure that iC-MSB starts with the PLCs mentioned above pull-up resistors can be used in the encoder. Values of 100 kΩ are usually sufficient; it is, however, recommended that PLC specifications be specifically referred to here.

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We understand suitable application of our published designs to be state-of-the-art technology which can no longer be classed as inventive under the stipulations of patent law. Our explicit application notes are to be treated only as mere examples of the many possible and extremely advantageous uses our products can be put to.

ORDERING INFORMATION

Type	Package	Order Designation
iC-MSB*SAFETY*	TSSOP20 TSSOP20 with thermal pad	iC-MSB TSSOP20 iC-MSB TSSOP20-TP
Evaluation Board iC-MSB*SAFETY*		iC-MSB EVAL MSB1D
iC-MSB2	TSSOP20	iC-MSB2 TSSOP20
Evaluation Board iC-MSB2		iC-MSB2 EVAL MSB1D

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (61 35) 92 92-0
Fax: +49 (61 35) 92 92-192
Web: http://www.ichaus.com
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