

iC-MSB^{SAFETY}, iC-MSB2

SIN/COS SIGNAL CONDITIONER WITH 1V_{pp} DRIVER



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FEATURES

- ◆ PGA inputs to 500 kHz for differential and single-ended sensor signals
- ◆ Selectable adaptation to voltage or current signals
- ◆ Flexible pin assignment due to signal path multiplexers
- ◆ Sine/Cosine signal conditioning for offset, amplitude and phase
- ◆ Separate index signal conditioning
- ◆ Short-circuit-proof and reverse polarity tolerant output drivers (1 V_{pp} to 100 Ω)
- ◆ Stabilized output signal levels due to sensor control
- ◆ Signal and system monitoring with configurable alarm output
- ◆ Supply voltage monitoring with integrated switches for reversed-polarity-safe systems
- ◆ Excessive temperature protection with sensor calibration
- ◆ I²C multimaster interface
- ◆ Supply from 4.3 to 5.5 V, operation within -40 to +125 °C
- ◆ Suitable for *SAFETY* applications within -25 to +100 °C
- ◆ Verifiable chip release code
- ◆ Version **iC-MSB2** with output multiplexer (not for *SAFETY*)

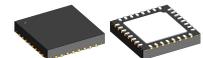
APPLICATIONS

- ◆ Programmable sensor interface for optical and magnetic position sensors
- ◆ Linear gauges and incremental encoders
- ◆ Linear scales

PACKAGES

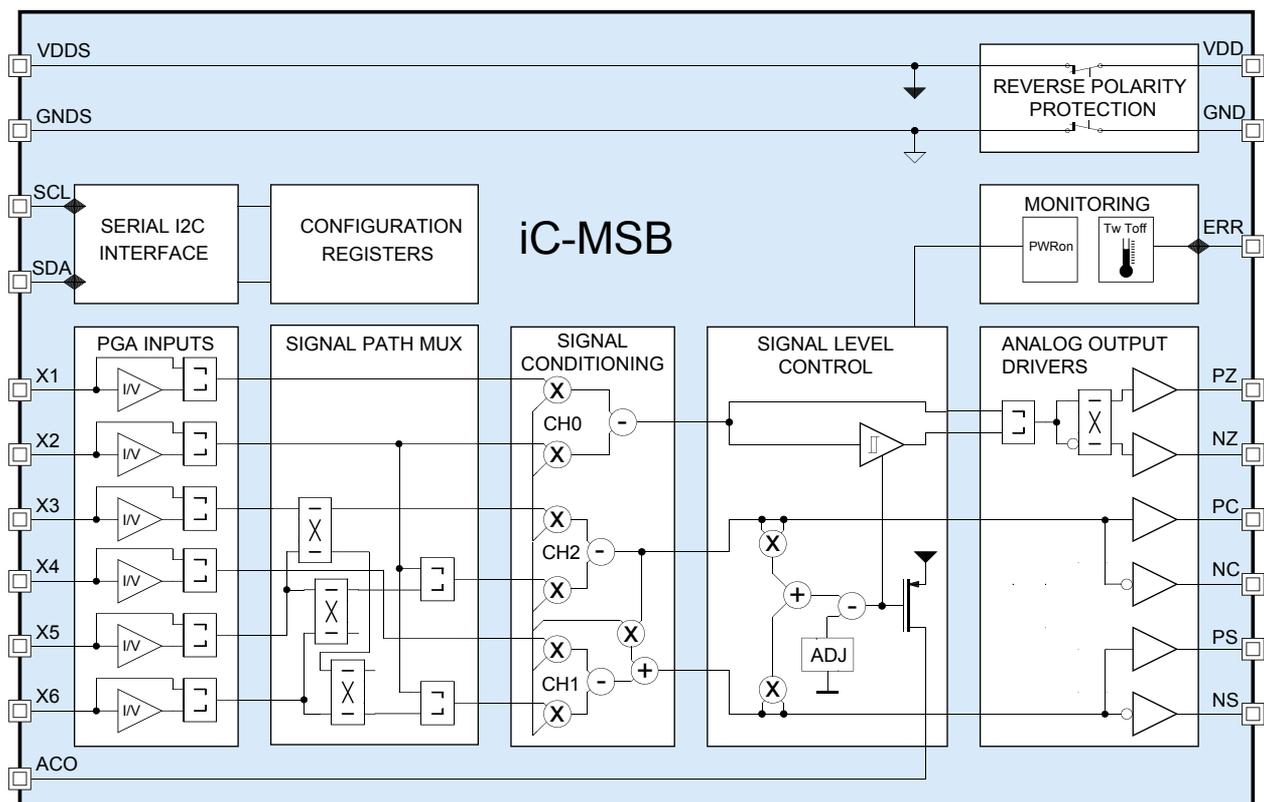


TSSOP20
TSSOP20-TP
RoHS compliant



QFN32
5 mm x 5 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-MSB is a signal conditioner with analog line drivers for sine/cosine sensors which are used to determine positions in linear and angular encoders, for example.

Programmable instrumentation amplifiers with selectable gain levels permit differential or referenced input signals; at the same time the modes of operation differentiate between high and low input impedance. This adaptation of the iC to voltage or current signals enables MR sensor bridges or photosensors to be directly connected up to the device.

The integrated signal conditioning unit allows signal amplitudes and offset voltages to be calibrated accurately and also any phase error between the sine and cosine signals to be corrected. Separate zero signal conditioning settings can be made for the gain and offset; data is then output either as an analog or a differential square-wave signal (low/high level analogous to the sine/cosine amplitude).

For the stabilization of the sine and cosine output signal levels a control signal is generated from the conditioned and calibrated input signals which can power the transmitting LED of optical systems via the integrated 50 mA driver stage (output ACO). If MR sensors are connected this driver stage also powers the measuring bridges.

By tracking the sensor energy supply any signal variations and temperature and aging effects can be compensated for and the set signal amplitude maintained with absolute accuracy. At the same time the control circuitry monitors both whether the sensor is functioning correctly and whether it is properly connected; signal loss due to wire breakage, short circuiting, dirt or aging, for example, is recognized when control

thresholds are reached and indicated at alarm output ERR.

iC-MSB is protected against a reversed power supply voltage; the integrated voltage switch for loads of up to 20 mA extends this protection to cover the overall system. The analog output drivers are directly cable-compatible and tolerant to false wiring; if supply voltage is connected up to these pins, the device is not destroyed.

The device configuration and calibration parameters are CRC protected and stored in an external EEPROM; they are loaded automatically via the I2C interface once the supply voltage has been connected up.

A safety-technical analysis of iC-MSB on device level with the inclusion of layout and internal/external circuitry has been carried out together with the BGIA, St. Augustin. The result proved iC-MSB's capability for safety oriented applications with Siemens Sinumerik Controls.

General notice on application-specific programming

Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

For magnetic sensor systems: The chip's performance in application is impacted by system conditions like the quality of the magnetic target, field strength and stray fields, temperature and mechanical stress, sensor alignment and initial calibration.

For optical sensor systems: The chip's performance in application is impacted by system conditions like the quality of the optical target, the illumination, temperature and mechanical stress, sensor alignment and initial calibration.

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iC-MSB SAFETY, iC-MSB2

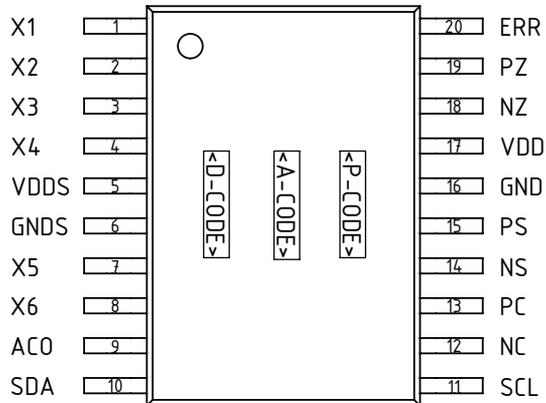
SIN/COS SIGNAL CONDITIONER WITH 1Vpp DRIVER



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PACKAGING INFORMATION

PIN CONFIGURATION TSSOP20, TSSOP20-TP



PIN FUNCTIONS

No.	Name	Function
1	X1	Signal Input 1 (Index +)
2	X2	Signal Input 2 (Index -)
3	X3	Signal Input 3
4	X4	Signal Input 4
5	VDDS ¹	Switched Supply Output and Internal Analog Supply Voltage (reverse-polarity-proof, load 20 mA max.)
6	GNDS ¹	Switched Ground (reverse-polarity-proof)
7	X5	Signal Input 5
8	X6	Signal Input 6
9	ACO	Signal Level Controller, high-side current source output
10	SDA	Serial Configuration Interface, data line
11	SCL	Serial Configuration Interface, clock line
12	NC	Neg. Cosine Output
13	PC	Pos. Cosine Output
14	NS	Neg. Sine Output
15	PS	Pos. Sine Output
16	GND	Ground
17	VDD	+4.5 to +5.5 V Supply Voltage
18	NZ	Neg. Index Output
19	PZ	Pos. Index Output
20	ERR	Error Signal (In/Out), and Test Mode Trigger Input
	TP ²	Thermal Pad (TSSOP20-TP)

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);

¹ It is advisable to connect a bypass capacitor of about 100 nF (up to 1 μ F max.) close to the chip's analog supply terminals.

² To improve heat dissipation the *thermal pad* of the package (bottom side) should be joined to an extended copper area which must have GNDS potential.

iC-MSB^{SAFETY}, iC-MSB2

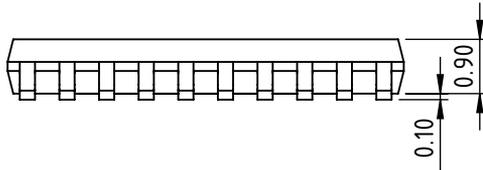
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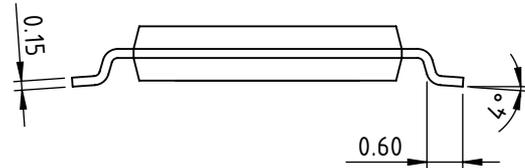
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PACKAGE DIMENSIONS : TSSOP20-TP

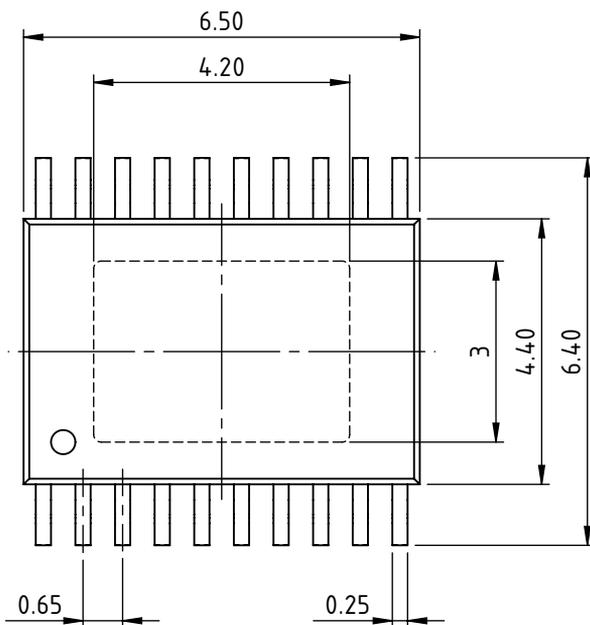
SIDE



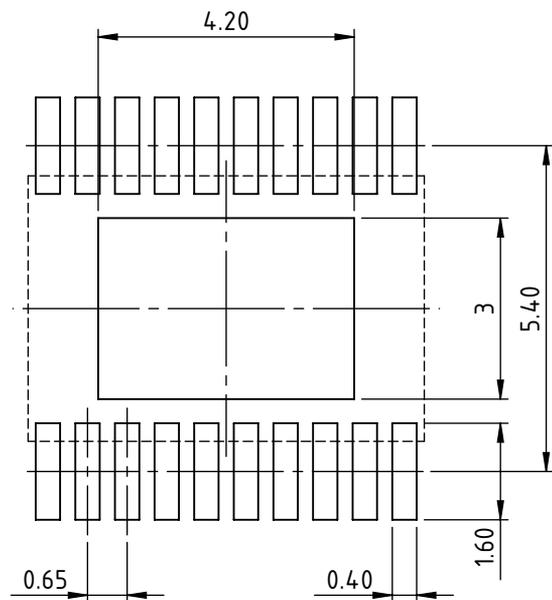
FRONT



TOP



RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-153

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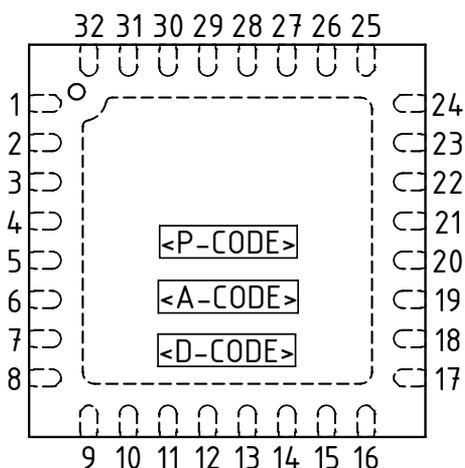
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PIN CONFIGURATION



PIN FUNCTIONS

No.	Name	Function
1, 2	n.c. ³	
3	ERR	Error Signal (In/Out), and Test Mode Trigger Input
4, 5	n.c. ³	
6	X1	Signal Input 1 (Index +)
7	X2	Signal Input 2 (Index -)
8, 9	n.c. ³	
10	X3	Signal Input 3
11	X4	Signal Input 4
12	VDD ^S 1	Switched Supply Output and Internal Analog Supply Voltage (reverse-polarity-proof, load 20 mA max.)
13	GNDS ¹	Switched Ground (reverse-polarity-proof)
14	X5	Signal Input 5
15	X6	Signal Input 6
16	n.c. ³	
17	ACO	Signal Level Controller, high-side current source output
18	n.c. ³	
19	SDA	Serial Configuration Interface, data line
20, 21	n.c. ³	
22	SCL	Serial Configuration Interface, clock line
23, 24	n.c. ³	
25	NC	Neg. Cosine Output
26	PC	Pos. Cosine Output
27	NS	Neg. Sine Output
28	PS	Pos. Sine Output
29	GND	Ground
30	VDD	+4.5 to +5.5 V Supply Voltage
31	NZ	Neg. Index Output
32	PZ	Pos. Index Output
	BP ²	Backside Paddle

(top view) IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);

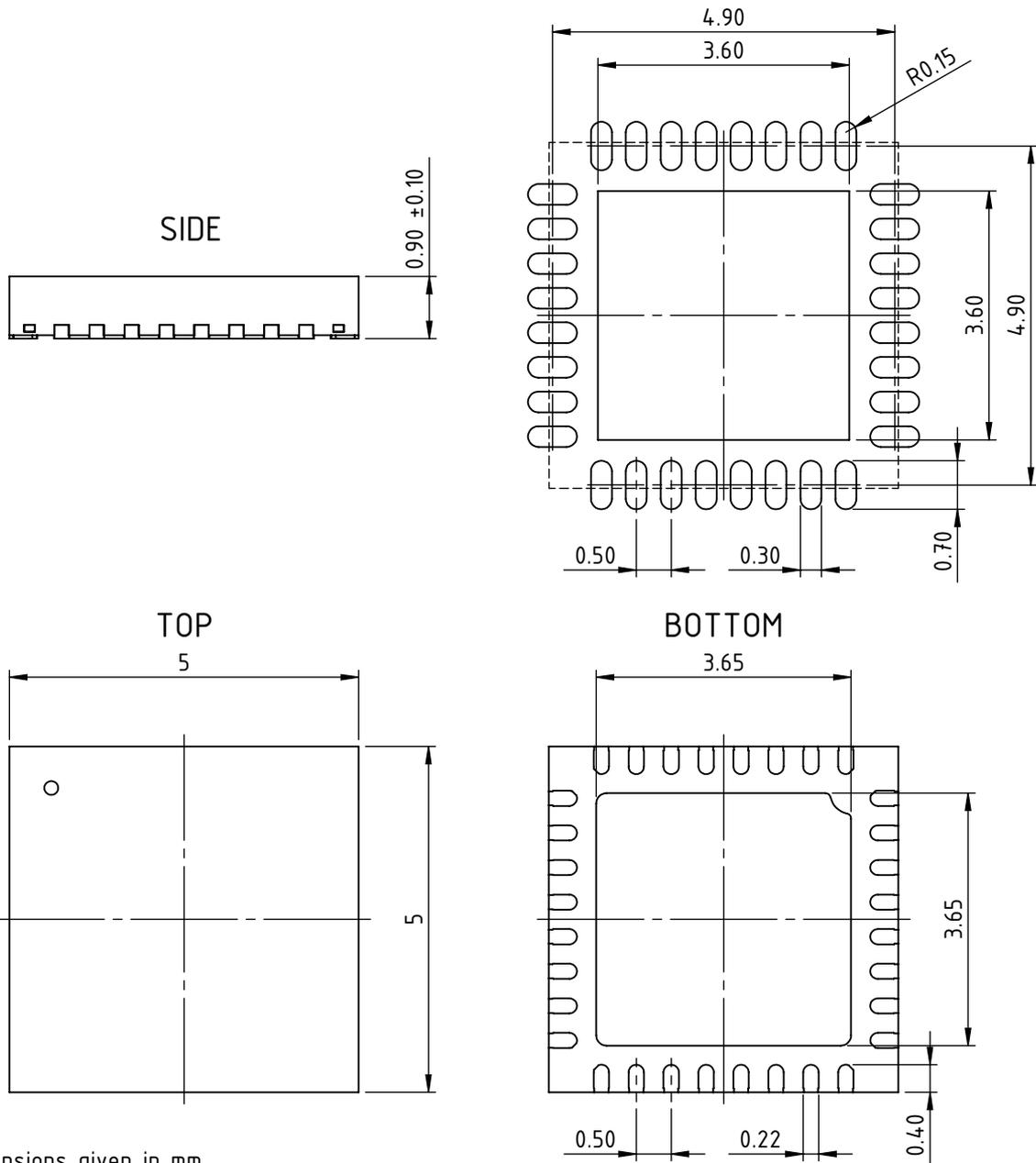
¹ It is advisable to connect a bypass capacitor of about 100 nF (up to 1 μF max.) close to the chip's analog supply terminals.

² To improve heat dissipation the backside paddle should be soldered and joined to an extended copper area, which must have GNDS potential.

³ Pin numbers marked n.c. are not connected.

PACKAGE DIMENSIONS : QFN32-5x5 (5 mm x 5 mm)

RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

iC-MSB^{SAFETY}, iC-MSB2

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ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions			Unit
				Min.	Max.	
G001	V()	Voltage at VDD, GND, PC, NC, PS, NS, PZ, NZ, ACO		-6	6	V
G002	V()	Voltage at ERR		-6	8	V
G003	V()	Pin-To-Pin Voltage between VDD, GND, PC, NC, PS, NS, PZ, NZ, ACO, ERR			6	V
G004	V()	Voltage at X1...X6, SCL, SDA		-0.3	V _{DDS} + 0.3	V
G005	I(VDD)	Current in VDD		-100	100	mA
G006	I()	Current in V _{DDS} , GNDS		-50	50	mA
G007	I()	Current in X1...X6, SCL, SDA, ERR, PC, NC, PS, NS, PZ, NZ		-20	20	mA
G008	I(ACO)	Current in ACO		-100	20	mA
G009	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G010	P _{tot}	Permissible Power Dissipation	TSSOP20 TSSOP20-TP, QFN32-5x5		300 400	mW mW
G011	T _j	Junction Temperature		-40	150	°C
G012	T _s	Storage Temperature Range		-40	150	°C

THERMAL DATA

VDD = 4.3...5.5 V

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
T01	T _a	Operating Ambient Temperature Range	iC-MSB2 TSSOP20	-25		100	°C
			iC-MSB TSSOP20	-25		100	°C
			iC-MSB TSSOP20-TP	-40		125	°C
			iC-MSB QFN32-5x5	-40		125	°C
T02	T _{a_safe}	Operating Ambient Temperature Range for SAFETY Applications	for iC-MSB and all package models	-25		100	°C
T03	R _{thja}	Thermal Resistance Chip to Ambient	TSSOP20 surface mounted to PCB according to JEDEC 51		80		K/W
T04	R _{thja}	Thermal Resistance Chip to Ambient	TSSOP20-TP surface mounted to PCB (incl. the thermal pad), according to JEDEC 51		35		K/W
T05	R _{thja}	Thermal Resistance Chip to Ambient	QFN32-5x5 surface mounted to PCB (incl. the backside paddle), according to JEDEC 51		40		K/W

All voltages are referenced to Pin GNDS unless otherwise stated.

All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

iC-MSB^{SAFETY}, iC-MSB2

SIN/COS SIGNAL CONDITIONER WITH 1V_{pp} DRIVER



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ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, T_j = -40...140 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Total Device							
001	VDD	Permissible Supply Voltage VDD versus GND	load current I(VDDS) up to 10 mA load current I(VDDS) up to 20 mA	4.3 4.5		5.5 5.5	V V
002	I(VDD)	Supply Current in VDD to GND	T _j = 27 °C, no load		25	50	mA
003	I(VDDS)	Permissible Load Current VDDS		-20		0	mA
004	Vc _{()hi}	Clamp Voltage hi at all pins				11	V
005	Vc _{()hi}	Clamp Voltage hi at inputs SCL, SDA	Vc _{()hi} = V() – V(VDDS), I() = 1 mA	0.4		1.5	V
006	Vc _{()hi}	Clamp Voltage hi at inputs X1...X6	Vc _{()hi} = V() – V(VDDS), I() = 4 mA	0.3		1.2	V
007	Vc _{()lo}	Clamp Voltage lo at all pins	I() = -4 mA	-1.2		-0.3	V
008	Irev(VDD)	Reverse-Polarity Current VDD vs. GND	V(VDD) = -5.5 V...-4.3 V	-1		1	mA
PGA Inputs and Signal Conditioning: X3...X6							
101	Vin _{()sig}	Permissible Input Voltage Range	RIN12(3:0) = 0x01 RIN12(3:0) = 0x09, BIAS12 = 1 RIN12(3:0) = 0x09, BIAS12 = 0	0.75 0 0		VDDS - 1.5 VDDS VDDS - 1.5	V V V
102	Iin _{()sig}	Permissible Input Current Range	RIN12(0) = 0, BIAS12 = 0 RIN12(0) = 0, BIAS12 = 1	-300 10		-10 300	µA µA
103	Iin ₍₎	Input Current	RIN12(3:0) = 0x01	-10		10	µA
104	Rin ₍₎	Input Resistance vs. VREFin	T _j = 27 °C; RIN12(3:0) = 0x09 RIN12(3:0) = 0x00 RIN12(3:0) = 0x02 RIN12(3:0) = 0x04 RIN12(3:0) = 0x06	16 1.1 1.6 2.2 3.2	20 1.6 2.3 3.2 4.6	24 2.1 3.0 4.2 6.0	kΩ kΩ kΩ kΩ kΩ
105	TCRin ₍₎	Temperature Coefficient Rin			0.15		%/K
106	VREFin12	Reference Voltage	RIN12(0) = 0, BIAS12 = 1 RIN12(0) = 0, BIAS12 = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
107	G12	Selectable Gain Factors	RIN12(3:0) = 0x01, GR12, GF1, GF2 = 0x0 RIN12(3:0) = 0x01, GR12, GF1, GF2 = max. RIN12(3:0) = 0x09, GR12, GF1, GF2 = 0x0 RIN12(3:0) = 0x09, GR12, GF1, GF2 = max.		2 100 0.5 25		
108	ΔGdiff	Differential Gain Accuracy	calibration range 11 bit	-0.5		0.5	LSB
109	ΔGabs	Absolute Gain Accuracy	calibration range 11 bit, guaranteed monotony	-1		1	LSB
110	Vin _{()diff}	Recommended Differential Input Voltage	Vin _{()diff} = V(CHPx) – V(CHNx); RIN12(3) = 0 RIN12(3) = 1	10 40		500 2000	mV _{pp} mV _{pp}
111	Vin _{()os}	Input Offset Voltage	referred to side of input		20		µV
112	VOScal	Offset Calibration Range	referred to the selected source (VOS12); ORx = 00 ORx = 01 ORx = 10 ORx = 11		±100 ±200 ±600 ±1200		%V() %V() %V() %V()
113	ΔVOSdiff	Differential Linearity Error of Offset Correction	calibration range 11 bit	-0.5		0.5	LSB
114	ΔVOSint	Integral Linearity Error of Offset Correction	calibration range 11 bit	-1		1	LSB
115	PHIkorr	Phase Error Calibration Range	CH1 versus CH2		±10.4		°
116	ΔPHIdiff	Differential Linearity Error of Phase Calibration	calibration range 10 bit	-0.5		0.5	LSB
117	ΔPHInt	Integral Linearity Error of Phase Calibration	calibration range 10 bit	-1		1	LSB
119	fin _{()max}	Permissible Input Frequency		500			kHz

iC-MSB SAFETY, iC-MSB2

SIN/COS SIGNAL CONDITIONER WITH 1Vpp DRIVER



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ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...140 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
120	fc()in	Input Amplifier Cut-off Frequency (-3dB)		250			kHz
PGA Inputs and Signal Conditioning: X1, X2							
201	Vin()sig	Permissible Input Voltage Range	RIN0(3:0) = 0x01	0.75		VDDS - 1.5	V
			RIN0(3:0) = 0x09	0		VDDS	V
202	lin()sig	Permissible Input Current Range	RIN0(0) = 0, BIAS0 = 0 RIN0(0) = 0, BIAS0 = 1	-300 10		-10 300	µA µA
203	lin()	Input Current	RIN0(3:0) = 0x01	-10		10	µA
204	Vout(X2)	Output Voltage at X2	BIASEX = 10, I(X2) = 0, referenced to VREFin12	95	100	105	%
205	Vin(X2)	Permissible Input Voltage at X2	BIASEX = 11	0.5		VDDS - 2	V
206	Rin(X2)	Input Resistance at X2	BIASEX = 11, RIN0(3:0) = 0x01, RIN12(3:0) = 0x01	20	27	35	kΩ
207	Rin()	Input Resistance vs. VREFin	Tj = 27 °C;				
			RIN0(3:0) = 0x09	16	20	24	kΩ
			RIN0(3:0) = 0x00	1.1	1.6	2.1	kΩ
			RIN0(3:0) = 0x02	1.6	2.3	3.0	kΩ
			RIN0(3:0) = 0x04	2.2	3.2	4.2	kΩ
		RIN0(3:0) = 0x06	3.2	4.6	6.0	kΩ	
208	TCRin()	Temperature Coefficient Rin			0.15		%/K
209	VREFin0	Reference Voltage	RIN0(0) = 0, BIAS0 = 1	1.35	1.5	1.65	V
			RIN0(0) = 0, BIAS0 = 0	2.25	2.5	2.75	V
210	G0	Selectable Gain Factors	RIN0(3:0) = 0x01, GR0 and GF0 = 0x0		2		
			RIN0(3:0) = 0x01, GR0 and GF0 = max.		100		
			RIN0(3:0) = 0x09, GR0 and GF0 = 0x0		0.5		
			RIN0(3:0) = 0x09, GR0 and GF0 = max		25		
211	ΔGdiff	Differential Gain Accuracy	calibration range 5 bit	-0.5		0.5	LSB
212	ΔGabs	Absolute Gain Accuracy	calibration range 5 bit, guaranteed monotony	-1		1	LSB
213	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(CHP0) - V(CHN0); RIN0(3:0) = 0x01 RIN0(3:0) = 0x09	10 40		500 2000	mVpp mVpp
214	Vin()os	Input Offset Voltage	referred to side of input		75		µV
215	VOScal	Offset Calibration Range	referenced to the selected source (REFVOS); OR0 = 00 OR0 = 01 OR0 = 10 OR0 = 11		±100 ±200 ±600 ±1200		%V() %V() %V() %V()
216	ΔVOSdiff	Differential Linearity Error of Offset Correction	calibration range 6 bit	-0.5		0.5	LSB
217	ΔVOSint	Integral Linearity Error of Offset Correction	calibration range 6 bit	-1		1	LSB
Signal Filter							
301	fc	Cut-off Frequency	ENF = 1, f()in 100 kHz for sine/cosine			4000	kHz
302	phi	Phase Delay (output vs. input)	ENF = 1, f()in 500 kHz for sine/cosine			10	°
Index Pulse Comparator Output PZ, NZ							
401	Vpk()	Output Amplitude With Sensor Tracking via ACO	EAZ = 1, ADJ(4:0) = 0x19	225	250	275	mV
402	SR()	Output Slew Rate	EAZ = 1		1		V/µs

iC-MSB SAFETY, iC-MSB2

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ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...140 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Analog Output Drivers: PS, NS, PC, NC, PZ, NZ							
501	Vpk(max)	Permissible Max. Output Amplitude	VDD = 4.5 V, DC level = VDD/2, RL = 50 Ω vs. VDD/2			300	mV
502	Vpk()	Output Amplitude With Sensor Tracking via ACO	ADJ(8:0) = 0x19	225	250	275	mV
503	Vdc()	DC Output Voltage	versus GND; reference is VPAH, see 802 for tolerances		50		% VDD
504	fc(out)	Cut-off Frequency	CL = 250 pF	500			kHz
506	Isc()	Short-circuit Current	pin shorten to VDD or GND	10	30	50	mA
507	Iik()	Tristate Leakage Current	tristate or reversed supply	-1		1	µA
508	Rout()	Output Impedance	MODE = 0x02 (mode calibration 2), BYP = 0		5		kΩ
509	fout(cal)	Permissible Output Frequency for Calibration	MODE = 0x02 (mode calibration 2), BYP = 0 CL = 250 pF			2	kHz
510	Rout(tm)	Bypass Resistance	MODE = 0x02, 0x06, BYP = 1		7		kΩ
Signal Level Controller ACO							
601	Vs(hi)	Saturation Voltage hi at ACO vs. VDD	Vs() = VDD - V(); ADJ(8:0) = 0x11F, I() = -5 mA ADJ(8:0) = 0x13F, I() = -10 mA ADJ(8:0) = 0x15F, I() = -25 mA Tj < 125 °C, ADJ(8:0) = 0x17F, I() = -50 mA Tj > 125 °C, ADJ(8:0) = 0x17F, I() = -50 mA			1 1 1 1 1.2	V V V V V
602	Isc(hi)	Short-circuit Current hi in ACO	Tj < 125 °C, V() = 0 ... VDD - 1 V; Tj > 125 °C, V() = 0 ... VDD - 1.2 V; ADJ(8:0) = 0x11F ADJ(8:0) = 0x13F ADJ(8:0) = 0x15F ADJ(8:0) = 0x17F	-10 -20 -50 -100	-66	-5 -10 -25 -50	mA mA mA mA
603	tr()	Current Rise Time in ACO	I(ACO): 0 → 90 % setpoint		1		ms
604	tset()	Current Settling Time in ACO	Square control, I(ACO): 50 → 100 % setpoint		400		µs
605	It(min)	Control Range Monitoring 1: lower limit	referenced to range ADJ(6:5)		3		%Isc
606	It(max)	Control Range Monitoring 2: upper limit	referenced to range ADJ(6:5)		90		%Isc
607	Vt(min)	Signal Level Monitoring 1: lower limit	referenced to Vscq()		40		%Vpp
608	Vt(max)	Signal Level Monitoring 2: upper limit	referenced to Vscq()		130		%Vpp
609	Vin(ACO)	Permissible Input Voltage for Offset-Tracking	versus GNDS, VOS12 = 0x0	0		VDDS	V
Test Current ERR							
701	I(ERR)	Permissible Test Current	test mode activated	0		1	mA
Bias Current Source and Reference Voltages							
801	IBN()	Bias Current Source	MODE(3:0) = 0x01, I(NC) vs. VDDS	180	200	220	µA
802	VPAH	Reference Voltage VPAH	referenced to GND	45	50	55	%VDD
803	V05	Reference Voltage V05		450	500	550	mV
804	V025	Reference Voltage V025			50		%V05
Power-Down-Reset							
901	VDDon	Turn-on Threshold (power-on release)	increasing voltage at VDD vs. GND	3.7	4	4.3	V
902	VDDoff	Turn-off Threshold (power-down reset)	decreasing voltage at VDD vs. GND	3.2	3.5	3.8	V
903	VDDhys	Threshold Hysteresis	VDDhys = VDDon – VDDoff	0.3			V
Clock Oscillator							
A01	fclk()	Internal Clock Frequency	MODE(3:0) = 0x0A (measured at pin NS)	120	160	200	kHz

iC-MSB SAFETY, iC-MSB2

SIN/COS SIGNAL CONDITIONER WITH 1Vpp DRIVER



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ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...140 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Error Input/Output: ERR							
B01	Vs()lo	Saturation Voltage lo	vs. GND, I() = 4 mA			0.4	V
B02	Isc()	Short-circuit Current lo	vs. GND; V(ERR) ≤ VDD V(ERR) > VTMon	4 2			mA mA
B03	Vt()hi	Input Threshold Voltage hi	vs. GND			2	V
B04	Vt()lo	Input Threshold Voltage lo	vs. GND	0.8			V
B05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	300	500		mV
B06	Ipu()	Input Pull-up Current	V() = 0 ... VDD – 1V, EPU = 1	-400	-300	-200	µA
B07	Rpu()	Input Pull-Up Resistor	EPU = 0		500		kΩ
B08	Vpu()	Pull-up Voltage	Vpu() = VDD – V(), I() = -5 µA, EPU = 1			0.4	V
B09	VTMon	Test Mode Activation Threshold	increasing voltage at ERR			VDD + 1.5	V
B10	VTMoff	Test Mode Disabling Threshold	decreasing voltage at ERR	VDD + 0.5			V
B11	VTMhys	Test Mode Hysteresis	VTMhys = VTMon – VTMoff	0.15	0.3		V
B12	Iik()	Leakage Current	tristate or reversed supply voltage	-1	-10	-50	µA
B13	tp()tri	Propagation Delay System Error to Driver Shutdown (tristate)	V(ERR): hi → lo		35		µs
Supply Switch and Reverse Polarity Protection: VDDS, GNDS							
C01	Vs()	Saturation Voltage VDDS vs. VDD	Vs(VDDS) = VDD – V(VDDS) I(VDDS) = -10 mA...0 mA I(VDDS) = -20 mA...-10 mA			150 250	mV mV
C02	Vs()	Saturation Voltage GNDS vs. GND	Vs(GNDS) = V(GNDS) – GND I(GNDS) = 0 mA...10 mA I(GNDS) = 10 mA...20 mA			150 250	mV mV
C03	C()	Backup Capacitor Analog Supply VDDS vs. GNDS		100			nF
Serial I²C Interface: SCL, SDA							
D01	Vs()lo	Saturation Voltage lo	I() = 4 mA			400	mV
D02	Isc()	Short-circuit Current lo		4		80	mA
D03	Vt()hi	Input Threshold Voltage hi				2	V
D04	Vt()lo	Input Threshold Voltage lo		0.8			V
D05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	300	500		mV
D06	Ipu()	Input Pull-up Current	V() = 0...VDDS – 1V	-650	-300	-60	µA
D07	Vpu()	Input Pull-up Voltage	Vpu() = VDDS – V(), I() = -5 µA			0.4	V
D08	fclk(SCL)	Clock Frequency at SCL	ENFAST = 0 ENFAST = 1	60 240	80 320	100 400	kHz kHz
D09	tbusy()cfg	Duration of Startup Configuration	IBN not calibrated, EEPROM access without read failure, time to outputs operational; ENFAST = 0 ENFAST = 1		40 25	55 35	ms ms
D10	tbusy()jerr	End Of I2C Communication; Time Until I2C Slave Mode Is Enabled	IBN not calibrated; V(SDA) = 0 V V(SCL) = 0 V or arbitration lost no EEPROM CRC ERROR		4 indef. 45 95	12 135 285	ms ms ms ms
D11	td()	Start Of Master Activity On I2C Protocol Error	SCL without clock signal: V(SCL) = constant; IBN not calibrated IBN calibrated to 200 µA	25 64	80 80	240 120	µs µs
D12	td()i2c	I2C-Slave Mode Enable Delay	no EEPROM, V(SDA) = 0 V		4	6.2	ms
D13	fclk()ext	Permissible External Clock Frequency at SCL				400	kHz

iC-MSB SAFETY, iC-MSB2

SIN/COS SIGNAL CONDITIONER WITH 1Vpp DRIVER



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ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 4.3...5.5 V, Tj = -40...140 °C, IBN calibrated to 200 µA, reference point GNDS, unless otherwise stated.

Item No.	Symbol	Parameter	Conditions				Unit
				Min.	Typ.	Max.	
Temperature Monitoring							
E01	VTs	Temperature Sensor Voltage	VTs() = VDDS – V(PS), Tj = 27 °C, Calibration Mode 3, no load	600	650	700	mV
E02	TCs	Temp. Co. of Temperature Sensor Voltage			-1.8		mV/K
E03	VTth	Temperature Warning Activation Threshold	VTth() = VDDS – V(NS), Tj = 27 °C, Calibration Mode 3, no load; CFGTA(3:0) = 0x00 CFGTA(3:0) = 0x0F	260 470	310 550	360 630	mV mV
E04	TCth	Temp. Co. Temperature Warning Activation Threshold			0.06		%/K
E05	Thys	Temperature Warning Hysteresis	Tj = 27 °C	4	12	20	°C
E06	ΔT	Relative Shutdown Temperature	ΔT = Toff – Tw, Tj = 27 °C	4	12	20	°C

PROGRAMMING

Register Layout	Page 15	Signal Conditioning CH1, CH2 (X3...X6) ..	Page 27
Serial I²C Interface	Page 17	GR12:	Gain Range CH1, CH2 (coarse)
ENFAST:	I ² C Fast Mode Enable	GF1:	Gain Factor CH1 (fine)
ENSL:	I ² C Slave Mode Enable	GF2:	Gain Factor CH2 (fine)
DEVID:	Device ID of EEPROM providing the chip configuration data (e.g. 0x50)	VOS12:	Offset Reference Source CH1, CH2
CHKSUM:	CRC of chip configuration data (address range 0x00 to 0x1E)	VDC1:	Intermediate Voltage CH1
CHPREL:	Chip Release	VDC2:	Intermediate Voltage CH2
NTRI:	Tristate Function and Op. Mode Change	OR1:	Offset Range CH1 (coarse)
		OF1:	Offset Factor CH1 (fine)
		OR2:	Offset Range CH2 (coarse)
		OF2:	Offset Factor CH2 (fine)
		PH12:	Phase Correction CH1 vs. CH2
Bias Current Source and Temperature Sensor	Page 20	Signal Conditioning CH0 (X1, X2)	Page 29
CFGIBN:	Bias Calibration	GR0:	Gain Range CH0 (coarse)
CFGTA:	Temperature Sensor Calibration	GF0:	Gain Factor CH0 (fine)
		VOS0:	Offset Reference Source CH0
		OR0:	Offset Range CH0 (coarse)
		OF0:	Offset Factor CH0 (fine)
Operating Modes	Page 21	Signal Level Control	Page 30
MODE:	Operation Mode	ADJ:	Setup of ACO Output Function
ENF:	Signal Filtering		
Test Mode	Seite 22	Monitoring and Error Output	Page 31
TMODE:	Test Mode Functions	EPH:	I/O Logic Alarm Output ERR
TMEM:	Test Mode Memory Selection	EMTD:	Min. Indication Time Alarm Outp. ERR
		EPU:	Pull-Up Enable Alarm Output ERR
		EMASKA:	Error Mask Alarm Output ERR
		EMASKO:	Error Mask Driver Shutdown
		EMASKE:	Error Mask EEPROM Savings
PGA Inputs Configuration and Signal Path Multiplexer	Page 23	ERR1:	Error Protocol: First Error
INMODE:	Diff./Single-Ended Input Mode	ERR2:	Error Protocol: Last Error
RIN12:	I/V Mode and Input Resistance CH1, CH2	ERR3:	Error Protocol: History
BIAS12:	Reference Voltage CH1, CH2		
RIN0:	I/V Mode and Input Resistance CH0	PDMODE:	Driver Activation
BIAS0:	Reference Voltage CH0		
MUXIN:	Input-To-Channel Assignment: X3...X6 to CH1, CH2		
INVZ:	Index Signal Inversion		
EAZ:	Index Comparator Enable		
MUXOUT:	Output Multiplexer (iC-MSB2 only)		
BIASEX:	Input Reference Selection		
BYP	Input-to-output Feedthrough		

iC-MSB^{SAFETY}, iC-MSB2

SIN/COS SIGNAL CONDITIONER WITH 1V_{pp} DRIVER



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CONFIGURATION REGISTERS

Register Map								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Interface								
0x00	ENFAST	DEVID(6:0)						
Calibration								
0x01	CFGIBN(3:0)				CFGTA(3:0)			
Operation Modes								
0x02	NTRI*	1	0	–	MODE(3:0)			
Input Configuration and Signal Path Multiplexer: iC-MSB								
0x03	EAZ	0	0	0	INVZ	INMODE	MUXIN(1:0)	
Input Configuration and Signal Path Multiplexer: iC-MSB2								
0x03	EAZ	MUXOUT(2:0)			INVZ	INMODE	MUXIN(1:0)	
Signal Conditioning CH1, CH2								
0x04	GF2(4:0)				GR12(2:0)			
0x05	GF1(7:0)							
0x06	VDC1(4:0)				GF1(10:8)			
0x07	VDC2(2:0)			VDC1(9:5)				
0x08	OR1(0)	VDC2(9:3)						
0x09	OF1(6:0)							OR1(1)
0x0A	OF2(1:0)	OR2(1:0)			OF1(10:7)			
0x0B	OF2(9:2)							
0x0C	PH12(6:0)							OF2(10)
0x0D	BIASEX(1:0)	BYP	1	1	PH12(9:7)			
0x0E	ENF	BIAS12	VOS12(1:0)		RIN12(3:0)			
Signal Level Controller								
0x0F	ADJ(0)	–	0	1	0	0	0	0
0x10	ADJ(8:1)							
Signal Conditioning CH0								
0x11	GF0(4:0)				GR0(2:0)			
0x12	OF0(5:0)					OR0(1:0)		
0x13	0	BIAS0	VOS0(1:0)		RIN0(3:0)			
Error Monitoring and Alarm Output								
0x14	0	EMASKA(6:0)						
0x15	TMODE(1:0)		EMTD(2:0)			EPH	0	0
0x16	0	EMASKO(6:0)*						
0x17	EMASKE(3:0)				ENSL	EPU	0	0
0x18	TMEM	PDMODE	0	0	0	EMASKE(6:4)*		
0x19.. 0x1A	not defined							
0x1B.. 0x1E	OEM Data							
Check Sum / Chip Release								
0x1F	EEPROM: CHKSUM(7:0) / ROM: CHPREL(7:0)							

Register Map								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Error Register								
0x20	–	ERR1(6:0)						
0x21	ERR2(5:0)						–	–
0x22	ERR3(3:0)				–	–	–	ERR2(6)
0x23	–	–	–	–	–	ERR3(6:4)		
Notes	The device RAM initially contains random data following power-on. *) Mandatory programming of EEPROM: NTRI = 1, EMASKO(6) = 0, EMASKE(6) = 0.							

Table 4: Register layout (EEPROM)

SERIAL I²C INTERFACE

The multi-master capable I²C interface consists of two bidirectional pins, SCL (for clock) and SDA (for data), and enables iC-MSB to restore its configuration from the external serial EEPROM. For this function, the read-out can be accelerated from ENFAST reading onwards if a higher clock frequency is selected as an option.

The I²C master of iC-MSB addresses I²C devices using an 8-bit register address plus 3 block selection bits as part of the I²C device ID. That way an external EEPROM of up to 2Kbit is addressed at 0x50 (for '1010 000' without the R/W bit), or 0xA0 respectively (for '1010 0000' with the R/W bit as zero), whereas the block selections bits are zero.

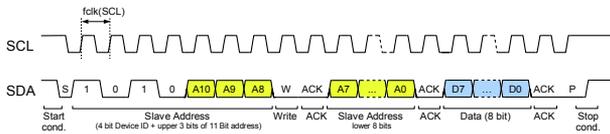


Figure 1: I²C slave addressing for writing a single byte to the EEPROM.

Furthermore, the I²C interface can be enabled to operate as an I²C slave (using ENSL), allowing an external I²C master to monitor and edit iC-MSB's configuration data.

ENFAST	
Code	Function
0	Regular clock rate, f(SCL) approx. 80 kHz
1	High clock rate, f(SCL) approx. 320 kHz
Notes	For in-circuit programming bus lines SCL and SDA require pull-up resistors (e.g. 2.2 kΩ for line capacitances of up to 170 pF and clock rate 320 kHz; the permissible minimum value is 1.5 kΩ). A ground trace between SCL and SDA is recommended to avoid cross talk.

Table 5: I²C Fast Mode

ENSL	
Code	Function
0	I ² C slave mode disabled
1	I ² C slave mode enabled (Device ID 0x55)

Table 6: I²C Slave Mode

I ² C Master Performance	
Protocol	Standard I ² C
Output Clock Rate	100 kHz max. (see Elec.Char. D08), 400 kHz max. using ENFAST = 1
Addressing	11 bit: 8 bit register address plus 3 bit block selection
Access Trials	Read: up to 4x at power-on (I ² C error: acknowledge missing), 1x at byte reading, 1x at byte writing (for consecutive writing with pauses from byte to byte)
Multi-Master Capability	Yes
I ² C Slave Performance	
Input Clock Rate	400 kHz max. (see Elec.Char. D13)
Device ID	0x55 ('1010 101' w/o R/W bit)

Table 7: I²C interface performance

Note: The I²C bus lines are sensitive. Keeping the traces short and shielding them with ground prevents unwanted actions.

The use of pull-up resistors (e.g. 2.2 kΩ at SCL and SDA) supports the bus signals on logic high and improves the EMI immunity.

Note: When programming the EEPROM in-circuit, iC-MSB must be powered up in advance to avoid interferences by its I²C master. Note that power must be maintained (e.g. for 10 ms) to allow the EEPROM finishing its write operation.

Attention: If a power failure interrupts the EEPROM's write operation, the entire page content may be lost.

Attention: If error logging is enabled and periodic errors occur, the maximum permissible write cycles may be exceeded. The recommended precaution is to disable error logging (refer to EMASKE), and to lock the EEPROM by its WP pin after factory calibration.

EEPROM Device Selection

EEPROM Device Requirements	
Supply Voltage	3.3 V to 5.5 V
Power-On Threshold	< 3.3 V (due to Elec.Char. 901)
Addressing	11 bit address max.
Device Address	0x50 ('1010 000' w/o R/W bit), 0xA0 ('1010 0000' with R/W = 0)
Page Buffer	Support of <i>Page Write</i> with pages of at least 4 bytes.
Size Minimum	512 bit (64x8 bit) (address range used is 0x00 to 0x3F)
Size Maximum	8 Kbit (4x 256x8 bit), type 24C08 If I ² C Slave Mode is disabled: 16 Kbit (8x 256x8 bit), type 24C16

Table 8: EEPROM Device Requirements

If the EEPROM does not feature *Page Write*, error events can not be saved (EMASKE must be configured to 0x00).

The following EEPROMs have been recommended, but may need to be re-tested for the above conditions: Atmel AT24C01, ST M24C01, ST M24C02 (2K), ROHM BR24L01A-W, BR24L02-W.

Attention: EEPROMs that ignore the block select or upper address bits in the control byte (such as the Microchip 24AA0x/24LC0xB, and maybe other 5-pin devices) should not be used with the iC-MSB. EEPROMs that use the address pins as additional enable bits should be used instead.

Attention: When I²C Slave Mode is enabled, iC-MSB responds to device ID 0x55, limiting the maximum EEPROM size to 8 Kbit (0x50 to 0x53 addresses 4x 256 bytes).

Device Startup

Once the supply has been switched on, i.e. after a power down reset, the iC-MSB outputs are high impedance (tristate) until a valid configuration is read from the EEPROM using device ID 0x50.

If the configuration data is not confirmed by its checksum, the readin process is repeated. If no valid configuration data is available after a fourth attempt, iC-MSB terminates communication with the EEPROM and enables I²C slave mode. For timing information, refer to the Electrical Characteristics, items D10 and D11.

For devices loading valid configuration data from the EEPROM, bit ENSL decides whether the I²C slave function is enabled or not.

Configuration Data Checksum

The checksum at address 0x1F is used to initially confirm the configuration data read from the EEPROM.

CHKSUM	Addr. 0x1F, bit 7:0
Code	Function
0x00... ...0xFF	Checksum for address range 0x00 to 0x1E; CRC polynomial 0x11D ($x^8 + x^4 + x^3 + x^2 + 1$) Start value: 0x01

Table 9: Configuration Data Checksum

Example of CRC Calculation Routine:

```

unsigned char ucDataStream = 0;
int iCRCPoly = 0x11D;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 1; // start value !!!
for (iReg = 0; iReg<31; iReg ++ )
{
    ucDataStream = ucGetValue(iReg);
    for (i=0; i<=7; i++) {
        if ((ucCRC & 0x80) != (ucDataStream & 0x80))
            ucCRC = (ucCRC << 1) ^ iCRCPoly;
        else
            ucCRC = (ucCRC << 1);
        ucDataStream = ucDataStream << 1;
    }
}
    
```

I²C Slave Mode (ENSL = 1)

In this mode iC-MSB behaves like an I²C slave with the device ID 0x55 and the configuration interface permits write and read accesses to iC-MSB's internal registers.

CHPREL	Adr 0x1F, bit 7:0 (ROM)
Code	Chip Release
0x00	Not available
0x04	iC-MSB SAFETY v4
0x05	iC-MSB SAFETY v5
0x25	iC-MSB2 v5

Table 10: Chip Release

NTRI	Adr 0x02, bit 7
Code	Function
0	Output drivers disabled
1	Setting the operating mode, output drivers active
Notes	NTRI is evaluated only during I ² C slave mode.

Table 11: Tristate Function And Op. Mode Change

Register	Read access in I ² C slave mode (ENSL = 1)
Address	Content
0x00-0x18	Configuration: register addresses 0x00-0x18
0x19-0x1A	Not available
0x1B-0x1E	OEM data (4 byte) (see EEPROM addresses 0x1B-0x1E)
0x1F	Chip release (ROM)
0x20-0x23	Configuration: register addresses 0x20-0x23
0x24-0x37	Not available
0x38	Configuration: register address 0x18
0x39-0x3A	Not available
0x3B-0x3E	OEM data (4 byte) (see EEPROM addresses 0x1B-0x1E)
0x3F	Chip release (ROM)
0x40-0x43	Current error memory (only active if enabled by EMASKE; messages are transferred to EEPROM Addresses 0x20-0x23)
0x44-0x7F	Not available

Table 12: RAM Read Access

Register	Write access in I ² C slave mode (ENSL = 1)
Address	Access and conditions
0x00	Changes possible, no restrictions
0x01	Changes possible (wrong entries for CFGIBN can limit functions)
0x02	Bit 7 = 0 (NTRI): changes to bits (6:0) permitted A change of operating mode follows only on writing Bit 7 = 1 (NTRI); when doing so changes to bits (6:0) are not permitted.
0x03-0x16	Changes possible, no restrictions
0x17	Bit 3 = 1 (ENSL): changes to bits (7:4) and (2:0) permitted
0x18	Changes possible, no restrictions
0x19-0x1A	Not available
0x1B-0x1E	Changes possible, no restrictions
others	No changes permitted

Table 13: RAM Write Access

BIAS SOURCE AND TEMPERATURE SENSOR

Bias Source Calibration

The calibration of the bias current source in operation mode *Calibration 1* (Tab. 16) is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. SCL clock frequency). For setup purposes the IBN value is measured using a 10 kΩ resistor by pin VDDS connected to pin NC. The setpoint is 200 μA which is equivalent to a measurement voltage of 2 V.

Note: The measurement delivers a false reading when outputs are tristate (due to a configuration error after cycling power, for instance).

CFGIBN Adr 0x01, bit 7:4			
Code k	IBN $\sim \frac{31}{39-k}$	Code k	IBN $\sim \frac{31}{39-k}$
0x0	79 %	0x8	100 %
0x1	81 %	0x9	103 %
0x2	84 %	0xA	107 %
0x3	86 %	0xB	111 %
0x4	88 %	0xC	115 %
0x5	91 %	0xD	119 %
0x6	94 %	0xE	124 %
0x7	97 %	0xF	129 %

Table 14: Bias Current Source Calibration

Temperature Sensor

The temperature monitor is calibrated in operating mode *Calibration Mode 3*.

To set the required warning temperature T_2 the temperature sensor voltage V_T at which the warning is generated is first determined. To this end a voltage ramp from VDDS towards GNDS is applied to pin PS until pin ERR triggers an error message (for EMASKA = 0x20 and EMTD = 0x00).

Example: $V_T(T_1)$ is approx. 650 mV, measured from VDDS versus PS, with $T_1 = 25^\circ\text{C}$;

The necessary activation threshold voltage $V_{Tth}(T_1)$ is then calculated. The required warning temperature T_2 , temperature coefficients TCs and TCth (see Electrical Characteristics, Section E) and measurement value $V_T(T_1)$ are entered into this calculation:

$$V_{Tth}(T_1) = \frac{V_T(T_1) + TCs \cdot (T_2 - T_1)}{1 + TCth \cdot (T_2 - T_1)}$$

Example: For $T_2 = T_1 + 100\text{K}$, $V_{Tth}(T_1)$ must be programmed to 443 mV.

Activation threshold voltage $V_{Tth}(T_1)$ is provided for a high impedance measurement (10 MΩ) at output pin NS (measurement versus VDDS) and must be set by programming CFGTA(3:0) to the calculated value.

Example: Altering $V_{Tth}(T_1)$ from 310 mV (measured with CFGTA(3:0) = 0x0) to 443 mV is equivalent to 143 %, the closest value for CFGTA is 0x9;

CFGTA Adr 0x01, bit 3:0			
Code k	$V_{Tth} \sim \frac{65+3.25k}{65}$	Code k	$V_{Tth} \sim \frac{65+3.25k}{65}$
0x0	100 %	0x8	140 %
0x1	105 %	0x9	145 %
0x2	110 %	0xA	150 %
0x3	115 %	0xB	155 %
0x4	120 %	0xC	160 %
0x5	125 %	0xD	165 %
0x6	130 %	0xE	170 %
0x7	135 %	0xF	175 %
Notes	With CFGTA = 0xF Toff is 80 °C typ., with CFGTA = 0x0 Toff is 155 °C typ.		

Table 15: Calibration of Temperature Monitoring

OPERATING MODES

In order to calibrate iC-MSB, compensate for the input signals and test iC-MSB the mode of operation must be changed. The output function changes according to the

various operating modes; the line drivers and protection against reverse polarity facility are only active in normal mode.

MODE(3:0)		Addr. 0x02; bit 3:0						
BYP		Addr. 0x0D; bit 5						
Code	Operating Mode	Pin PS	Pin NS	Pin PC	Pin NC	Pin PZ	Pin NZ	Pin ERR
0x00	Normal operation	PS	NS	PC	NC	PZ	NZ	ERR
0x01	Calibration 1	TANA0(2)	VREFI0	VREFI12	IBN	PZI	NZI	ERR
0x02	Calibration 2, BYP = 0 Calibration 2, BYP = 1*	PCH1 X4	NCH1 X6	PCH2 X3	NCH2 X5	VDC1 X1	VDC2 X2	—
0x03	iC-Haus Test 1	VPAH	VPD	—	CGUCK	IPF	V05	IERR
0x04	iC-Haus Test 2	PS_out	NS_out	PC_out	NC_out	PZ_out	NZ_out	IERR
0x05	iC-Haus Test 3	PS_out	NS_out	PC_out	NC_out	PZ_out	NZ_out	ERR
0x06	iC-Haus Test 4, BYP = 0 iC-Haus Test 4, BYP = 1*	TANA12(0) X4	TANA12(1) X6	TANA12(2) X3	TANA12(3) X5	TANA12(4) X1	TANA12(5) X2	IERR
0x07	Calibration 3	VTs	VTth	—	—	—	—	ERR
0x08	Saturation low	SCL, SDA and ERR low						
0x09	—	—	—	—	—	—	—	—
0x0A	iC-Haus Test 5	TP	CLK6	—	—	—	—	—
0x0B	—	—	—	—	—	—	—	—
0x0C	—	—	—	—	—	—	—	—
0x0D	—	—	—	—	—	—	—	—
0x0E	IDDQ-Test	All PU/PD resistors, oscillator and supply voltage deactivated						
0x0F	—	—	—	—	—	—	—	—
Notes	Analog calibration signals are output via approx. 5 kΩ source impedance (see Elec. Char. No.508). For accuracy of calibration the signal frequency should not exceed 2 kHz (see Elec. Char. No.509). * Bypass function: inputs (without voltage divider) to outputs, approx. 7 kΩ source impedance (see Elec. Char. No.510).							

Table 16: Selection of Operating Modes

Calibration Op. Modes

In *Calibration Mode 1* the user can measure the BIAS current (IBN), input amplifier reference potential VREFI and the analog signals from channel 0 following signal conditioning (PCH0 and NCH0).

In *Calibration Mode 2* the conditioned signals from channels 1 and 2 are output (PCH1, NCH1, PCH2 and NCH2). In addition the intermediate potentials of the compensating circuits are also available for CH1 (VDC1) and CH2 (VDC2).

In *Calibration Mode 3* the internal temperature monitoring signals are provided.

Special Device Test Functions

IDDQ-Test, Saturation Low, Saturation High, and Test 1 to 5 are test modes for iC-Haus device tests. With an activated bypass (BYP = 1), mode *iC-Haus Test 4* permits the direct feedthrough of X1 - X6 input signals to the output pins; in this instance the output impedance is high-ohmic. Furthermore, if the input voltage divider is selected (by RINx = 1--1), it reduces the signal amplitudes to approx. 7/8.

Signal Filter

iC-MSB has a noise limiting signal filter to filter the conditioned analog signals. This can be activated using ENF.

ENF		Adr 0x0E, bit 7
Code	Function	
0	Noise limiter deactivated	
1	Noise limiter activated	

Table 17: Signal Filtering

PGA INPUTS CONFIGURATION

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Referenced input signals can be processed as an option; in this mode input X2 acts as a reference. Both current and voltage signals can be processed as input signals, selected using RIN12(0) and RIN0(0).

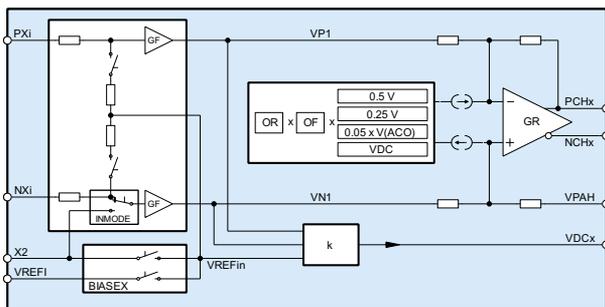


Figure 3: Signal conditioning input circuit.

Current Signals

In I Mode an input resistor Rin() becomes active at each input pin, converting the current signal into a voltage signal. Input resistance Rin() consists of a pad wiring resistor and resistor Rui() which is linked to the adjustable bias voltage source VREFin(). The following table shows the possible selections, with Rin() giving the typical resulting input resistance (see Electrical Characteristics for tolerances). The input resistor should be set in such a way that intermediate potentials VDC1 and VDC2 lie between 125 mV and 250 mV (verifiable in Calibration Mode 2).

Note: The input circuit is not suitable for back-to-back photodiodes.

Voltage Signals

In V Mode an optional voltage divider can be selected which reduces unacceptably large input amplitudes to approx. 25%. The circuitry is equivalent to the resistor chain in I Mode; the pad wiring resistor is considerably larger here, however.

For sensors whose offset calibration is to be proportional to an external DC voltage source the reference source can be selected using BIASEx; for all other sensors BIASEx should be set to '00'.

INMODE Adr 0x03, bit 2	
Code	Function
0	Differential input signals
1	Single-ended input signals*
Note	* Input X2 is reference for all inputs.

Table 20: Input Signal Mode

RIN12 Adr 0x0E, bit 3:0			
RIN0 Adr 0x13, bit 3:0			
Code	Nominal Rin()	Intern Rui()	I/V Mode
-000	1.7 kΩ	1.6 kΩ	current input
-010	2.5 kΩ	2.3 kΩ	current input
-100	3.5 kΩ	3.2 kΩ	current input
-110	4.9 kΩ	4.6 kΩ	current input
1—1	20 kΩ	5 kΩ	voltage input 4:1*
0—1	high impedance	1 MΩ	voltage input 1:1
Notes	RIN0 must be set as RIN12 when using INMODE = 1 for single-ended input signals. *) Refer to Elec.Char. No. 101 for permissible input voltage range. VREFin is the voltage divider's footpoint; input currents may be positive or negative (Vin > VREFin, or Vin < VREFin).		

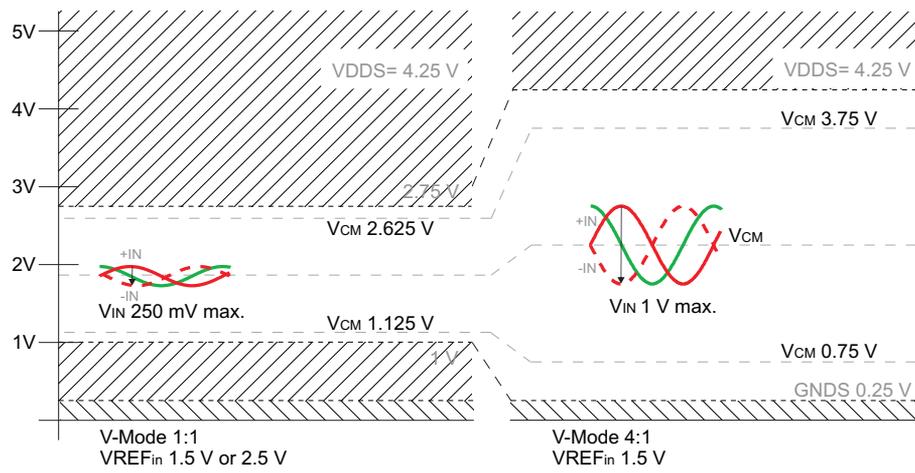
Table 21: I/V Mode and Input Resistance

BIAS12 Adr 0x0E, bit 6	
BIAS0 Adr 0x13, bit 6	
Code	Function
0	VREFI = 2.5 V for low-side current sinks (e.g. photodiodes with common anode at GNDS) Note*: V(PXi) + V(NXi) < 2 x VREFin
1	VREFI = 1.5 V for high-side current-sources (e.g. photodiodes with common cathode at VDD5) for voltage sources versus ground for Wheatstone sensor bridges (e.g. iC-SM2) for voltage sources with low-side reference (e.g. iC-LSHB, when using BIASEx = 11) Note*: V(PXi) + V(NXi) > 2 x VREFin
Notes	*) Relevant if using - offset references VDC1/VDC2 (see Table 36) - the input voltage divider (see Table 21) - sum control mode (see Table 47)

Table 22: Reference Voltage

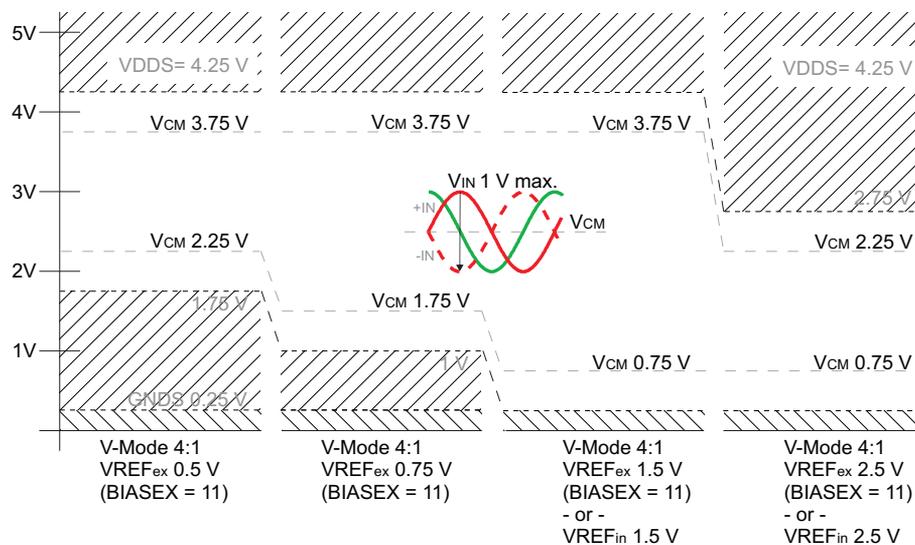
BIASEX ADR 0x0D, bit 7:6		
Code	VREFin	Pin function of X2
00*	internal	Input Index- (negative zero signal)
10	internal	Output of VREFin12*
11	external	Input for external reference**: V(X2) replaces VREFin
Notes	*) Do not load, buffering recommended **) See Elec. Char. Nos. 205 and 206	

Table 23: Input Reference Selection



NB: VREFin is referenced to GNDS.

Figure 4: Permissible common mode range and maximum input signal for lowest gain (GR12 = 0x0, GF1, GF2 = 0x00); left side: voltage input 1:1, right side: voltage input 4:1.



NB: VREFex and VREFin are referenced to GNDS.

Figure 5: Permissible common mode range for voltage input 4:1 in dependency to the reference voltage.

SIGNAL PATH MULTIPLEXING: iC-MSB SAFETY

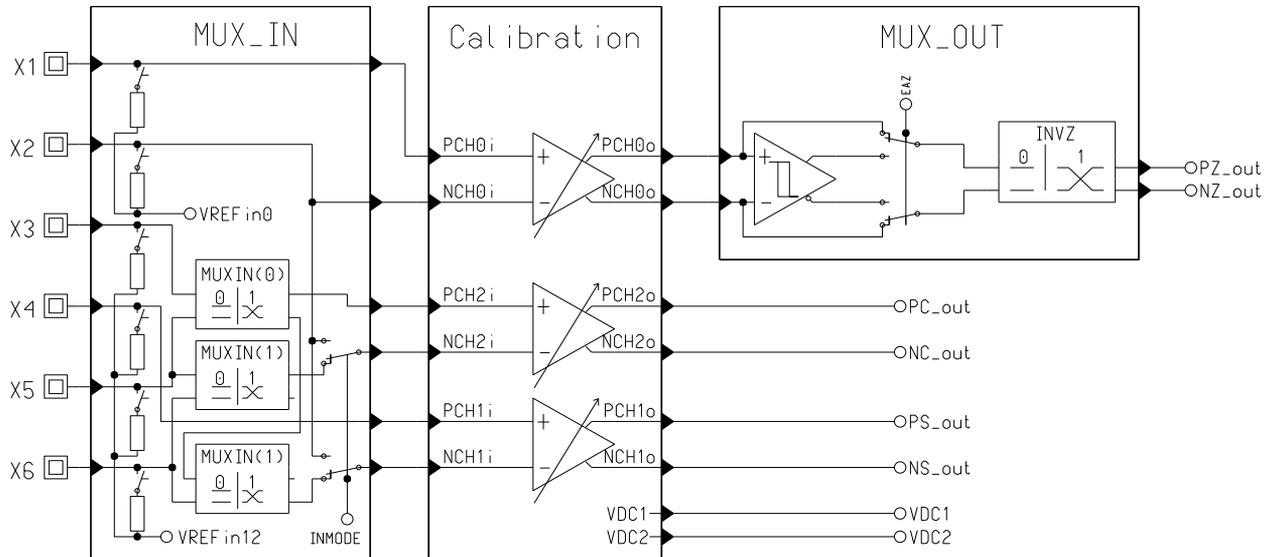


Figure 6: Multiplexer Schematics

The signals for index channel CH0 are connected up to pins X1 and X2. Pins X3 to X6 are allocated to internal channels CH1 and CH2 via MUXIN. INMODE can be activated for referenced input signals; this then selects X2 as the reference input. For output purposes INVZ allows the index signal phase to be inverted.

EAZ permits the activation of an analog comparator for index channel CH0.

MUXIN 0x03, bit 1:0				
Code	PCH1i	NCH1i	PCH2i	NCH2i
00	X4	X6	X3	X5
01	X4	X6	X5	X5
10	X4	X5	X3	X6
11	X4	X3	X5	X6

Table 24: Input Multiplexer for INMODE = 0

MUXIN 0x03, bit 1:0				
Code	PCH1i	NCH1i	PCH2i	NCH2i
-0	X4	X2	X3	X2
-1	X4	X2	X5	X2

Table 25: Input Multiplexer for INMODE = 1

EAZ Adr 0x03, bit 7	
Code	Function
0	Comparator bypass
1	Comparator active

Table 26: Index Comparator Enable

INVZ Adr 0x03, bit 3		
Code	PZ_out	NZ_out
0	PCH0o	NCH0o
1	NCH0o	PCH0o

Table 27: Index Signal Inversion

EXTENDED SIGNAL PATH MULTIPLEXING: iC-MSB2 (not for safety applications)

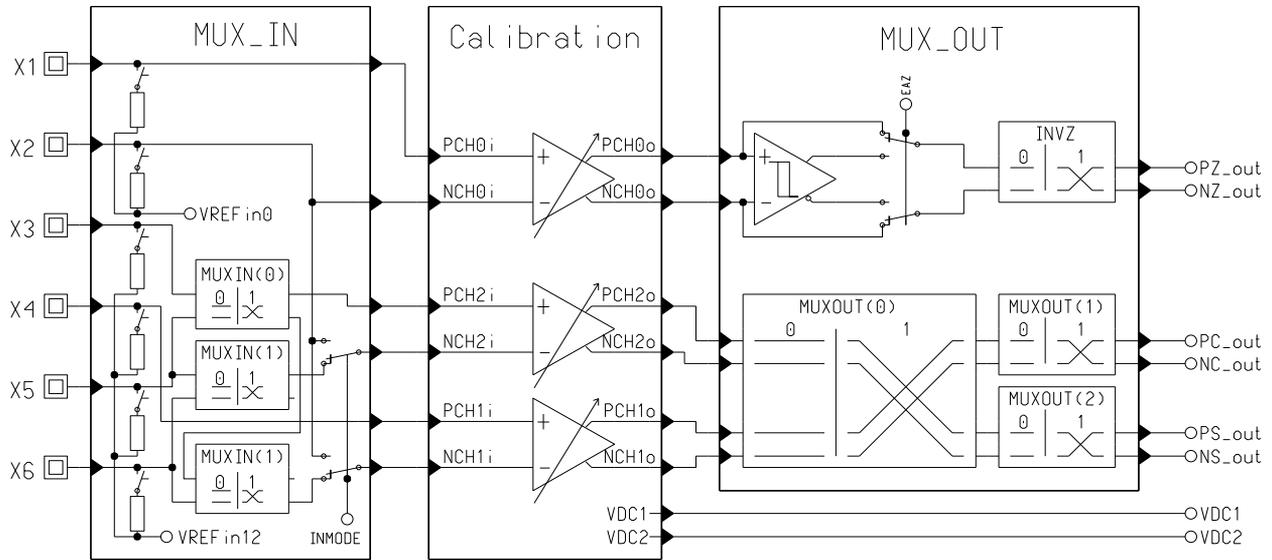


Figure 7: Multiplexer Schematics

The signals for index channel CH0 are connected up to pins X1 and X2. Pins X3 to X6 are allocated to internal channels CH1 and CH2 via MUXIN. INMODE can be activated for referenced input signals; this then selects X2 as the reference input. For output purposes INVZ allows the index signal phase to be inverted.

EAZ permits the activation of an analog comparator for index channel CH0.

MUXIN 0x03, bit 1:0				
Code	PCH1i	NCH1i	PCH2i	NCH2i
00	X4	X6	X3	X5
01	X4	X6	X5	X5
10	X4	X5	X3	X6
11	X4	X3	X5	X6

Table 28: Input Multiplexer for INMODE = 0

MUXIN 0x03, bit 1:0				
Code	PCH1i	NCH1i	PCH2i	NCH2i
-0	X4	X2	X3	X2
-1	X4	X2	X5	X2

Table 29: Input Multiplexer for INMODE = 1

INVZ Adr 0x03, bit 3		
Code	PZ_out	NZ_out
0	PCH0o	NCH0o
1	NCH0o	PCH0o

Table 30: Index Signal Inversion

EAZ Adr 0x03, bit 7	
Code	Function
0	Comparator bypass
1	Comparator active

Table 31: Index Comparator Enable

MUXOUT Adr 0x03, bit 6:4				
Code	PS_Out	NS_Out	PC_Out	NC_Out
000	Channel 1		Channel 2	
010	Channel 1		Channel 2 inverted	
100	Channel 1 inverted		Channel 2	
110	Channel 1 inverted		Channel 2 inverted	
001	Channel 2		Channel 1	
011	Channel 2		Channel 1 inverted	
101	Channel 2 inverted		Channel 1	
111	Channel 2 inverted		Channel 1 inverted	

Table 32: Output Multiplexer

SIGNAL CONDITIONING CH1, CH2

The voltage signals necessary for the conditioning of channels 1 and 2 can be measured in operation mode *Calibration 2*.

Gain Settings CH1, CH2

The gain is set in four stages:

1. The sensor supply tracking is shut down and the constant current source for the ACO output set to a suitable output current (register ADJ; current value close to the later operating point).
2. The coarse gain is selected so that the differential signal amplitudes of approx. 1 Vpp are produced (signal Px vs. Nx, see Figure below).
3. Using fine gain factor GF2 the CH2 signal amplitude is then adjusted to 1 Vpp.
4. The CH1 signal amplitude can then be adjusted to the CH2 signal amplitude via fine gain factor GF1.

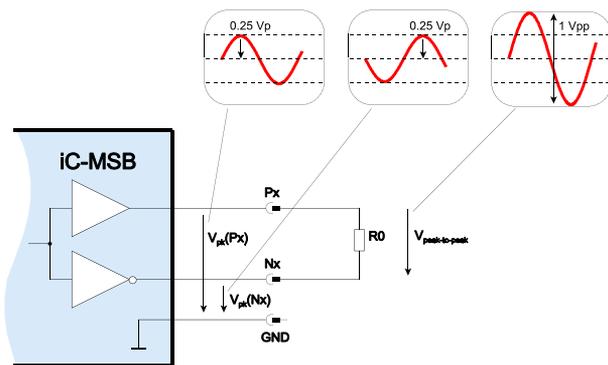


Figure 8: Definition of 1 Vpp signal. Termination R0 must be high-ohmic during all *Test* and *Calibration* modes.

GR12	
Adr 0x04, bit 2:0	
Code	Factor
0x0	2.0
0x1	4.1
0x2	5.3
0x3	6.7
0x4	8.7
0x5	10.5
0x6	13.2
0x7	16.0
Notes	The effective total gain calculates as: $G12_{\text{eff}} = GFx \times GR12$, respectively $G12_{\text{eff}} = 1/4 \times GFx \times GR12$ if using the input voltage divider (RIN12 = 0x9).

Table 33: Gain Range CH1, CH2

GF2	
Adr 0x04, bit 7:3	
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25 \frac{GF2}{31}$
0x1F	6.25

Table 34: Fine Gain Factor CH2

GF1	
Adr 0x06, bit 2:0, Adr 0x05, bit 7:0	
Code	Factor
0x000	1.0
0x001	1.0009
...	$6.25 \frac{GF1}{1984}$
0x7FF	6.6245

Table 35: Fine Gain Factor CH1

Offset Calibration CH1, CH2

In order to calibrate the offset the reference source must first be selected using VOS12. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which provide stable, self-regulating signals.

So that photosensors can be operated in optical encoders iC-MSB tracks changes in offset voltages via the signal-dependent source VDC when used in conjunction with the controlled sensor current source for LED supply (pin ACO). The VDC potential automatically tracks higher DC photocurrents. To this end intermediate potentials VDC1 and VDC2 must be adjusted to a minimal AC ripple using the selectable k factor.

The feedback of pin voltage V(ACO) fulfills the same task as source VDC when MR bridge sensors are supplied by the controlled current source or by supply VDDS.

VOS12	Adr 0x0E, bit 5:4
Code	Type of source
0x0	Feedback of ACO pin voltage: V(ACO)/20 for sensor supply-dependent diff. voltage signals for Wheatstone sensor bridges to measure VDDS
0x1, 0x2	Fixed reference: V05 of 500 mV, V025 of 250 mV for single-ended current or voltage signals for single-ended or differential stabilized signals (regulated sensor or waveform generator)
0x3	Self-tracking sources VDC1, VDC2 (125...250 mV) for differential current signals for differential voltage signals*
Notes	*) Requires BIASEX = 11 and the sensor's reference level connected to input X2 (see Elec. Char. No. 205 for acceptable input voltage).

Table 36: Offset Reference Source CH1, CH2

VDC1	Adr 0x07, bit 4:0; Adr 0x06, bit 7:3
VDC2	Adr 0x08, bit 6:0; Adr 0x07, bit 7:5
Code	$VDC_i = (1 - k) \cdot VPI + k \cdot VNi$
0x000	$k = 1/3$
0x001	$k = 0.3337$
...	$k = 1/3 + 1/3 \cdot Code/1023$
0x200	$k = 0.5000$ (center setting)
...	...
0x3FF	$k = 2/3$
Notes	Adjustment is required only if VOS12 = 0x3

Table 37: Intermediate Voltages CH1, CH2

The calibration range for the CH1/CH2 offset is dependent on the selected VOS12 source and is set using OR1 and OR2. Both sine and cosine signals are then calibrated using factors OF1 and OF2. The calibration target is reached when the DC fraction of the differential signals PCHx versus NCHx is zero.

OR1	Adr 0x09, bit 0; Adr 0x08, bit 7
OR2	Adr 0x0A, bit 5:4
Code	Range
0x0	x1
0x1	x2
0x2	x6
0x3	x12

Table 38: Offset Range CH1, CH2

OF1	Adr 0xA, bit 3:0; Adr 0x9, bit 7:1	OF2	Adr 0xC, bit 0; Adr 0xB, bit 7:0; Adr 0xA, bit 7:6
Code	Factor	Code	Factor
0x000	0	0x400	0
0x001	0.00098	0x401	- 0.00098
...	+ Code / 1023	...	-(Code - 1024) / 1023
0x3FF	1	0x7FF	- 1

Table 39: Offset Factors CH1, CH2

Phase Correction CH1 vs. CH2

The phase shift between CH1 and CH2 can be adjusted using parameter PH12. Following phase calibration other calibration parameters may have to be adjusted again (those as amplitude compensation, intermediate potentials and offset voltages).

PH12	Adr 0xD, bit 2:0; Adr 0xC, bit 7:1		
Code	Correction angle	Code	Correction angle
0x000	0°	0x200	0°
0x001	+ 0.0204°	0x201	- 0.0204°
...	+ 10.42° . PH12/511	...	- 10.42° . (PH12 - 512)/511
0x1FF	+ 10.42°	0x3FF	- 10.42°

Table 40: Phase Correction CH1 vs. CH2

SIGNAL CONDITIONING CH0

The voltage signals needed to calibrate channel 0 are available in *Calibration Mode 1*.

Gain Settings CH0

Parallel to the conditioning process for the CH1 and CH2 signals the CH0 gain is set in the following stages:

1. The sensor supply tracking unit is shut down and the constant current source for the ACO output set to the same output current as in the compensation of CH1 and CH2 (register ADJ; current value close to the later operating point).

2. The coarse gain is selected so that a differential signal amplitude of approx. 1 Vpp is produced internally (signal PCHx versus NCHx).

3. GF0 then permits fine gain adjustment to 1 Vpp.

GR0		Adr 0x11, bit 2:0
Code	Factor	
0x0	2.0	
0x1	4.1	
0x2	5.3	
0x3	6.7	
0x4	8.7	
0x5	10.5	
0x6	13.2	
0x7	16.0	
Notes	The effective total gain calculates as: $G_{\text{eff}} = GF0 \times GR0$, respectively $G_{\text{eff}} = 1/4 \times GF0 \times GR0$ if using the input voltage divider (RIN0 = 0x9).	

Table 41: Gain Range CH0

GF0		Adr 0x11, bit 7:3
Code	Factor	
0x00	1.00	
0x01	1.06	
...	$6.25 \frac{GFZ}{31}$	
0x1F	6.25	

Table 42: Fine Gain Factor CH0

Offset Calibration CH0

To calibrate the offset the source of supply must first be selected using VOS0 (see Offset Calibration CH1 and CH2 for further information). For the CH0 path the dependent source VDC is identical to source VDC1.

VOS0		Adr 0x13, bit 5:4
Code	Source	
0x0	0.05 · V(ACO)	
0x1	0.5 V	
0x2	0.25 V	
0x3	VDC (ie. VDC1)	

Table 43: Offset Reference Source CH0

OR0		Adr 0x12, bit 1:0
Code	Range	
0x0	x1	
0x1	x2	
0x2	x6	
0x3	x12	

Table 44: Offset Range CH0

OF0				Adr 0x12, bit 7:2
Code	Factor	Code	Factor	
0x00	0	0x20	0	
0x01	+ 0.0322	0x21	– 0.0322	
...	+ OF0/31	...	– (OF0 - 32)/31	
0x1F	+ 1	0x3F	– 1	

Table 45: Offset Factor CH0

SIGNAL LEVEL CONTROL and SIGNAL MONITORING

Via the controlled sensor current source (pin ACO) iC-MSB can keep the output signals for the ensuing sine/digital converter constant regardless of temperature and aging effects by tracking the sensor supply.

Both the controller operating range and input signal amplitude for the controller are monitored and can be enabled for error messaging. A constant current source can be selected for the ACO output when setting the signal conditioning; the current range for the highside current source is adjusted using ADJ(6:5).

ADJ (6:5) Adr 0x10, bit 5:4	
Code	Function
00	5 mA - Range
01	10 mA - Range
10	25 mA - Range
11	50 mA - Range

Table 46: ACO Output Current Range (applies for control modes and constant current source)

ADJ (8:7) Adr 0x10, bit 7:6	
Code	Function
00	Sine/cosine square control
01	Sum control
10	Constant current source
11	Not permitted (device test only)

Table 47: ACO Output Control Mode

Note: Excessive input signals or internal signal clipping can interfere control operation, so that the preset operating point may not be reached (upon power up) or maintained (upon disturbances). Use Control Error 2 and Signal Error 1 for monitoring and configure EMASKA accordingly.

ADJ (4:0) Adr 0x10, bit 3:0; Adr 0x0F, bit 7	
Code	Square control ADJ(8:7) = 00
0x00	Vpp() approx. 300 mV (60 %)
0x01	Vpp() approx. 305 mV (61 %)
...	... $\approx 300 \text{ mV} \frac{77}{77 - (1.25 * \text{Code})}$
0x19	Vpp() approx. 500 mV (101 %)
...	...
0x1F	Vpp() approx. 600 mV (120 %)

Table 48: Setpoint Square Control (internal sin/cos signal amplitude)

In operation with the active square control mode ADJ(4:0) sets the internal signal amplitudes according to the relation $(\text{PCH1-NCH1})^2 + (\text{PCH2-NCH2})^2$; these should be set to 0.25 Vpk.

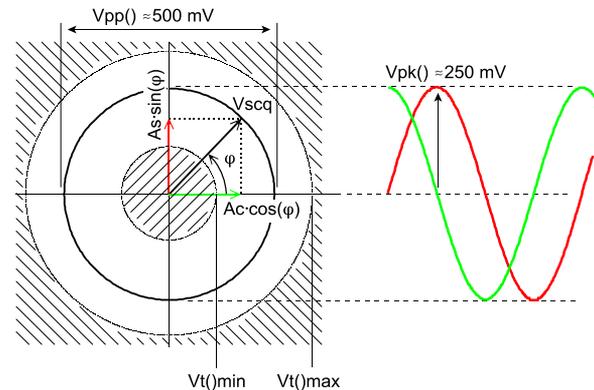


Figure 9: Internal signal monitoring and test signals in Calibration 2 mode (example for ADJ(8:0) = 0x19);

Signal monitoring and limits			
ADJ (4:0)	Vt()min ... max	ADJ (4:0)	Vt()min ... max
0x00	120 mV...390 mV	0x19	200 mV ...650 mV
0x01	122 mV...397 mV
...	...	0x1F	240 mV...780 mV
Notes	All values nominal, see also Elec. Char. Nos. 607, 608		

Table 49: Signal Monitoring

The signal monitoring limits are tracked according to ADJ(4:0) and fit for square control mode. When using sum control mode a different operating point can be required for which the monitoring limits may not be suitable. In this case signal monitoring should be disabled via the error mask (see EMASKA etc.).

ADJ (4:0) Adr 0x10, bit 3:0; Adr 0x0F, bit 7	
Code	Sum control ADJ(8:7) = 01
0x00	VDC1 + VDC2 approx. 245 mV
0x01	VDC1 + VDC2 approx. 249 mV
...	... $\approx 245 \text{ mV} \frac{77}{77 - (1.25 * \text{Code})}$
0x1F	VDC1 + VDC2 approx. 490 mV

Table 50: Setpoint Sum Control (DC value)

ADJ (4:0) Adr 0x10, bit 3:0; Adr 0x0F, bit 7	
Code	Constant current source ADJ(8:7) = 10
0x00	I(ACO) approx. 3.125% Isc(ACO)
0x01	I(ACO) approx. 6.25% Isc(ACO)
...	... $\approx 3.125% * (\text{Code} + 1) * Isc(ACO)$
0x1F	I(ACO) approx. 100% Isc(ACO)
Notes	See Elec. Char. No. 602 for Isc(ACO)

Table 51: Setpoint Current Source (ACO output current)

MONITORING AND ERROR OUTPUT

The following table gives the errors which can both be recognized by iC-MSB and enabled either for messaging, output shutdown or protocol in the EEPROM.

Mask EMASKA stipulates that errors should be signaled at pin ERR, mask EMASKO determines whether the line drivers are to be shutdown or not (with PDMODE defining reactivation) and mask EMASKE governs the storage of error events in the EEPROM.

EMASKA	Addr 0x14, bit 6:0
EMASKO	Addr 0x16, bit 6:0
EMASKE	Addr 0x18, bit 2:0; ADR 0x17, bit 7:4
Bit	Error Event
6*	Configuration error (SDA or SCL pin error, no acknowledge signal from EEPROM or invalid check sum);
5	Excessive temperature warning
4	External system error
3	Control error 2: range at max. limit
2	Control error 1: range at min. limit
1	Signal error 2: clipping
0	Signal error 1: loss of signal (wrong s/c phase, poor differential amplitude, may also result from excessive input signals or internal signal clipping)
EMASKA	Error Mask Alarm Output ERR
1	Enable: event changes state of pin ERR (if EMASKO does not disable the output function).
0	Disable: event does not affect pin ERR.
*Note	EMASKA(6): Pin ERR can not pull low on config. error. Use EPH = 1 for high-active error logic.
EMASKO	Error Mask Driver Shutdown
1	Enable: event resets pin ACO to the 5 mA range, tristates the line driver outputs and pin ERR (i.e. low-active error messages can not be displayed)
0	Disable: output functions remain active
*Note	EMASKO(6) = 1 (ROM bit): The line drivers remain high impedance (tristate) when cycling power. Program EMASKO(6) = 0 to EEPROM. This allows to reactivate disabled output drivers by toggling bit NTRI (set zero, then one). If set 1, the driver shutdown persists and can not be resolved.
EMASKE	Error Mask EEPROM Savings
1	Enable: event will be latched
0	Disable: event will not be latched
*Note	Program EMASKE(6) = 0 to EEPROM. This avoids conflicts with I ² C programming adapters which are not multi-master capable.

Table 52: Error Masking

Error Input/Output: pin ERR

Pin ERR is operated by a current-limited open-drain output driver and has an internal pull-up which can be disabled. The output logic (low or high active) is con-

figured by EPH, and the minimum indication time by EMTD.

Pin ERR also acts as an input for error messages of the external system. This function requires EPH = 0 and an external error being low active. Pin ERR can also switch iC-MSB to test mode, for which a voltage of larger than VTMon must be applied (see page 22).

EPH			Addr 0x15, bit 2
Code	State with error	State w/o error	
0*	active low	high impedance (evaluation of low active external system error)	
1	high impedance (or optional pull-up)	active low	
Note	*) Pin ERR is disabled during driver shutdown and cannot indicate errors in this case.		

Table 53: I/O Logic, Alarm Output ERR

EMTD				Addr 0x15, bit 5:3
Code	Indication Time	Code	Indication Time	
0x0	0 ms	0x4	50 ms	
0x1	12.5 ms	0x5	62.5 ms	
0x2	25 ms	0x6	75 ms	
0x3	37.5 ms	0x7	87.5 ms	

Table 54: Min. Indication Time, Alarm Output ERR

EPU		Addr 0x17, bit 2
Code	Function	
0	No internal pull-up	
1	Internal 300 µA pull-up current source active	

Table 55: Pull-Up Enable, Alarm Output ERR

Excessive Temperature Warning

Exceeding the temperature warning threshold T_w (corresponds to T_2 , refer to Temperature Sensor, page 20) can be signaled at pin ERR or used to shut down the line drivers (via mask EMASKO). The temperature warning is cleared when the temperature falls below $T_w - T_{hys}$.

Note: If the temperature shutdown threshold $T_{off} = T_w + \Delta T$ is exceeded, the line drivers are shut down independently of EMASKO. For ΔT refer to Elec. Char. E06.

Analog Output Drivers Shutdown

PDMODE Addr 0x18, bit 6	
Code	Function
0	Driver shutdown terminates with the error event
1	Permanent driver shutdown until cycling power

Table 56: Driver Activation

Error Protocol

Out of the errors enabled by EMASKE both the first error (under ERR1) and last error (under ERR2) which occur after the iC-MSB is powered up are stored in the EEPROM.

The EEPROM also has a memory area in which all occurring errors can be stored (ERR3). Only the fact that

an error has occurred can be recorded, with no information as to the time and count of appearance of that error given. Error recording can be used to statistically evaluate the causes of system failure, for example.

ERR1 Addr 0x20, bit 6:0	
ERR2 Addr 0x22, bit 0; Adr 0x21, bit 7:2	
ERR3 Addr 0x23, bit 2:0; Adr 0x22, bit 7:4	
Bit	Error Event
9:0	Assignment according to EMASKE
Code	Function
0	No event
1	Registered error event

Table 57: Error Protocol

ANALOG OUTPUT DRIVERS

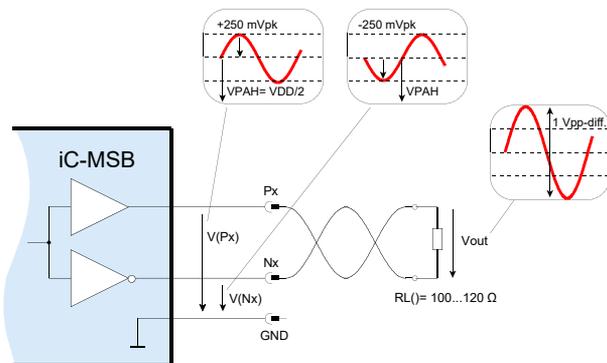


Figure 10: Output amplitude and offset according to Elec. Char. 502 and 503.

iC-MSB outputs differential 1 Vpp signals with approx. 2.5 V in offset onto the transmission cable, which is terminated with 100 Ω or 120 Ω at the receiver end (PLC).

The output drivers are shut down (tristated) in case of excessive temperature (see page 31), or when reverse polarity is detected (see section Reverse Polarity Protection, page 32).

Using EMASKO for error masking, further events can be selected to shut down the output drivers (see Table 52). Using PDMODE, the duration of a shutdown can be prolonged until power was cycled (see Table 56).

If there is no EEPROM or no valid configuration provided on power up, the output drivers will not be enabled.

REVERSE POLARITY PROTECTION

The analog output drivers of iC-MSB are protected against reverse polarity and short-circuiting. A defective or wrongly connected device cable causes no damage, neither to iC-MSB nor to the components protected against reverse polarity by VDDs and GNDS.

The following pins feature reverse polarity protection: PC, NC, PS, NS, PZ, NZ, ERR, VDD, GND and ACO (as long as GNDS is only loaded relative to VDDs). The maximum voltage difference between these pins should not exceed 6 V (8 V for pin ERR).

Reverse polarity is permanently monitored and detected if the voltage at a protected pin undershoots the ground potential at GND.

If the state of reverse polarity is resolved, iC-MSB reboots from the EEPROM and enables the output drivers.

Note: When iC-MSB is linked to a PLC and does not enable its output drivers on power up, a negative line potential could be the root cause. Refer to Application Hints, page 33, for details and recommended countermeasures.

APPLICATION HINTS

Connecting MR sensor bridges for safety-related applications

For safety-related applications iC-MSB^{SAFETY} requires an external overvoltage protection of supply VDD (Zener diode with fuse, for instance) and external pull-down resistors at the inputs X3 to X6 towards GNDS (of up to 100 kΩ).

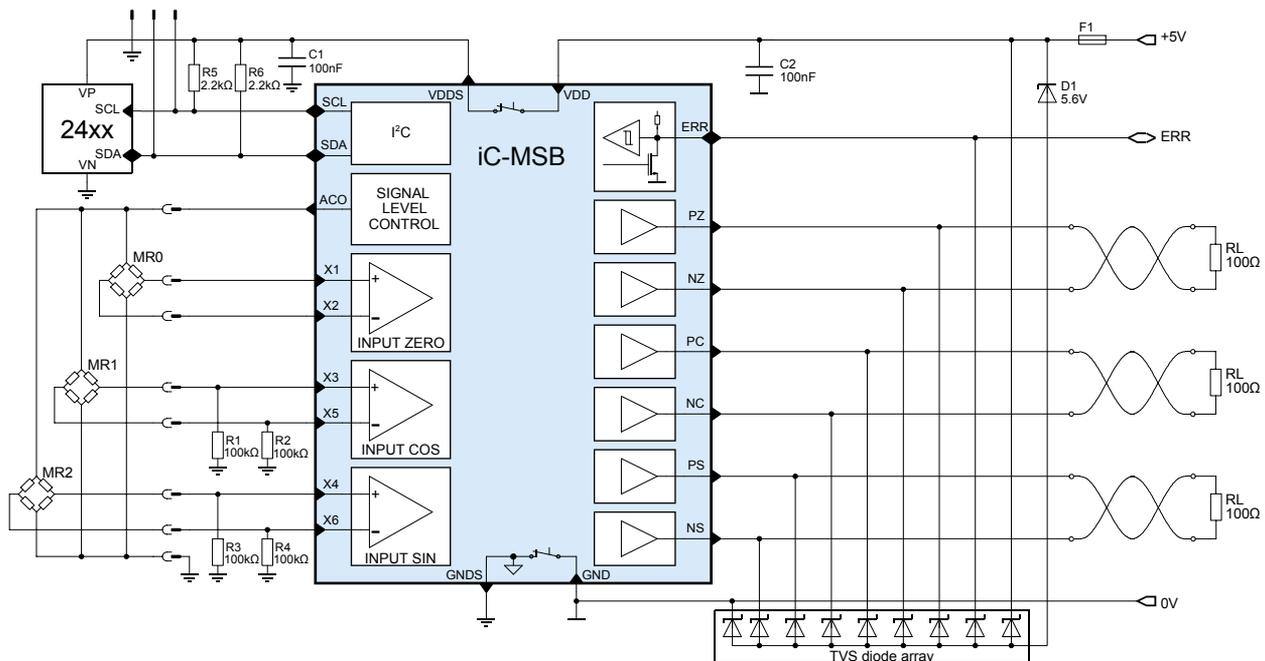


Figure 11: Example circuit for safety-related applications with iC-MSB^{SAFETY}.

PLC Operation

There are PLCs with a remote sense supply which require longer for the voltage regulation to settle. At the same time the PLC inputs can have high-impedance resistances versus an internal, negative supply voltage which define the input potential for open inputs.

In this instance iC-MSB's reverse polarity protection feature can be activated as the outputs are tristate during the start phase and the resistances in the PLC determine the pin potential. During the start phase neither

the supply VDD nor the output pins, which are also monitored, must fall to below ground potential (pin GND); otherwise the device is not configured and the outputs remain permanently set to tristate.

Note: In order to ensure that iC-MSB starts with the PLCs mentioned above pull-up resistors can be used in the encoder. Values of 100 kΩ are usually sufficient; it is, however, recommended that PLC specifications be specifically referred to here.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
F2	2016-09-29	Various	Introduction of QFN32-5x5 package	1, 5-7, 32
		REGISTER MAP	Addr 0x14 to 0x18: Mandatory programming of undescribed bits; Footnote on mandatory programming of specific parameters	15
		SERIAL CONFIGURATION INTERFACE (EEPROM)	EEPROM device address, note on I ² C in-circuit programming	17
		INPUT CONFIGURATION	Figure 2 updated, Table 19: update of footnote, Table 19: update of contents	23
		SIGNAL CONDITIONING CH1, CH2	Table 33: update of contents	27
		SIGNAL CONDITIONING CH0	Table 41: update of contents	29
		ERROR MONITORING AND ALARM OUTPUT	Table 52, 53: update of contents Alarm output: description improved	31
		REVERSE POLARITY PROTECTION	Max. voltage difference: 8 V at pin ERR Note box added	32

Rel.	Rel. Date*	Chapter	Modification	Page
F3	2017-05-02	FEATURES, THERMAL DATA	Operating temperature range (OTR) extended to +125 °C Introduction of OTR for SAFETY applications (Ta_safe)	1, 8
		ELECTRICAL CHARACTERISTICS	Junction temperature range extended to +140 °C Items 107, 301, 302: conditions corrected Items 601, 602: conditions and limits updated	9ff
		ORDERING INFORMATION	Adaption of OTR for TSSOP20-TP, QFN32-5x5, and SAFETY applications	35

Rel.	Rel. Date*	Chapter	Modification	Page
F4	2020-08-19	BLOCK DIAGRAM	Update of block diagram, adaption of section titles	1ff
		DESCRIPTION	Note box added	2
		PACKAGING INFORMATION	Pin configuration figure and footnote updated (value of bypass cap) Package TSSOP20-TP: dimensions added	4
		ELECTRICAL CHARACTERISTICS	Item 001: conditions completed Item D06: min limit changed to -650 µA Items 503, D13 added	9ff
		SERIAL I ² C INTERFACE	Update of description, Figure 1 added, Table 5: note updated, Table 7 added, note and attention boxes added; Section EEPROM Device Selection: Table 8 added, update of description, note boxes added;	17ff
		BIAS SOURCE AND TEMP. SENSOR CALIBRATION	Table 15: formula corrected	20
		ANALOG OUTPUT DRIVERS	Section added	32
		REVERSE POLARITY PROT.	Description updated	32
		ORDERING INFORMATION	Listing updated	35

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ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-MSB ^{SAFETY}	20-pin TSSOP RoHS compliant		iC-MSB TSSOP20
	20-pin TSSOP with Thermal Pad RoHS compliant	Temperature range -40 °C to +125 °C*	iC-MSB TSSOP20-TP
	32-pin QFN, 5 mm x 5 mm, thickness 0.9 mm, RoHS compliant	Temperature range -40 °C to +125 °C*	iC-MSB QFN32-5x5
iC-MSB ^{SAFETY} Evaluation Board			iC-MSB EVAL MSB1D
iC-MSB2	TSSOP20		iC-MSB2 TSSOP20

*) Note that for *SAFETY* applications, the compliant temperature range is -25 to +100 °C.

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