iC-MR3 13-BIT S&H SIN/COS INTERPOLATOR WITH MCU INTERFACE FOR FUNCTIONAL SAFETY

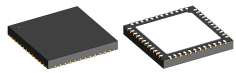
FEATURES

- Triggered 13-bit sine-to-digital conversion within 2 µs
- Precision PGA for diff. and single-ended signals up to 500 kHz
- Voltage or current input mode with signal monitoring
- Adjustable signal conditioning for offset, amplitude, and phase
- Input signal stabilization through LED or MR bridge current control of up to 50 mA
- Serial I/O (SPI, BiSS, SSI) and 8-bit parallel MCU interfaces with separate low-voltage supply of 2.5 V up to 5 V
- Absolute data interface (ADI: BiSS/SSI) for initialization
- For position data of up to 50 bit with adjustable singleturn/multiturn data length
- Position data preset using ST/MT offset registers
- 12-bit A/D converter for temperature sensing
- Special functions for safety applications (signal monitoring, sign-of-life counter, and extended CRC)
- Current-limited, differential 1 Vpp sine/cosine outputs to 100 Ω
- Device configurable through I/O interfaces or a serial EEPROM
- Single-sided 5 V operation from -40 to +125 °C
- Approved for safety applications (e.g. using iC-RZ Series)

APPLICATIONS

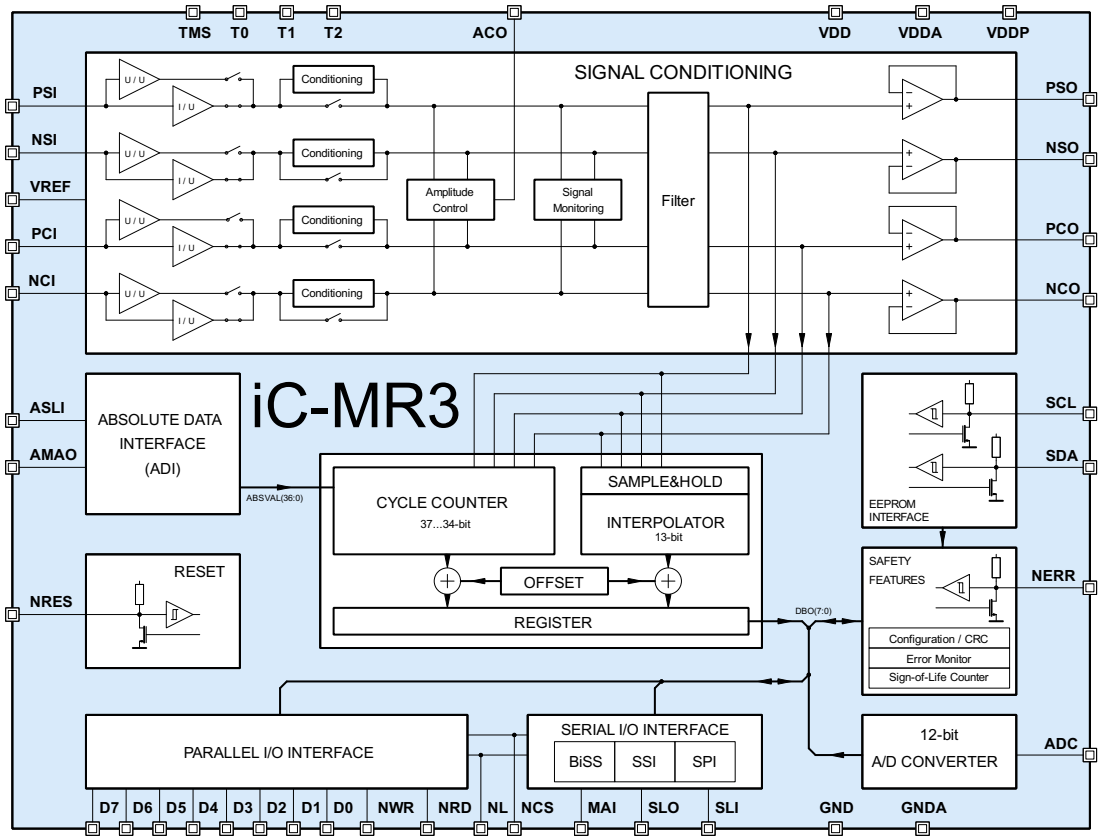
- High-resolution encoders for motor feedback
- Safe motion control with redundant sensing for safe position and safe speed

PACKAGES



48-pin QFN
7 mm x 7 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

The iC-MR3 is a universal sine-to-digital converter with signal conditioning and various interfaces for configuration and data communication. The Microcontrollers can be connected through a parallel I/O interface with an 8-bit bus width (12.5 MHz) or using a serial I/O interface (4-pin SPI, 10 MHz). The serial I/O interface can function as a sensor interface either using the BiSS C protocol (up to 10 MHz, bidirectional) or SSI protocol (up to 4 MHz).

In the analog signal path the iC-MR3 has precision input amplifiers with an adjustable gain for differential or referenced voltage signals of 10 mV peak to 1 V peak or for current signals of approx. 10 µA to 300 µA (input pins PSI, NSI, PCI, and NCI). A separate measurement input (VREF) enables signals to be referenced to the sensor's reference voltage.

The following signal conditioning unit can compensate for typical sine/cosine sensor signal errors, such as offset, amplitude, and phase errors. The conditioned signals are filtered and output through analog line drivers with an amplitude of typically 250 mV (output pins PSO, NSO, PCO, and NCO). A differential 1 Vpp signal to 100 Ω is available for line transmission.

A control signal is gained from the conditioned signals to stabilize the sine/cosine output signals. This can adjust the transmitting LED of optical encoder systems using the integrated 50 mA driver stage (output ACO). With magnetic sensors, this driver output supplies the MR sensor bridges and/or measures the bridge's supply voltage. By tracking the sensor supply, sensor temperature and ageing effects are compensated for, the input signals are stabilized, and precise calibration of the input signals is maintained. This makes a constant interpolation accuracy possible across the entire operating temperature range.

At the same time, the sensor is monitored to see whether it is functioning properly. The amplitude and offset of the input signals at pins PSI, NSI, PCI, and NCI are checked, enabling wire-breakage or short circuits to be detected. The control unit operating limits are also monitored so that an alarm can be signaled through the I/O interface and/or at error output NERR, when the brightness of the LED falls below a configurable value. This could be caused by a build up of dust or ageing of the optical system.

The sine-to-digital conversion is performed by a fast interpolator with a sample-&-hold circuit which resolves a sine cycle with 13 bits either continuously or on request. In parallel and independent of the interpolator, a configurable 37-bit cycle counter logs the sine and cosine zero crossings. This cycle counter is programmable and can take its start value from the serial absolute data interface (ADI); the corresponding interface master operates either using the BiSS C or the SSI protocol.

For position measurement applications, the iC-MR3 differentiates between multiturn and singleturn data using a selectable intersection on the cycle counter. The position can be corrected accordingly using the multiturn and singleturn offset values.

An integrated 12-bit A/D converter digitizes linear measurement voltages at pin ADC for the evaluation of KTY or PT1000 temperature sensors, for example. Measurement of the calibratable converter is observed by settable threshold values so that a permissible operating temperature range with a lower and upper temperature threshold can be monitored.

After power-on, the iC-MR3 collects its CRC protected configuration data from an external I^2C-EEPROM or waits for the configuration from one of the I/O interfaces. An undervoltage reset zeroes internal registers and is shown as a reset pulse at pin NRES, which also serves as a low-active reset input.

Errors can always be masked and allocated to an error bit (and displayed at the error message output NERR) or a warning bit. The internal status registers are available to the I/O interfaces which have a number of different commands (software reset, memory verification, and error simulation).

Safety Applications
The iC-MR3 is TUEV-verified for safety applications up to SIL 3 according to IEC 61508 and PL e, Cat. 3 according to ISO 13849-1. The instructions of the associated safety manual and referenced documents have to be considered.

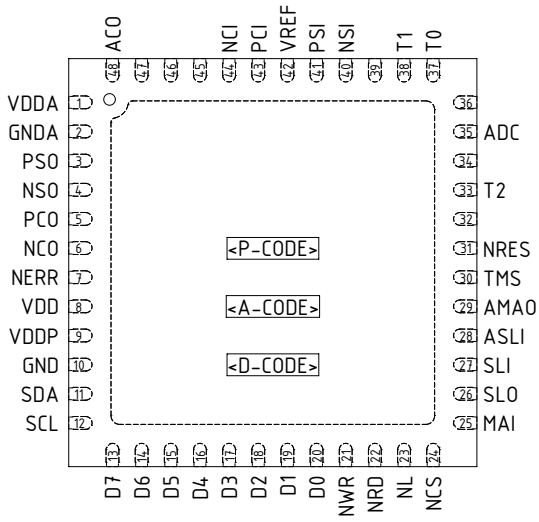
General notice on application-specific programming
Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

For optical sensor systems: The chip's performance in application is impacted by system conditions like the quality of the optical target, the illumination, temperature and mechanical stress, sensor alignment and initial calibration.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION QFN48-7x7 (topview)



PIN FUNCTIONS

No.	Name	Function
1	VDDA	+5 V Analog Supply Voltage
2	GNDA	Analog Ground
3	PSO	Sine Output
4	NSO	Inverted Sine Output
5	PCO	Cosine Output
6	NCO	Inverted Cosine Output
7	NERR [2]	Error Signal, input/indication output
8	VDD	+5 V Digital Supply Voltage
9	VDDP	+2.5 V....+5 V Dig. I/O Supply Voltage
10	GND	Digital Ground
11	SDA	EEPROM Interface, data line I²C
12	SCL	EEPROM Interface, clock line I²C
13	D7 [3]	Par. Interface, data line / Status INIT
14	D6 [3]	Par. Interface, data line / Status ERR
15	D5 [3]	Par. Interface, data line / Status WARN
16	D4 [3]	Par. Interface, data line / Status EWKH

PIN FUNCTIONS

No.	Name	Function
17	D3 [3]	Par. Interface, data line / Status EWKL
18	D2 [3]	Par. Interface, data line / Status BUSY
19	D1 [3]	Par. Interface, data line / Status ADV
20	D0 [3]	Par. Interface, data line / Status PDV
21	NWR [2]	Par. Interface, write signal
22	NRD [2]	Par. Interface, read signal
23	NL [2]	Par./Serial Interf., storage signal
24	NCS [2]	Par./Serial Interf., chip select (NCS)
25	MAI	Serial Interface, clock input (SCLK)
26	SLO	Serial Interface, data output (MISO)
27	SLI	Serial Interface, data input (MOSI)
28	ASLI	Absolute Data Interface, data input
29	AMAO	Absolute Data Interface, clock output
30	TMS [4]	Test Mode Selection Input
31	NRES [2,7]	Reset Signal, input/indication output
32	n.c. [1]	
33	T2	Test Pin
34	n.c.	
35	ADC	12-bit ADC Input, temperature sensor
36	n.c.	
37	T0 [4]	Test Pin
38	T1 [4]	Test Pin
39	n.c.	
40	NSI	Inverted Sine Input
41	PSI	Sine Input
42	VREF	Reference Voltage, input/output (use is optional)
43	PCI	Cosine Input
44	NCI	Inverted Cosine Input
45	n.c.	
46	n.c.	
47	n.c.	
48	ACO	Amplitude Control, high-side current source output
	BP [6]	Backside Paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes); dashed lines are used for visible or hidden outlines.

[1] Pin numbers marked n.c. are not connected.

[2] Pin is low active.

[3] Pin outputs the status register during serial I/O interface modes.

[4] It is generally recommended to connect unused inputs to GNDA, with the exception of pin TMS (leave open or connect VDDP).

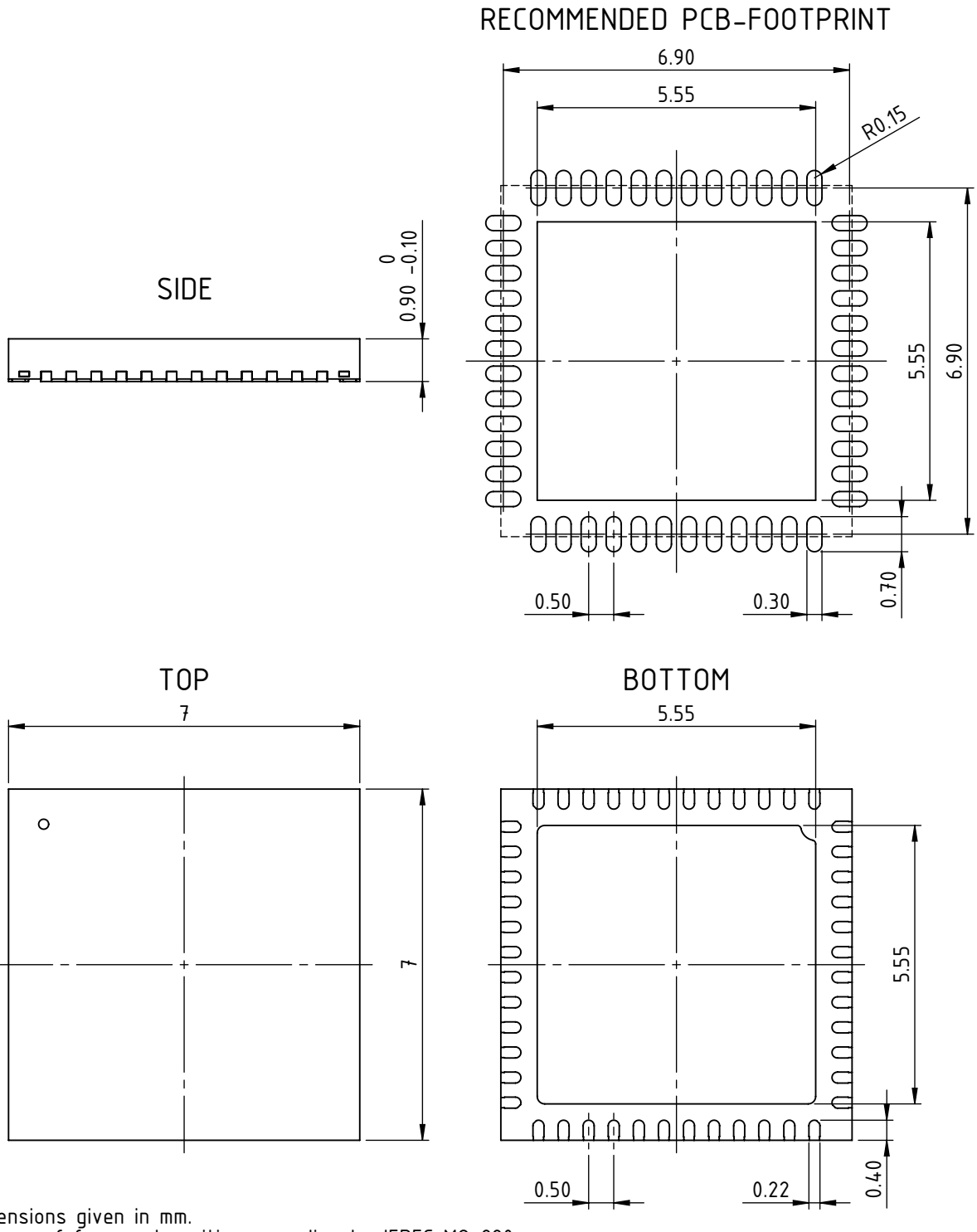
[5] To calibrate the chip's bias current use a pull-down resistor of 10 kΩ ±1 % connected from pin NCO to GNDA (see page 24).

[6] To improve the heat dissipation connect the backside paddle to an extended copper area connected to GNDA. Avoid any current flow across the paddle. The heat distribution can be supported by connecting further PCB layers using *thermal vias*. If those need to be placed below the paddle, prefer blind vias.

[7] A low at NRES causes a high at SCL, SDA, D(7:0), NERR (I/O's with internal pull-up), a high at AMAO (push-pull clock outp.), and high impedance of SLO.

PACKAGE DIMENSIONS

Note: QFN48-7x7 package version with reduced thickness.



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

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ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V(VDDA)	Voltage at VDDA		-0.3	6	V
G002	V(VDD)	Voltage at VDD		-0.3	6	V
G003	V(VDDP)	Voltage at VDDP		-0.3	6	V
G004	V()	Voltage at ACO, ADC, PSO, NSO, PCO, NCO, PSI, NSI, VREF, PCI, NCI, T0, T1		-0.3	VDDA +0.3	V
G005	V()	Voltage at SDA, SCL, NERR, NRES, D(7...0), NWR, NRD, NL, NCS, MAI, SLO, SLI, ASLI, AMAO, TMS		-0.3	VDDP +0.3	V
G006	V()	Voltage at T2		-0.3	VDD +0.3	V
G007	I(VDDA)	Current in VDDA		-100	400	mA
G008	I(VDD)	Current in VDD		-100	100	mA
G009	I(VDDP)	Current in VDDP		-100	100	mA
G010	I()	Current in PSO, NSO, PCO, NCO		-20	20	mA
G011	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ, all pins relative to GNDA		2	kV
G012	Ptot	Permissible Power Dissipation			500	mW
G013	Tj	Junction Temperature		-40	150	°C

THERMAL DATA

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	QFN48-7x7 soldered to PCB according to JEDEC 51	-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN48-7x7 soldered to PCB according to JEDEC 51		30		K/W
T03	Ts	Storage Temperature	QFN48-7x7	-40		150	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDDA, VDD	Permissible Supply Voltage		4.5	5	5.5	V
002	I(VDDA)	VDDA Supply Current			25	35	mA
003	I(VDD)	VDD Supply Current			8	15	mA
004	VDDP	Permissible Dig. Supply Voltage		2.375		VDD	V
005	I(VDDP)	VDDP Supply Current	no load at I/O interface pins		1		mA
006	Vc()hi	Clamp Voltage hi at digital inputs ASLI, SLI, MAI, NCS, NL, NRD, NWR, NRES, NERR, SDA, SCL, TMS	Vc()hi = V() - V(VDDP), I() = 4 mA	0.3		1.2	V
007	Vc()hi	Clamp Voltage hi at digital inputs D(7...0)	Vc()hi = V() - V(VDDP), I() = 1.6 mA	0.3		1.2	V
008	Vcz()hi	Clamp Voltage hi at ACO, VDDA, PSO, NSO, PCO, NCO, AMAO, SLO, ADC, PSI, NSI, VREF, PCI, NCI	I() = 4 mA			11	V
009	Vc()lo	Clamp Voltage lo at ACO, VDDA, PSO, NSO, PCO, NCO, AMAO, SLO, ADC, PSI, NSI, VREF, PCI, NCI	I() = -4 mA	-1.2		-0.3	V
Bias Current Source, Reference Voltages, Input/Output VREF							
101	IBP	Bias Current Source	IBP calibrated to 200 µA	92.5	100	107.5	%
102	VPAH	Reference Voltage VPAH	relative to GNDA	45	50	55	%VDDA
103	V05	Reference Voltage V05		450	500	570	mV
104	VREFI	Internal Ref. Voltage VREFI	DCPOS = 1 DCPOS = 0	1.35 2.25	1.5 2.5	1.65 2.75	V V
105	Vin()	Permissible Input Voltage $VREF_{ex}$ at VREF	SELREF = 0x3	0.5		VDDA − 2	V
106	Rin()	Input Resistance at VREF	SELREF = 0x3, REFVOS = 0x3, UIN = 1, TUIN = 0, Rin() relative to VREFin()	20	26	30	kΩ
107	Vref()out	Output Voltage at VREF	SELREF = 0x2, I() = 0		100		%VREFI
108	I0()	Leakage Current at VREF	SELREF = 0x0 or 0x1	-1		+1	µA
12-bit A/D Converter, Measuring Input ADC							
601	Vin()max	Permissible Input Voltage		0		VDDA	V
602	Vin()FS	Maximum Full Scale Input Voltage	ADCSLOP = 0xFF ADCSLOP = 0x00		2.5 2.0		V V
603	RESOadc	Converter Resolution			12		bit
604	tp()adc	Conversion Time			1.1		ms
605	I0()adc	Leakage Current		-100		+100	nA
606	INL()adc	Integral Nonlinearity	after calibration			±10	LSB
607	ΔINL()adc	INL Temperature Drift			±2		LSB/K
Signal Conditioning, Inputs: PSI, NSI, PCI, NCI							
701	Vin()sig	Permissible V-Mode Input Voltage	UIN = 1, TUIN = 0 (V-Mode 1:1) UIN = 1, TUIN = 1, DCPOS = 1 (V-Mode 4:1)	0.75 -0.1		VDDA − 1.5 VDDA + 0.1	V V V V
702	Iin()	V-Mode Input Current	UIN = 1, TUIN = 0 (V-Mode 1:1)	-100		100	nA
703	Rin()	V-Mode Input Resistance	relative to VREFin, UIN = 1, TUIN = 1; Tj = 27 °C (V-Mode 4:1)	15.0 16.4	20	28.5 23.6	kΩ kΩ
704	Iin()sig	Permissible I-Mode Input Current	UIN = 0, DCPOS = 0 UIN = 0, DCPOS = 1	-300 10		-10 300	µA µA
705	CTR()sig	Permissible Signal Contrast Ratio	current ratio of Iin()pkpk to Iin()dc	0.125		1	

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
706	Rin()	I-Mode Input Resistance	relative to VREFin, Tj = 27 °C; UIN = 0, RIN = 00 UIN = 0, RIN = 01 UIN = 0, RIN = 10 UIN = 0, RIN = 11	 1.2 1.8 2.6 3.8	 1.7 2.4 3.3 4.7	 2.5 3.4 4.6 6.4	 kΩ kΩ kΩ kΩ
707	R2()	I-Mode Conversion Resistor	Tj = 27 °C; UIN = 0, RIN = 00 UIN = 0, RIN = 01 UIN = 0, RIN = 10 UIN = 0, RIN = 11 UIN = 1, TUIN = 1 (V-Mode 4:1)		 1.6 2.3 3.2 4.6 5.0		 kΩ kΩ kΩ kΩ kΩ
708	TC(Rin)	Temperature Coefficient of Rin			0.15		%/K
709	Vin()os	V-Mode Input Offset Voltage	relative to side of input (V-Node 1:1); GR = 0x4, GFC = 0x7C0, GFS = 0x7C0			±300	µV
710	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(PSI) – V(NSI), Vin()diff = V(PCI) – V(NCI) respectively; TUIN = 0 (V-Mode 1:1) TUIN = 1 (V-Mode 4:1)	 20 80		 1000 4000	 mVpp mVpp
711	Vcore()	Recommended Internal Signal Level	G * Vin()diff, MODE = 0x01		6		Vpp
712	GF, GC	Selectable Gain Factors	TUIN = 0 TUIN = 1	2 0.5		100 25	
713	ΔGFdiff	Differential Gain Accuracy	refer to fine gain (GFS, GFC)	-1		1	LSB
714	ΔGFabs	Absolute Gain Accuracy	refer to fine gain (GFS, GFC), guaranteed range of monotonicity	-20		20	LSB
715	ΔGRabs	Gain Accuracy	refer to coarse gain (GR)	-8		8	%
716	VOScal1	Offset Calibration Range	measured at output, source V(ACO) = 3 V, REFVOS = 00, MODE =0x01; ORS, ORC = 00 ORS, ORC = 01 ORS, ORC = 10 ORS, ORC = 11		 ±450 ±900 ±2700 ±5400		 mV mV mV mV
717	VOScal2	Offset Calibration Range	measured at output, source V05, REFVOS = 01, MODE = 0x01; ORS, ORC = 00 ORS, ORC = 01 ORS, ORC = 10 ORS, ORC = 11		 ±1500 ±3000 ±9000 ±18000		 mV mV mV mV
718	VOScal3	Offset Calibration Range	measured at output, source V025, REFVOS = 10, MODE = 0x01; ORS, ORC = 00 ORS, ORC = 01 ORS, ORC = 10 ORS, ORC = 11		 ±750 ±1500 ±4500 ±9000		 mV mV mV mV
719	VOScal4	Offset Calibration Range	measured at output, source VDC = 125 mV, REFVOS = 11, MODE = 0x01; ORS, ORC = 00 ORS, ORC = 01 ORS, ORC = 10 ORS, ORC = 11		 ±375 ±750 ±2250 ±4500		 mV mV mV mV
720	ΔVOSdiff	Differential Linearity Error of Offset Correction		-0.5		0.5	LSB
721	ΔVOSint	Integral Linearity Error of Offset Correction		-100		100	LSB
722	PHIcal	Phase Correction Range	relative to sine signal to cosine signal		±10.4		°
723	ΔPHIdiff	Differential Linearity Error of Phase Correction		-0.25		0.25	LSB
724	ΔPHIint	Integral Linearity Error of Phase Correction		-20		20	LSB

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
725	fin()max	Permissible Input Frequency	angle accuracy better than 8 bit	500			kHz
726	fhc()	Input Amplifier Cutoff Frequency (-3 dB)		250			kHz
Amplitude Control, Output ACO							
801	Vs()hi	Saturation Voltage hi	Vs()hi = VDD − V(); ACOR = 00, I() = -5 mA ACOR = 01, I() = -10 mA ACOR = 10, I() = -25 mA ACOR = 11, I() = -50 mA			 1 1 1.15 1.25	 V V V V
802	Isc()hi	Short-Circuit Current hi in ACO	V() = 0 V ... VDD − Vs()hi; ACOR = 00 ACOR = 01 ACOR = 10 ACOR = 11	 -10 -20 -50 -100		 -5 -10 -25 -50	 mA mA mA mA
803	tr()	Rise Time Current Source ACO	I(ACO): 0 % → 90 % of setpoint		1		ms
804	tset()	Settling Time Current Source ACO	square control active, I(ACO): 50 % → 100 % of setpoint		400		µs
805	Vscq()	Regulated Mean Target Amplitude with Square Control	Vscq() = Vpp(V(PSO) - V(NSO)), Vscq() = Vpp(V(PCO) - V(NCO)) respectively; Tj() = 27°C, ACOC = 0x19		 500		 mV
806	Vdc()	Regulated Mean Setpoint with Sum Control	ACOD = 0x00 ACOD = 0x7F		166 551		mV mV
807	It()min	Monitoring of ACO Output Current, lower threshold	refer to current range ACOR		3		%Isc
808	It()max	Monitoring of ACO Output Current, upper threshold	refer to current range ACOR		90		%Isc
809	Vt()min	Monitoring of Signal Level 1, lower threshold	relative to Vscq()		40		%
810	Vt()max	Monitoring of Signal Level 2, upper threshold	relative to Vscq()		135		%
Signal Filter							
901	fc()	Cut-off Frequency	ENF = 1, SELBP = 1; fin < 10 Hz fin > 100 kHz		15 2400		kHz kHz
902	PHI()	Output-to-Input Phase Lag	ENF = 1, SELBP = 1, fin = 100 kHz for sine and cosine		1.5		°
Sin/Cos Output Drivers PSO, NSO, PCO and NCO							
A01	Vpk()max	Permissible Maximum Output Amplitude	VDDA = 4.5 V, DC level VDDA/2, RL = 50 Ω vs. VDDA/2			300	mV
A02	Vpk()	Output Amplitude with Sensor Tracking by Output ACO	Vpk() calibrated to 250 mV	225	250	275	mV
A03	fc	Cut-off Frequency	CL = 250 pF	500			kHz
A04	Vos	Output Offset Voltage			±200		µV
A05	Isc()hi	Short-Circuit Current hi	V() = 0 V	-40	-20	-15	mA
A06	Isc()lo	Short-Circuit Current lo	V() = VDD	15	20	40	mA
A07	SR()	Slew Rate	RLdiff = 100 Ω, CL = 25 pF		5		V/µs
A08	Rout()	Test Signal Source Resistance	MODE = 0x01 (Analog 1)		5		kΩ
A09	fout()cal	Permissible Test Signal Output Frequency	MODE = 0x01 (Analog 1), CL = 200 pF			2	kHz
Signal Monitoring							
B01	fin()	Signal Monitoring Frequency Range	DC level monitoring amplitude monitoring by Lissajous figure	0 0		500 100	kHz kHz
B02	ΔPHI	Phase Error Tolerance	fin() = 0 ... 100 kHz fin() = 1 kHz, signal of 1 Vpp	±7	 ±30		° °

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B03	Vpp()max	AC Level Monitoring, upper threshold	relative to target amplitude of analog output, see Fig. 14; ΔPHI = 0 (phase | 90°|), $(V(PSIN-NSIN))^2 + (V(PCOS-NCOS))^2$ > Vpp()max for at least 5 µs	110	130	150	%Vpp
B04	Vpp()min	AC Level Monitoring, lower threshold	relative to target amplitude of analog output, see Fig. 14; ΔPHI = 0 (phase | 90°|), $(V(PSIN-NSIN))^2 + (V(PCOS-NCOS))^2$ < Vpp()min for at least 5 µs	30	45	60	%Vpp
B05	Vpp()hys	AC Level Monitoring, Hysteresis	relative to Vpp()min, Vpp()max		30		mV
B06	Vdc()max	DC Level Monitoring, upper threshold	relative to analog output, see Fig. 13	120	125	140	%VPAH
B07	Vdc()min	DC Level Monitoring, lower threshold	relative to analog output, see Fig. 13	50	70	80	%VPAH
Sample & Hold-Stage and 13-bit Interpolator							
C01	t_{IPO}	Conversion Time	ACQMODE = 00			2	µs
C02	AAabs	Absolute Conversion Accuracy	Vpk() = 250 mV		2		LSB
Reset Input / Reset Indication Output NRES							
K01	VDDon	VDD Turn-on Threshold	increasing voltage at VDD relative to GND	3.4		4.3	V
K02	VDDoff	VDD Turn-off Threshold (undervoltage reset)	decreasing voltage at VDD relative to GND	3.0		4.0	V
K03	VDDhys	VDD Hysteresis	VDDhys = VDDon - VDDoff	400			mV
K04	$Vt()hi_{TTL}$	Input Threshold Voltage hi	TTL compatibility: VDDP = 2.375 ... 5.5 V			2	V
K05	$Vt()lo_{TTL}$	Input Threshold Voltage lo	TTL compatibility: VDDP = 2.375 ... 5.5 V	0.8			V
K06	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi - Vt()lo	50	100		mV
K07	$Vt()hi_{CMOS}$	Input Threshold Voltage hi	CMOS compatibility: VDDP = 3.0 ... 3.6 V CMOS compatibility: VDDP = 2.375 ... 3.0 V			70 85	%VDDP %VDDP
K08	$Vt()lo_{CMOS}$	Input Threshold Voltage lo	CMOS compatibility: VDDP = 2.375 ... 3.6 V	30			%VDDP
K09	Ipu()	Pull-up Current		-750	-300	-60	µA
K10	Vs()lo	Output Saturation Voltage lo	I() = 4 mA			400	mV
K11	Isc()lo	Output Short-Circuit Current lo	V() = 0.4 V...VDDP	4		80	mA
Oscillator							
M01	fosc	Internal Oscillator Frequency		12	14	18	MHz
EEPROM Interface SCL, SDA							
N01	Vs()lo	Saturation Voltage lo	I() = 4 mA			400	mV
N02	Isc()	Short-Circuit Current lo		4		80	mA
N03	$Vt()hi_{TTL}$	Input Threshold Voltage hi	TTL compatibility: VDDP = 2.375 ... 5.5 V			2	V
N04	$Vt()lo_{TTL}$	Input Threshold Voltage lo	TTL compatibility: VDDP = 2.375 ... 5.5 V	0.8			V
N05	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi - Vt()lo	50	100		mV
N06	$Vt()hi_{CMOS}$	Input Threshold Voltage hi	CMOS compatibility: VDDP = 2.375 ... 3.6 V			70	%VDDP
N07	$Vt()lo_{CMOS}$	Input Threshold Voltage lo	CMOS compatibility: VDDP = 2.375 ... 3.6 V	30			%VDDP
N08	Ipu()	Input Pull-up Current	V() = 0 V...VDDP - 1 V	-750	-300	-60	µA
N09	Vpu()	Input Pull-up Voltage	Vpu() = VDDP - V(), I() = -5 µA			0.4	V
N10	fclk()	Clock Frequency at SCL		100	120	140	kHz
N11	tbusy()cfg	Duration of Configuration Phase	IBP not adjusted; without EEPROM EEPROM access without I^2C read error EEPROM access with I^2C read error		0.5 5 15	1 6 18	ms ms ms
Serial I/O Interface MAI, SLO, SLI							
O01	$Vt()hi_{TTL}$	Inp. Threshold Volt. hi SLI, MAI	TTL compatibility: VDDP = 2.375 ... 5.5 V			2	V
O02	$Vt()lo_{TTL}$	Inp. Threshold Volt. lo SLI, MAI	TTL compatibility: VDDP = 2.375 ... 5.5 V	0.8			V
O03	Vt()Hys	Hysteresis at SLI, MAI	Vt()hys = Vt()hi - Vt()lo	50	100		mV

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
O04	$Vt()hi_{CMOS}$	Inp. Threshold Volt. hi SLI, MAI	CMOS compatibility: VDDP = 2.375 ... 3.6 V			70	%VDDP
O05	$Vt()lo_{CMOS}$	Inp. Threshold Volt. lo SLI, MAI	CMOS compatibility: VDDP = 2.375 ... 3.6 V	30			%VDDP
O06	Ipu()	Pull-up Current at MAI		-100	-50	-10	µA
O07	Ipd()	Pull-down Current at SLI	NPD_SLI = 0	10	20	100	µA
O08	fclk()	Permissible Clock Frequency at MAI	SSI protocol BiSS C protocol SPI protocol	0.08 0.08		4 10 10	MHz MHz MHz
O09	$t_{out}()$	Slave Timeout at SLO	related to the clock timing, refer to Fig. 5 to 8; NTOA = 1 (fixed) NTOA = 0 (adaptive)	2/fosc	300/fosc t_{init} + 4/fosc	300/fosc	
O10	Vs()hi	Saturation Voltage hi at SLO	Vs()hi = VDDP - V(), I() = -4 mA; VDDP = VDD VDDP = 2.375 V			400 550	mV mV
O11	Vs()lo	Saturation Voltage lo at SLO	I() = 4 mA			400	mV
O12	Isc()hi	Short-circuit Current hi at SLO	V() = 0 V...VDDP - 0.4 V	-90		-4	mA
O13	Isc()lo	Short-circuit Current lo at SLO	V() = 0.4 V...VDDP	4		80	mA
Parallel I/O Interface D(7...0), NWR, NRD, NL, NCS							
P01	$Vt()hi_{TTL}$	Input Threshold Voltage hi	TTL compatibility: VDDP = 2.375 ... 5.5 V; D(7...0) as input			2	V
P02	$Vt()lo_{TTL}$	Input Threshold Voltage lo	TTL compatibility: VDDP = 2.375 ... 5.5 V; D(7...0) as input	0.8			V
P03	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi - Vt()lo; D(7...0) as input	50	100		mV
P04	$Vt()hi_{CMOS}$	Input Threshold Voltage hi	CMOS compatibility: VDDP = 2.375 ... 3.6 V; D(7...0) as input			70	%VDDP
P05	$Vt()lo_{CMOS}$	Input Threshold Voltage lo	CMOS compatibility: VDDP = 2.375 ... 3.6 V; D(7...0) as input	30			%VDDP
P06	Ipu()	Pull-up Current at D(7...0)		-100	-50	-10	µA
P07	Ipu()	Pull-up Current at NWR, NRD, NL, NCS		-100	-50	-10	µA
P08	Vs()hi	Saturation Voltage hi at D(7...0) Outputs	Vs()hi = VDDP - V(), I() = -1.6 mA VDDP = VDD VDDP = 2.375 V			400 550	mV mV
P09	Vs()lo	Saturation Voltage lo at D(7...0) Outputs	I() = 1.6 mA			400	mV
P10	Isc()hi	Short-circuit Current hi at D(7...0) Outputs	V() = 0 V...VDDP - 0.4 V	-50		-1.6	mA
P11	Isc()lo	Short-circuit Current lo at D(7...0) Outputs	V() = 0.4 V...VDDP	1.6		50	mA
Absolute Data Interface ASLI, AMAO							
Q01	$Vt()hi_{TTL}$	Inp. Threshold Volt. hi at ASLI	TTL compatibility: VDDP = 2.375 ... 5.5 V			2	V
Q02	$Vt()lo_{TTL}$	Inp. Threshold Volt. lo at ASLI	TTL compatibility: VDDP = 2.375 ... 5.5 V	0.8			V
Q03	Vt()hys	Hysteresis at ASLI	Vt()hys = Vt()hi - Vt()lo	50	100		mV
Q04	$Vt()hi_{CMOS}$	Inp. Threshold Volt. hi at ASLI	CMOS compatibility: VDDP = 2.375 ... 3.6 V			70	%VDDP
Q05	$Vt()lo_{CMOS}$	Inp. Threshold Volt. lo at ASLI	CMOS compatibility: VDDP = 2.375 ... 3.6 V	30			%VDDP
Q06	Ipu()	Pull-up Current at ASLI		-100	-50	-10	µA
Q07	Vs()hi	Saturation Voltage hi at AMAO	Vs()hi = VDDP - V(), I() = -4 mA VDDP = VDD VDDP = 2.375 V			400 550	mV mV
Q08	Vs()lo	Saturation Voltage lo at AMAO	I() = 4 mA			400	mV
Q09	Isc()hi	Short-circuit Current hi at AMAO	V() = 0 V...VDDP - 0.4 V	-90		-4	mA
Q10	Isc()lo	Short-circuit Current lo at AMAO	V() = 0.4 V...VDDP	4		80	mA

ELECTRICAL CHARACTERISTICS

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Q11	fc1(), fc2()	Clock Frequency at AMAO	GET_ADI = 0, SSI_ADI = 1 (SSI protocol) SLOW_ADI = 0 SLOW_ADI = 1 GET_ADI = 0, SSI_ADI = 0 (BiSS C protocol) SLOW_ADI = 0 SLOW_ADI = 1		 1/16 1/64 1/2 1/8		 fosc fosc fosc fosc
Error Signal Input/Output NERR							
R01	Vt()hi$_{TTL}$	Input Threshold Voltage hi	TTL compatibility: VDDP = 2.375 ... 5.5 V			2	V
R02	Vt()lo$_{TTL}$	Input Threshold Voltage lo	TTL compatibility: VDDP = 2.375 ... 5.5 V	0.8			V
R03	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi - Vt()lo	50	100		mV
R04	Vt()hi$_{CMOS}$	Input Threshold Voltage hi	CMOS compatibility: VDDP = 2.375 ... 3.6 V			70	%VDDP
R05	Vt()lo$_{CMOS}$	Input Threshold Voltage lo	CMOS compatibility: VDDP = 2.375 ... 3.6 V	30			%VDDP
R06	Ipu()	Pull-up Current		-750	-300	-60	µA
R07	Vs()lo	Saturation Voltage lo	I() = 4 mA			400	mV
R08	Isc()lo	Short-circuit Current lo	V() = 0.4 V...VDDP	4		80	mA

OPERATING REQUIREMENTS: Absolute Data Interface (ADI)

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
BiSS Protocol (SSI_ADI = 0)						
I001	t_C	Clock Period	refer to Elec. Char. M01, SLOW_ADI = 0 SLOW_ADI = 1	$2/f_{osc}$ $8/f_{osc}$		
I002	t_{L1}, t_{L2}	Clock Signal Hi/Lo Level Duration		50		% t_C
I003	t_{busy}	Permissible Processing Time	relative to clock period		1021	t_C
I004	t_{P0}	Permissible Propagation Delay (Line Delay Compensation)	not featured (data is captured on next rising clock edge)	0	t_C - t_S	
I005	Δt_P	Permissible Propagation Delay Variance	not featured (refer to t_S and t_H)			% t_C
I006	t_S	Setup Time: Data stable before clock edge lo → hi	without line delay compensation (t_{P0} = 0)	50		ns
I007	t_H	Hold Time: Data stable after clock edge lo → hi	without line delay compensation (t_{P0} = 0)	10		ns
I008	t_{out}	Permissible Slave Timeout		t_C	40	µs
I009	t_{frame}	Clock Frame Repetition	CYC_ADI = 1, refers to Elec. Char. M01	$8192/f_{osc}$		
SSI Protocol (SSI_ADI = 1)						
I010	t_C	Clock Period	refer to Elec. Char. M01, SLOW_ADI = 0 SLOW_ADI = 1	$16/f_{osc}$ $64/f_{osc}$		
I011	t_{L1}, t_{L2}	Clock Signal Hi/Lo Level Duration		50		% t_C
I012	t_S	Setup Time: Data stable before clock edge lo → hi		50		ns
I013	t_H	Hold Time: Data stable after clock edge lo → hi		10		ns
I014	t_{out}	Permissible Slave Timeout		t_C	40	µs
I015	t_{frame}	Clock Frame Repetition	CYC_ADI = 1, refers to Elec. Char. M01	$8192/f_{osc}$		

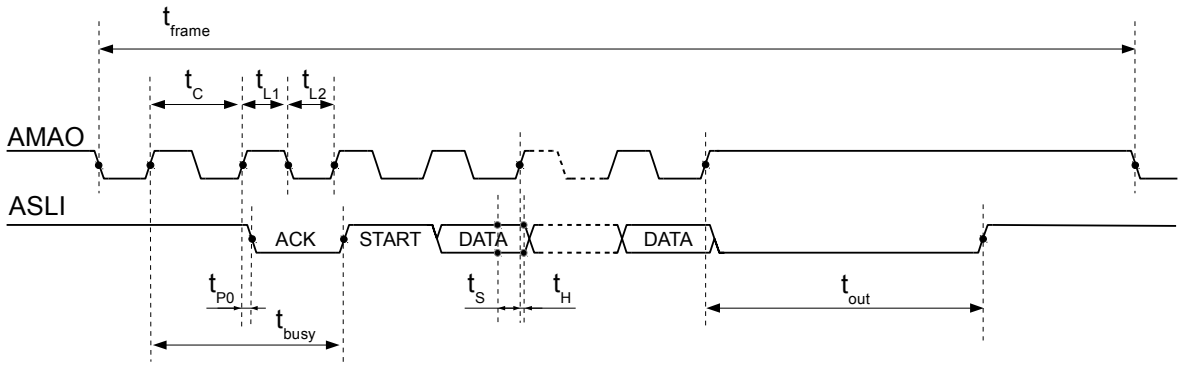

Figure 1: ADI timing with BiSS protocol

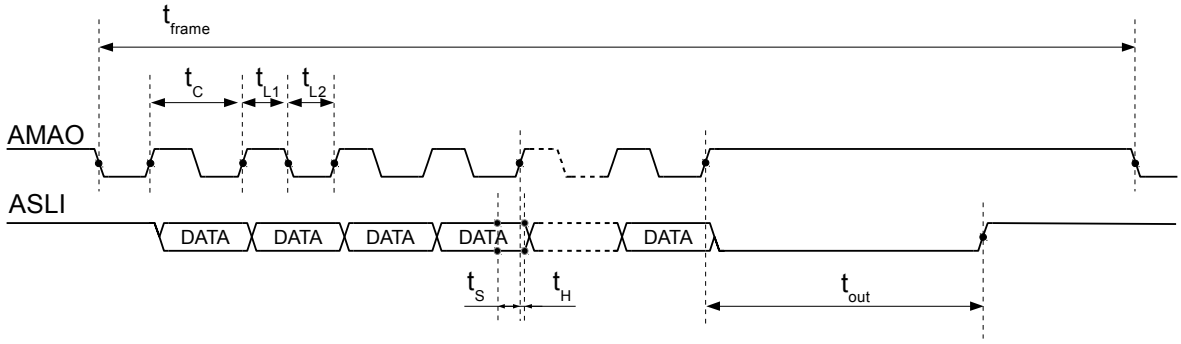

Figure 2: ADI timing with SSI protocol

OPERATING REQUIREMENTS: Parallel I/O Interface

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	t_{S1}	Setup Time: Address stable before NWR lo → hi		50		ns
I102	t_{H1}	Hold Time: Address stable after NWR lo → hi		50		ns
I103	t_{S2}	Setup Time: Data stable before NWR lo → hi		50		ns
I104	t_{H2}	Hold Time: Data stable after NWR lo → hi		50		ns
I105	t_{L1}	Write Signal Lo-Level Duration at NWR		80		ns
I106	t_{L2}	Write Signal Hi-Level Duration at NWR		80		ns
I107	t_{W1}	Wait Time between R/W Cycles: between NWR lo → hi to NRD hi → lo, and NRD lo → hi to NWR hi → lo		80		ns
I108	t_{L3}	Read Signal Lo-Level Duration at NRD		80		ns
I109	t_{L4}	Read Signal Hi-Level Duration at NRD		80		ns
I110	t_{P1}	Read Data Access Time: D(7...0) stable after NRD hi → lo			50	ns
I111	t_{P2}	Read Data Hold Time: D(7...0) high impedance after NRD lo → hi			50	ns
I112	t_{S3}	Setup Time: NCS hi → lo before NWR or NRD hi → lo		80		ns
I113	t_{H3}	Hold Time: NCS stable after NWR or NRD lo → hi		80		ns
I114	t_{S4}	Setup Time: NL hi → lo before NRD hi → lo		80		ns
I115	t_{H4}	Hold Time: NL stable after NRD lo → hi		80		ns

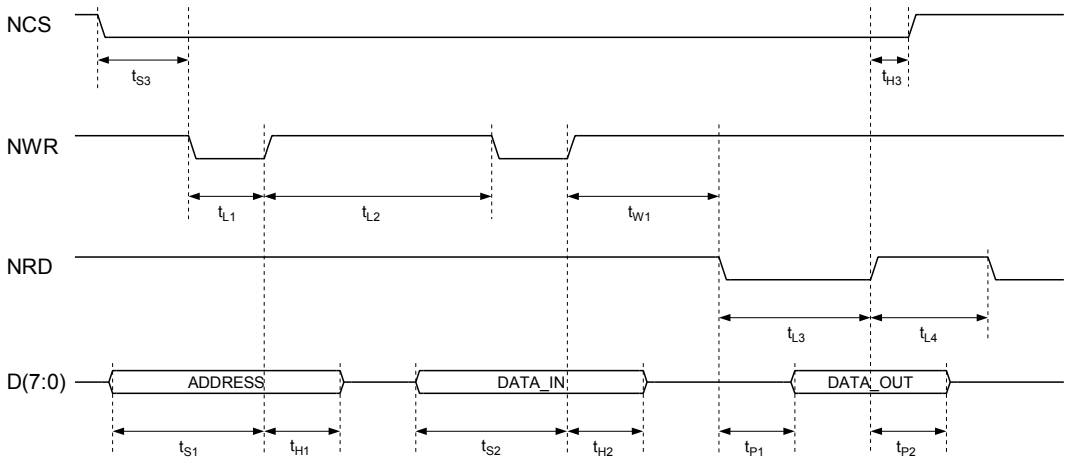

Figure 3: Parallel I/O interface timing

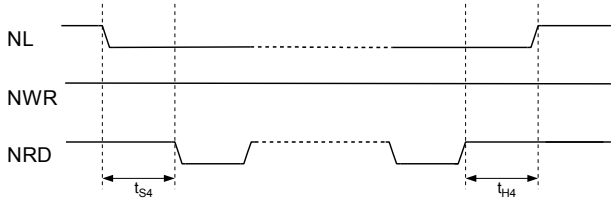

Figure 4: Parallel I/O interface timing for pin NL

OPERATING REQUIREMENTS: Serial I/O Interface: BiSS/SSI Protocol

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI protocol (INTCFG = 00, NESSI = 0)						
I201	t_C	Permissible Clock Period	refer to Elec. Char. O08 for clock frequency.	250		ns
I202	t_{L1}	Clock Signal Hi-Level Duration		125	t_{out}	ns
I203	t_{L2}	Clock Signal Lo-Level Duration		125	t_{out}	ns
I204	t_{RQ}	REQ Signal Lo-Level Duration		125	t_{out}	ns
I205	t_{P3}	Propagation Delay		10	50	ns
I206	t_{out}	Slave Timeout		see Elec. Char. O09		
I207	t_{frame}	Permissible Frame Repetition		*)	indefinite	
BiSS C protocol (INTCFG = 00, NESSI = 1)						
I208	t_C	Permissible Clock Period	refer to Elec. Char. O08 for clock frequency.	100		ns
I209	t_{L1}	Clock Signal Hi-Level Duration		50	t_{out}	ns
I210	t_{L2}	Clock Signal Lo-Level Duration		50	t_{out}	ns
I211	t_{busy}	Minimum Data Output Delay	ACQMODE ≠ 00 (modes w/o processing time)	2 t_C		
I212	t_{busy}	Maximum Data Output Delay	ACQMODE = 00 (mode with processing time)	t_{IPO} (see E.C. C01)		
I213	t_{P3}	Propagation Delay		10	50	ns
I214	t_{out}	Slave Timeout		see Elec. Char. O09		
I215	t_{S1}	Setup Time: SLI stable before MAI hi → lo		25		ns
I216	t_{H1}	Hold Time: SLI stable after MAI hi → lo		10		ns
I217	t_{frame}	Permissible Frame Repetition		*)	indefinite	

Note: *) Allow t_{out} to elapse.

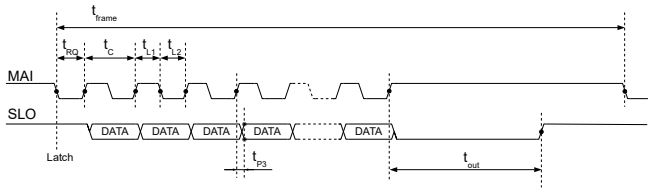

Figure 5: SSI protocol timing

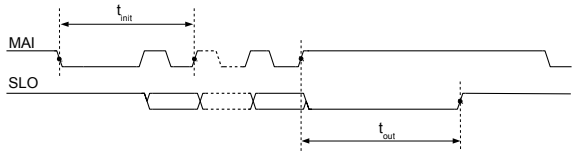

Figure 6: Adaptive timeout

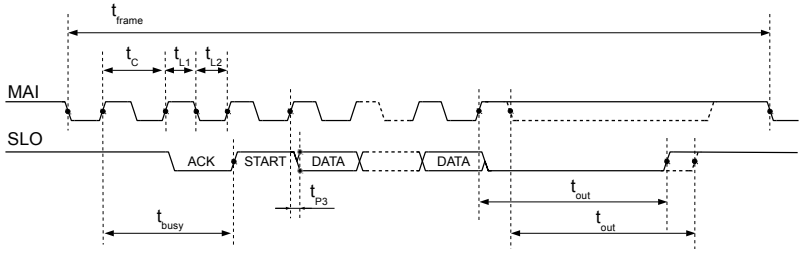

Figure 7: BiSS C protocol timing (ACQMODE ≠ 00)

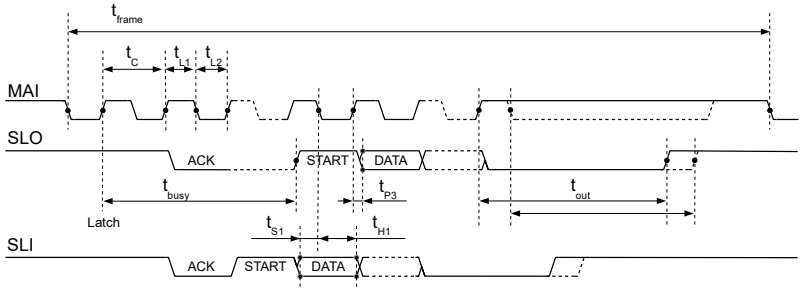

Figure 8: BiSS C protocol timing with triggered conversion (ACQMODE = 00) and chain operation

OPERATING REQUIREMENTS: Serial I/O Interface: SPI Protocol

Operating conditions:
VDDA = VDD = 4.5...5.5 V, VDDP = 2.375...VDDx, GNDA = GND = 0 V, IBP calibrated to 200 µA, Tj = -40...135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI protocol (INTCFG = 10)						
I301	t_C	Permissible Clock Period		100		ns
I302	t_{L1}	Clock Signal Hi-Level Duration		50		ns
I303	t_{L2}	Clock Signal Lo-Level Duration		50		ns
I304	t_{S1}	Setup Time: NCS lo before MAI hi → lo		50		ns
I305	t_{H1}	Hold Time: NCS lo after MAI lo → hi		100		ns
I306	t_{W1}	Wait Time between Cycles: between NCS lo → hi to NCS hi → lo		100		ns
I307	t_{S2}	Setup Time: SLI stable before MAI lo → hi		25		ns
I308	t_{H2}	Hold Time: SLI stable after MAI lo → hi		10		ns
I309	t_{P3}	Propagation Delay: SLO stable after MAI hi → lo			50	ns
I310	t_{P4}	Propagation Delay: SLO stable (low) after NCS hi → lo			50	ns
I311	t_{P5}	Propagation Delay: SLO high impedance after NCS lo → hi			50	ns

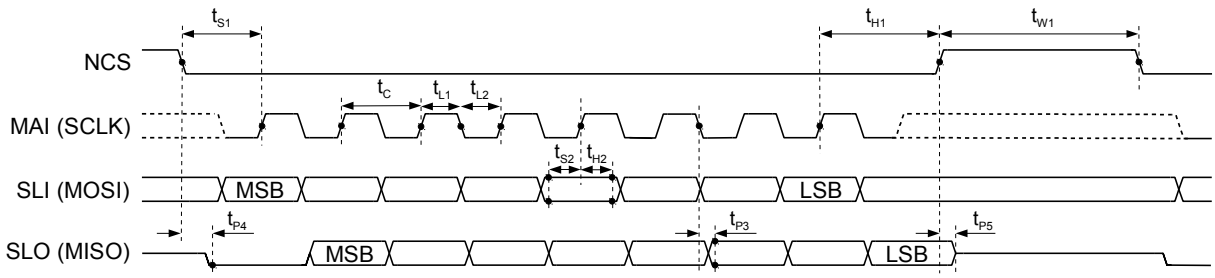

Figure 9: SPI protocol timing

CONFIGURATION PARAMETERS

REGISTER MAP: RAM

Configuration data and output data								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
The following addresses are available to BiSS accesses using slave ID = 0. If temperature data is enabled (ENTS = 1), these addresses are also serviced using slave ID = 1. **Pulling pin NRES low zeroizes all registers except of UIN[3]; the reset state is kept as long as NRES remains low.**								
Amplitude control								
0x00	ACOT(0)	ACOR(1:0)		ACOC(4:0)				
0x01	ACOD(6:0)							ACOT(1)
Signal conditioning								
0x02	GFS(3:0)				CTRLMOD	GR(2:0)		
0x03	0	GFS(10:4)						
0x04	GFC(7:0)							
0x05	MPS(3:0)				0	GFC(10:8)		
0x06	0	0	MPS(9:4)					
0x07	MPC(7:0)							
0x08	0	0	ORS(1:0)		0	0	MPC(9:8)	
0x09	OFS(7:0)							
0x0A	0	0	ORC(1:0)		0	OFS(10:8)		
0x0B	OFC(7:0)							
0x0C	PH(3:0)				NDBF	OFC(10:8)		
0x0D	SELREF(1:0)		PH(9:4)					
0x0E	INMODE	DCPOS	REFVOS(1:0)		TUIN	RIN(1:0)		UIN
0x0F	CFGBIAS(3:0)				SELBP	ENF	MODE(1:0)	
0x10	0	0	1	1	0	0	0	0
12-bit A/D converter and temperature monitoring								
0x11	ADCSLOP(7:0)							
0x12	ADCOFF(7:0)							
0x13	ADCOFF(15:8)							
0x14	TEMPLO(7:0)							
0x15	TEMPLO(15:8)							
0x16	TEMPHI(7:0)							
0x17	TEMPHI(15:8)							
Interfaces								
0x18	INTCFG(1:0)		FULL_CYC	GET_ADI	STP_ADI	CYC_ADI	SSIRING	SSIERR
0x19	ACQMODE(1:0)		ENLC	NESSI	CRC16	ENTS	SSIMODE(1:0)	
0x1A	DL_ADI(4:0)					SBL_ADI(1:0)		SSI_ADI
Offset & interpolator								
0x1B	OFFS_ST(1:0)		0	0	0	DIR	RESO_CC(1:0)	
0x1C	OFFS_ST(9:2)							
0x1D	OFFS_ST(17:10)							
0x1E	OFFS_ST(25:18)							
0x1F	OFFS_MT(7:0)							
0x20	OFFS_MT(15:8)							
0x21	OFFS_MT(23:16)							
Mask register for error and warning: EMASK, WMASK								
0x22	EM_EXT	EM_ABS	EM_IPO	EM_KNF	EM_SYN	EM_TMP	EM_AMP	EM_RGL
0x23	WM_EXT	WM_ABS	WM_IPO	WM_KNF	WM_SYN	WM_TMP	WM_AMP	WM_RGL

Configuration data and output data								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data resolution								
0x24	RESO_MT(2:0)			RESO_ST(4:0)				
Safety register								
0x25	NRDOK	SEC_HI(6:0)						
0x26	CFG_E2P(1:0)		SEC_LO(5:0)					
CRC configuration								
0x27	0	RES_ERR	CHK_ADI	0	0	0	0	0
0x28	CRCS(15:8)							
0x29	CRCS(7:0)							
Extended settings								
0x2A	0	0	0	0	0	0	0	0
0x2B	SLOW_ADI	0	0	0	THR_FAMP(1:0)		TO_FAMP	EN_FAMP
0x2C	NPD_SLI	SPO_ADI(3:0)				NTOA	0	0
0x2D	Reserved					DRVMASK	DRVDIS(1:0)	
Checksum for configuration data [EEPROM]								
0x2E	CRCCFG(15:8)							
0x2F	CRCCFG(7:0)							
0x30 ...0x3F	Not available							
Bank select								
0x40	I2CDEV [1]			BSEL(4:0)				
BiSS Device information (accessed from EEPROM)								
0x41	EDSBANK(7:0)							
0x42 [2]	PRO_IDx(15:8) : PRO_ID2(15:8) (Position) on BiSS access to slave ID = 0 PRO_ID1(15:8) (Temperature) on BiSS access to slave ID = 1							
0x43 [2]	PRO_IDx(7:0) : PRO_ID2(7:0) (Position) on BiSS access to slave ID = 0 PRO_ID1(7:0) (Temperature) on BiSS access to slave ID = 1							
0x44	SER_NO(31:24)							
0x45	SER_NO(23:16)							
0x46	SER_NO(15:8)							
0x47	SER_NO(7:0)							
0x48	PRO_ID1(15:8) (Temperature)							
0x49	PRO_ID1(7:0) (Temperature)							
0x50 ...0x57	Unused section (read only)							
Monitoring data (output data)								
0x58	Reserved							
0x59	Reserved							
0x5A	RG_MAX	AMP_MAX	DC_MAX	CMP_MAX	RG_MIN	AMP_MIN	DC_MIN	CMP_MIN
0x5B	Reserved							
0x5C	Reserved							
0x5D	Reserved							
0x5E	Reserved							
0x5F	Reserved							

Configuration data and output data								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status register / Command register (output data)								
0x60	INIT	ERR	WARN	EWKH	EWKL	BUSY	ADV	PDV
Position (output data)								
0x61	ST(1:0)		-					
0x62	ST(9:2)							
0x63	ST(17:10)							
0x64	ST(25:18)							
0x65	MT(7:0)							
0x66	MT(15:8)							
0x67	MT(23:16)							
Sign-of-life counter (output data)								
0x68	LC(7:0)							
Error register (output data)								
0x69	ERR_EXT	ERR_ABS	ERR_IPO	ERR_KNF	ERR_SYN	ERR_TMP	ERR_AMP	ERR_RGL
Temperature (output data)								
0x6A	TEMP(7:0)							
0x6B	TEMP(15:8)							
Checksum for cyclic telegrams (SPI or parallel output data)								
0x6C	CRC(7:0)							
0x6D	CRC(15:8)							
0x6E ...0x70	Unused							
Device information (ROM)								
0x71	CHIP_REV(7:0) (n/a MR3_W1) 0x30 = MR3_0, 0x31 = MR3_1, 0x33 = MR3_Z							
BiSS Device information (accessed from EEPROM)								
0x78	DEV_IDx(47:40) : DEV_ID2(7:0) (Position) on BiSS access to slave ID = 0 DEV_ID1(7:0) (Temperature) on BiSS access to slave ID = 1							
0x79	DEV_IDx(39:32)							
0x7A	DEV_IDx(31:24)							
0x7B	DEV_IDx(23:16)							
0x7C	DEV_IDx(15:8)							
0x7D	DEV_IDx(7:0)							
0x7E	MFG_ID(15:8)							
0x7F	MFG_ID(7:0)							

Notes

There is an address offset of 16 bytes between RAM and EEPROM: configuration data at 0x00 is read from the EEPROM at 0x10.

[1] I2CDEV = 000 is required to access the external EEPROM (I^2C device ID 0x50). Consult the Design Review if using early chip revisions.

[2] If SSI is configured, the GUI uses address 0x42 and 0x43 for backup purposes.

[3] UIN = 1 is the reset state for chip revision iC-MR3 Z2; UIN = 0 is the reset state for iC-MR3 Z and Z1.

Table 1: Register map

REGISTER MAP: EEPROM

Section CONF								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved								
0x000 ...0x00F	16 bytes of reserved memory (for system use)							
Configuration Data								
0x010 ...0x03F	iC-MR 3 configuration data							
BiSS Device Information								
0x040	Unused							
0x041	EDSBANK(7:0)							
0x042	PRO_ID2(15:8) (Position)							
0x043	PRO_ID2(7:0) (Position)							
0x044	SER_NO(31:24)							
0x045	SER_NO(23:16)							
0x046	SER_NO(15:8)							
0x047	SER_NO(7:0)							
0x048	PRO_ID1(15:8) (Temperature)							
0x049	PRO_ID1(7:0) (Temperature)							
0x050 ... 0x071	Unused							
BiSS Device Information Channel 1: Temperature Sensor								
0x072	DEV_ID1(47:40) (Temperature)							
0x073	DEV_ID1(39:32) (Temperature)							
0x074	DEV_ID1(31:24) (Temperature)							
0x075	DEV_ID1(23:16) (Temperature)							
0x076	DEV_ID1(15:8) (Temperature)							
0x077	DEV_ID1(7:0) (Temperature)							
BiSS Device Information Channel 2: Position Sensor								
0x078	DEV_ID2(47:40) (Position)							
0x079	DEV_ID2(39:32) (Position)							
0x07A	DEV_ID2(31:24) (Position)							
0x07B	DEV_ID2(23:16) (Position)							
0x07C	DEV_ID2(15:8) (Position)							
0x07D	DEV_ID2(7:0) (Position)							
BiSS Device Information Channel 1+2								
0x07E	MFG_ID(15:8)							
0x07F	MFG_ID(7:0)							
Sections EDS and USER								
0x080 ...	EDS data and USER data							

Table 2: Register map

OPERATING MODES

The operation mode can be altered using the register MODE, in order to calibrate the iC-MR3, to adjust the input signals, as well as to test the iC-MR3. The output functions of PSO, NSO, PCO and NCO change according to the selected operating mode.

MODE(1:0) **MODE(4:2)**		**ADR 0x0F; bit 1:0** **ADR 0x10; bit 2:0**			
Code	Operating mode	Pin PSO	Pin NSO	Pin PCO	Pin NCO
0x00 [1]	Normal operation	PSO	NSO	PCO	NCO
0x01	Analog 1	PS_W	NS_W	PC_W	NC_W
0x02	Analog 2	SVDC	CVDC	VREFI	IBP
0x03 [2]	Bypass	PSI	NSI	PCI	NCI
0x04	Extended test mode				
...					
0x1F	Extended test mode				
Notes	[1] Configuration in accordance to register map. Extended test modes are disabled.				
	[2] In bypass mode, the conditioned input signals ahead of the filter circuit are provided. As the sin/cos output drivers are bypassed, any pin load may interfere LED control.				

Table 3: Operating mode

Calibration modes

In operation mode Analog 1, the adjusted sine and cosine signals (PS_W, NS_W, PC_W and NC_W) are provided at the output pins.
In operation mode Analog 2, bias current source (IBP), reference potential input (VREFI), and the VDC center potentials of the calibration circuits for sine (SVDC) and cosine (CVDC) can be measured.

Extended test modes

Extended test modes (0x04 to 0x1F) have been implemented to allow device testing at iC-Haus. During normal operation the bits of MODE(4:2) are not evaluated by iC-MR3 and thus can be kept '0'.

BIAS CURRENT SOURCE

The calibration of the bias current source in operating mode Analog 2 is required to ensure the validity of the Electrical Characteristics and is instrumental in the determination of the chip timing (e.g. SCL clock frequency). To adjust the bias current source, the voltage drop is to be measured using a 10 kΩ resistor from pin NCO to pin GNDA. The setpoint of 200 µA is reached with a measurement voltage of 2 V.

CFGBIAS	Addr. 0x0F, bit 7:4		
Code k (signed)	$IBP \sim \frac{31}{31-k}$	Code k (signed)	$IBP \sim \frac{31}{31-k}$
0x0	100 %	0x8	79 %
0x1	103 %	0x9	81 %
0x2	107 %	0xA	84 %
0x3	111 %	0xB	86 %
0x4	115 %	0xC	88 %
0x5	119 %	0xD	91 %
0x6	124 %	0xE	94 %
0x7	129 %	0xF	97 %

Table 4: Bias calibration

SIGNAL CONDITIONING

Input configuration

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Single-ended input signals can be processed by applying the input signal's reference voltage to the negative inputs. Both voltage and current signals can be accepted as input signals. For selection, use register bit UIN.

Figure 10 shows the sine channel's conditioning unit; the cosine channel's set-up is equivalent to that of the sine channel. Signal adjustment is possible only in operating modes Analog 1 and Analog 2.

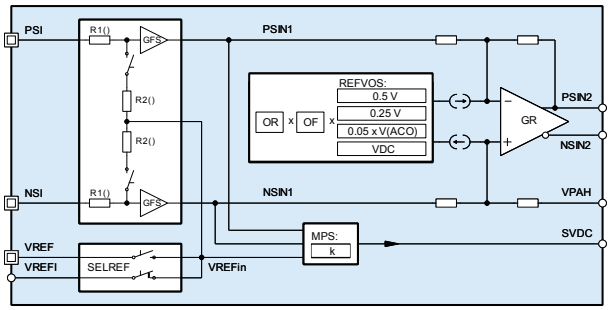

Figure 10: Signal-conditioning unit (sine channel)

INMODE	Addr. 0x0E, bit 7
Code	Function
0	Differential input signals
1	Single-ended input signals The negative inputs must be connected to a suitable reference voltage.
Notes	The configuration of INMODE is relevant only if using the self-tracking VDC offset references (see Table 13).

Table 5: Differential/single-ended signal mode

UIN	Addr. 0x0E, bit 0
Code	Function
0	Current inputs (I-Mode)
1	Voltage inputs (V-Mode)
Notes	Voltage input is the default state ahead of configuration and during reset (pin NRES = low). After startup, UIN is overwritten either by the value from the EEPROM or by zero if there is no EEPROM connected.

Table 6: Current/voltage signal mode

Current signals

In current mode (I-Mode), an internal resistor R2() becomes active at each input, converting the current signal into a voltage signal. The effective input resistance Rin() is always determined by the sum of R1 and R2, whereas R2 is linking to the selectable reference voltage VREFin.
R2 should be set to obtain approx. 125 mV to 250 mV for the VDC offset references (for SVDC and CVDC, using operating mode Analog 2).

RIN	Addr. 0x0E, bit 2:1		
Code	In-line R1()	Internal R2()	I/V Mode
00	0.1 kΩ	1.6 kΩ	I-Mode
01	0.2 kΩ	2.3 kΩ	I-Mode
10	0.3 kΩ	3.2 kΩ	I-Mode
11	0.3 kΩ	4.6 kΩ	I-Mode
Notes	Nominal values; Rin = R1() + R2(); for tolerances refer to Elec.Char. No. 706, 707, and 708.		

Table 7: Input resistance

Note: The input circuit is not suitable for back-to-back photodiodes.

Voltage signals

In voltage mode (V-Mode), an optional voltage divider can be selected for high input amplitudes. This voltage divider reduces the input signal's amplitude to 25% of the original. The internal circuit corresponds to the circuit in current mode, just the in-line resistor R1 is altered.

TUIN	Addr. 0x0E, bit 3		
Code	In-line R1()	Internal R2()	I/V Mode
0	3.5 kΩ	High impedance	V-Mode 1:1
1	15 kΩ	5 kΩ	V-Mode 4:1
Notes	Nominal values; Rin = R1() + R2(); for tolerances refer to Elec.Char. No. 703, and 708.		

Table 8: Input voltage divider

Input reference voltage

The parameter DCPOS determines the internal input reference voltage VREFI. In the generation of the VDC offset references (SVDC and CVDC), it also determines whether the reference voltage VREFin is subtracted from the sum of the particular input signals or the sum is subtracted from VREFin.

Parameter SELREF configures the reference voltage multiplexer.

DCPOS	Addr. 0x0E, bit 6		
Code	VREFI	Sensor output:	
		Current	Voltage*
0	2.5 V	Lowside current sink	V(PSI) + V(NSI) < 2 x VREFin
1	1.5 V	Highside current source	V(PSI) + V(NSI) > 2 x VREFin
Notes	*) Condition is relevant only if using - the self-tracking VDC offset ref. (see Table 13) - the input voltage divider (see Table 8) - sum and combined control modes (see Table 20)		

Table 9: Reference voltage and current polarity

SELREF	Addr. 0x0D, bit 7:6	
Code	VREF Pin Function	Input Reference Voltage
0x0, 0x1	None (high impedance)	$VREF_{in}$ = VREFI
0x2	Output* VREFI → VREF	$VREF_{in}$ = VREFI
0x3	Input** VREF ← $VREF_{ex}$	$VREF_{in}$ = $VREF_{ex}$
Notes	*) Output signal should be buffered. **) Refer to Elec.Char. No. 105 for permissible input voltage.	

Table 10: Input reference selection

Sine/cosine gain settings
The gain is set in four steps:

1. The amplitude control is to be shut down and the constant current source for the ACO output set to a suitable output current (register ACOC; current value close to the later operating point).

2. The coarse gain factor is selected so that differential signal amplitudes of almost 6 Vpp are output.

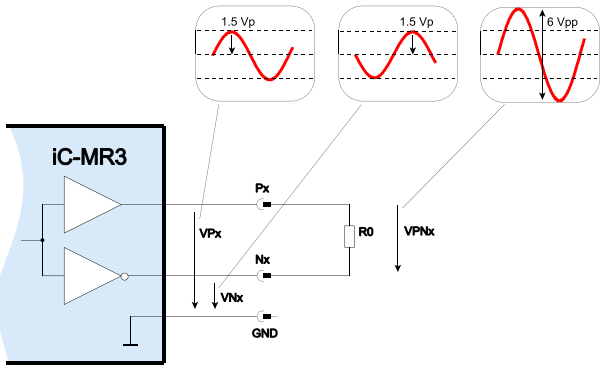

Figure 11: Output signals in mode Analog 1.
Refer to Elec. Char. No. A08 for source resistance.

Note: In Normal mode, the converter's core signals are output via line drivers at 1/6 the amplitude in Analog 1 mode.

3. Using fine gain factor GFS the sine signal amplitude is then adjusted to 6 Vpp.

4. Finally, the cosine signal amplitude needs to be adjusted exactly to the sine signal amplitude using the fine gain factor GFC.

GR	Addr. 0x02, bit 2:0
Code	Factor in mode Analog 1
0x0	6.0
0x1	12.3
0x2	15.9
0x3	20.1
0x4	26.1
0x5	31.5
0x6	39.6
0x7	48.0
Notes	The effective total gain is calculated using: G_{eff} = GFx x GR, or G_{eff} = 1/4 x GFx x GR if using the input voltage divider (TUIN = 1).

Table 11: Coarse gain factor

GFS	Addr. 0x03, bit 6:0, Addr 0x02, bit 7:4
GFC	Addr. 0x05, bit 2:0, Addr 0x04, bit 7:0
Code	Factor in mode Analog 1
0x000	1.0
0x001	1.0009
...	$6.25^{(Code/1984)}$
0x7FF	6.6245

Table 12: Sine and cosine fine gain factor

Sine/cosine offset calibration
In order to calibrate the offset, the reference source must first be selected using register REFVOS. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which provide stable, self-regulated signals.

The VDC offset references enable the calibration to be automatically tracked dependent on the DC level of the input signal. In order to use this function, center potentials SVDC and CVDC have to be adjusted to a minimal AC ripple using parameters MPS and MPC (refer to the k factor of Table 14).

When single-ended signal mode is selected (bit INMODE, see Table 5) MPS and MPC have no impact and the voltage applied to the negative input replaces the configurable center voltage in the VDC generation.

If V(ACO) is chosen as the offset reference, 1/20 of the voltage at pin ACO acts as the reference. This enables the offset to be calibrated dependent on the

supply voltage of the sensor. In this case the justification of the VDC center potentials using MPS and MPC is unnecessary.

REFVOS	Addr. 0x0E, bit 5:4
Code	Source type
0x0	Feedback of ACO pin voltage: V(REFVOS) = V(ACO)/20 for sensor supply-dependent diff. voltage signals for Wheatstone measuring bridges to measure VDDS
0x1 0x2	Fixed offset reference voltage: V05: V(REFVOS) = 500 mV V025: V(REFVOS) = 250 mV for single-ended current or voltage signals for single-ended or differential stabilized signals (regulated sensors, frequency generator)
0x3	Self-tracking VDC offset references: $V(REFVOS)_S$ = SVDC $V(REFVOS)_C$ = CVDC for differential current signals for differential voltage signals*
Note	*) Requires SELREF = 0x3 and the supply of pin VREF with the sensor's reference potential (refer to Elec. Char. No. 105 for acceptable input voltages).

Table 13: Offset reference source

MPS **MPC**	Addr. 0x06, bit 5:0, Addr. 0x05, bit 7:4 Addr. 0x08, bit 1:0, Addr. 0x07, bit 7:0
Code	$SVDC = k * V(PSIN1) + (1 - k) * V(NSIN1)$ $CVDC = k * V(PCOS1) + (1 - k) * V(NOCS1)$
0x000	$k = 0.33$
0x001	$k = 0.33032$
...	... $k = 0.33 + Code \cdot 0.00032$
0x200	$k = 0.50$ (center setting)
...	...
0x3FF	$k = 0.66$
Note	Adjustment required only if REFVOS = 0x3

Table 14: Sine and cosine VDC center potential

The offset calibration is dependent on the selected REFVOS source and is adjusted using the registers ORS and ORC. The actual offset calibration happens through adjusting the fine offset factors OFS and OFC after having selected the coarse offset factors. The calibration target is reached when the differential output signals V(PSO)-V(NSO) and V(PCO)-V(NCO) show a zero DC voltage.

ORS **ORC**	Addr. 0x08, bit 5:4 Addr. 0x0A, bit 5:4
Code	Factor
0x0	3
0x1	6
0x2	18
0x3	36
Notes	The maximum offset calibration range maxVOS refers to the calibrated internal signals (mode Analog 1, see page 24) and is calculated using: $maxVOS_{Sin}$ = ORS x $V(REFVOS)_S$, or $maxVOS_{Cos}$ = ORC x $V(REFVOS)_C$

Table 15: Sine and cosine coarse offset factor

OFS **OFC**	Addr. 0x09, bit 7:0, Addr. 0x0A, bit 2:0 Addr. 0x0B, bit 7:0, Addr. 0x0C, bit 2:0
Code	Factor
0x000	0
0x001	0.00098
...	+ $Code/1023$
0x3FF	1
0x400	0
0x401	-0.00098
...	$-(Code - 1024)/1023$
0x7FF	-1
Notes	The effective total offset correction is calculated using: $VOSeff_{Sin}$ = $maxVOS_S$ x OFS, or $VOSeff_{Cos}$ = $maxVOS_C$ x OFC

Table 16: Sine and cosine fine offset factor

The maximum offset calibration range maxVOS also increases the offset calibration step size (LSB), what can rise residual offset errors. Depending on the signal's amplitude, the residual offset errors can limit the possible interpolation accuracy. Table 17 shows the dependencies for full-scale and half-scale signals (refered to mode Analog 1).

Coarse F. x Source	maxVOS	Cal. Step Size (LSB)	Limitation of Angle Accuracy
3 x 0.25 V	750 mV	733 µV	none (>13 bit) [a, b]
6 x 0.25 V	1.5 V	1466 µV	0.03° >13 bit [a] 0.06° ≈ 12 bit [b]
6 x 0.5 V	3 V	2933 µV	0.06° ≈ 12.5 bit [a] 0.11° ≈ 11.7 bit [b]
18 x 0.5 V	9 V	8798 µV	0.17° ≈ 11 bit [a] 0.34° ≈ 10 bit [b]
Note	[a]) Full scale signal ≈ 6 Vpp, [b]) 50 % FS signal ≈ 3 Vpp		

Table 17: Offset calibration range and impact on the angle accuracy

Sine to cosine phase correction

The phase shift between sine and cosine can be adjusted using parameter PH. Following phase calibration, other calibration parameters may have to be readjusted (those as fine gain, VDC center potentials and offset voltages).

Note: When correcting a phase error beyond 2.25°, gain and offset need to be readjusted. Otherwise the interpolation accuracy can be less than 13 bit.

PH	Addr. 0x0D, bit 5:0, Addr. 0x0C, bit 7:4
Code	Correction angle
0x000	0 °
0x001	+ 0.0204 °
...	+ 10.42 ° · *Code*/511
0x1FF	+ 10.42 °
0x200	0 °
0x201	– 0.0204 °
...	– 10.42 ° · (*Code* – 512)/511
0x3FF	– 10.42 °

Table 18: Sine to cosine phase correction

AMPLITUDE CONTROL

The iC-MR3 allows the amplitude of the output signals at pins PSO, NSO, PCO, and NCO to be kept constant - regardless of temperature and ageing effects - by tracking the sensor supply. For this purpose, the iC-MR3 has a controlled high-side current source at pin ACO which can power the external sensor. The driver capability of this current source is selected by ACOR, the control mode by ACOT.

ACOR	Addr. 0x00, bit 6:5
Code	Current Range
00	0.05 mA ... 5 mA
01	0.1 mA ... 10 mA
10	0.25 mA ... 25 mA
11	0.5 mA ... 50 mA
Note	The range defines the ACO output's guaranteed driving capability. Refer to Elec. Char. No. 802 for the corresponding short-circuit current.

Table 19: ACO Output current range (for control operation and constant current source)

ACOT	Addr. 0x01, bit 0; Addr 0x00, bit 7
Code	Function
00	Square control
01	Sum control
10	Sum and square combined
11	Current source (constant current)

Table 20: ACO Output control mode

CTRLMOD	Addr 0x02, bit 3
Code	Function (ACOT < 11)
0	Continuous control
1	Deadband control (approx. 5 % of setpoint)

Table 21: Type of control

Note: The control output ACO is activated with power-on, using reset values (0x00) initially, until the relevant configuration registers have been read from the EEPROM.

Sum control mode

In sum control mode the sine and cosine DC values (SVDC and CVDC) are added together and the ACO output current is regulated to keep the DC setpoint constant. The DC setpoint is configured using the register ACOD.

Sum control mode results in a higher interpolation accuracy at low input frequencies, opposed to square control mode. However, at higher input frequencies it cannot compensate for a reduction in the signal amplitude caused by the amplifier cutoff frequency of the sensors.

ACOD	Addr. 0x01, bit 7:1
Code	**Sum mode** ACOT = 01
0x00	SVDC + CVDC ≈ 166 mV
0x01	SVDC + CVDC ≈ 167 mV
...	SVDC + CVDC ≈ 166 mV $\frac{109}{109-(0.6*Code)}$
0x7F	SVDC + CVDC ≈ 551 mV

Table 22: Sum control DC setpoint

Square control mode

Square control mode keeps the sum of the sine/cosine amplitude squares at a constant value. In this case the ACO output current is regulated to the AC setpoint configured by the register ACOC.

ACOC	Addr. 0x00, bit 4:0
Code	**Square mode** ACOT = 00
0x00	Vpp() ≈ 300 mV (60 %)
0x01	Vpp() ≈ 305 mV (61 %)
...	Vpp() ≈ 300 mV $\frac{77}{77-(1.25*Code)}$
0x19	Vpp() ≈ 500 mV (98 %)
...	...
0x1F	Vpp() ≈ 600 mV (120 %)

Table 23: Square control AC setpoint

Combined control mode

iC-MR3 features a combined control mode which utilizes both control modes, sum and square (see Table 20). In this mode, sum control is applied at low frequencies with square control taking over at higher frequencies, when the sensor's amplifiers cutoff frequency is exceeded. So that this control mode functions correctly, the set signal amplitude for square control mode (AC setpoint) must be lower than that of the sum control (DC setpoint).

Constant current source

So that the output signals at the pins PSO, NSO, PCO, and NCO can be calibrated without control interference, the high-side current source at pin ACO can be set to a constant current.

ACOC	Addr. 0x00, bit 4:0
Code	**Constant current source** ACOT = 11
0x00	I(ACO) ≈ 3.125 % Isc(ACO)
0x01	I(ACO) ≈ 6.250 % Isc(ACO)
...	I(ACO) ≈ 3.125 % * (Code + 1) * Isc(ACO)
0x1F	I(ACO) ≈ 100 % Isc(ACO)
Note	The setpoint defines the ACO output current relative to Isc(ACO), the output's short-circuit current (see Elec. Char. No. 802) which depends on the selected range.

Table 24: Current source setpoint (ACO output current)

Signal level monitoring

The control's operating range and the input signal amplitudes supplied to the control unit are both monitored. Should any error occur during operation, this can be indicated by error and warning messages (refer to Diagnosis Register page 61 and Error/Warning Masking on page 60).

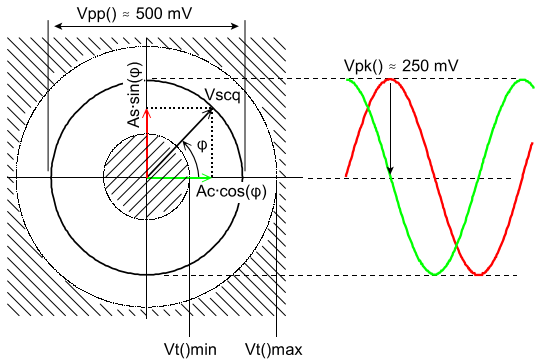

Figure 12: Signal level monitoring according to square control AC setpoint (example for ACOC(4:0) = 0x19)

ACOC()	Vpp()	Vt()min ... Vt()max
0x19	≈ 500 mV	200 mV ... 675 mV
Notes	Nominal values, see Elec. Char. Nos. 809, 810 for variation.	

Table 25: Signal level monitoring (example)

The signal monitoring limits are tracked according to ACOC(4:0) and fit for square control mode. When using sum control the resulting signal amplitudes may differ, so that the monitoring limits need to be readjusted using ACOC(4:0). If there is no match possible, signal monitoring can just be excluded from status messaging using the error masking registers.

SIGNAL MONITORING

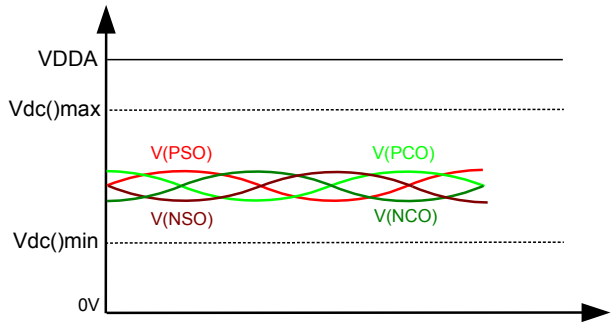

Figure 13: DC level monitoring: max. and min. voltage thresholds according to Elec. Characteristics B06 and B07.
For error messaging, refer to the diagnosis register, page 61.

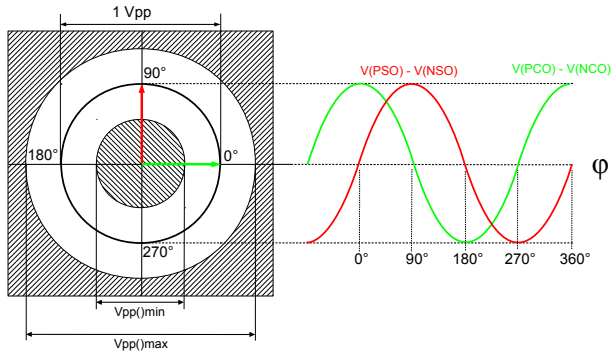

Figure 14: AC level monitoring: differential voltage thresholds according to Elec. Characteristics B03 and B04.
For error messaging, refer to the diagnosis register, page 61.

The signal monitoring circuit verifies that all four analog signal lines show an acceptable DC voltage (within approx. 1.75 V to 3.12 V) and that both differential signals, sine and cosine, show an acceptable AC amplitude (within approx. 0.35 Vpp to 1.3 Vpp).

The AC monitoring circuit uses an analog multiplier and evaluates the circular XY-plot (Lissajous figure) derived from the square sum signal of sine and cosine ($sin(\omega t)^2 + cos(\omega t)^2$).

Independent comparators for DC monitoring and AC monitoring then stipulate the signal error messages DC_MAX, DC_MIN and CMP_MAX, CMP_MIN (refer to diagnosis register, page 61).

Note: If a fractured cable needs to be detected, each analog input may require an external pull-down resistor to drag the DC potential into the error range.

SIGNAL FILTERING AND SIN/COS OUTPUT DRIVERS

Signal filtering

In order to decrease the analog sin/cos signals' noise, the iC-MR3 offers an adaptive noise filter which adjusts its cutoff depending on the input frequency. This filtering can be activated through parameter ENF.

ENF	Addr. 0x0F, bit 2
Code	Function
0	Signal noise filter disabled
1	Signal noise filter enabled

Table 26: Noise filter enable

Parameter SELBP adjusts how tight the noise filter's lowpass cutoff frequency is tracking the actual input frequency. The tighter value is favorable for signal noise reduction, the relaxed value is favorable regarding signal distortion.

SELBP	Addr. 0x0F, bit 3
Code	Function
0	7.5 kHz (@ fin < 10 Hz)
1	15 kHz (@ fin < 10 Hz)

Table 27: Noise filter cutoff frequency

The noise filter's adaption mode can be changed using NDBF. Using deadband adaption is favorable regarding signal distortion. However, assuming a fixed input frequency, note that the lowpass cutoff frequency can vary due to the deadband behavior.

NDBF	Addr. 0x0C, bit 3
Code	Function
0	Deadband
1	Standard

Table 28: Noise filter adaption mode

Sin/Cos output drivers

The analog signal path of iC-MR3 operates independently from the interpolation engine, and features embedded line drivers to output differential 1 Vpp signals to lines with 100 Ω or 120 Ω termination.

The parameter DRVDIS defines if the output drivers come active after startup, and if error events can switch the drivers to tristate. For the latter, DRVMASK chooses between *Standard Errors*, a selected subset of implemented error messages, and *Configured Errors*, which are selected by EMASK to be indicated on the BiSS error bit, as well as at the error output NERR.

DRVDIS	Addr. 0x2D; bit 1...0
Code	Function
0x0	Never disable the drivers on error (the drivers are disabled during startup only)
0x1	Disable the drivers during error(s) (as long as an error persists)
0x2	Disable the drivers on error(s) until clearing action (as configured by RES_ERR: either read of position data, or read of the error register)
0x3	Drivers permanently disabled.

Table 29: Output driver disable

DRVMASK	Addr. 0x2D, bit 2
Code	Function
0	Driver disabled on *Standard Errors* Definition of *Standard Errors*: 1. Initialization phase 2. Configuration Error (ERR_KNF) 3. Temperature Error (ERR_TMP)
1	Driver disabled on *Configured Errors* Definition of *Configured Errors*: 1. Initialization phase 2. Events selected by EMASK

Table 30: Output driver disable masking

Note: When there is no EEPROM or no valid configuration provided on power up, DRVDIS = 0x0 is the default and the sin/cos output drivers are active following startup.

Note: When iC-MR3 has been configured with checksum (CRCCFG at 0x2E-0x2F) using an interface (e.g. BiSS) with DRVDIS = 0x1 or 0x2, a command for CRC verification is required to reset configuration error ERR_KNF and to enable the sin/cos output drivers (depending on the setting of DRVMASK).

When iC-MR3 has been configured w/o the checksum, a command for writing the configuration to the EEPROM can be used. Following a power cycle, iC-MR3 is operational as configured.

Note: The sin/cos outputs PSO, NSO, PCO, NCO are all floating if all chip supply pins are left open.
The sin/cos outputs are tristate if NRES = 0.
The sin/cos outputs are defined by DRVDIS and DRVMSK if there is an error condition in operation.

12-BIT A/D CONVERTER

The iC-MR3 features a 12-bit A/D converter at the ADC input pin. Its output data is stored in the TEMP register, which can be read using the interfaces.

The A/D converter operates constantly, updating the data in register TEMP after each conversion. The TEMP register at addresses 0x6A and 0x6B must be read out from the cyclic frame. Otherwise if reading bytewise, it is not guaranteed that a coherent data word is read.

The A/D converter can be calibrated using registers ADCSLOP and ADCOFF. Register ADCSLOP has 8 bits and is used to set the maximum voltage the converter can process at pin ADC. The allocation of the register data in ADCSLOP to the maximum voltage is expressed in Table 31. Using the second calibration register ADCOFF, which has 16 bits, an offset can be added to the converter's digital output data.

ADCSLOP	Addr. 0x11; bit 7...0	R/W
Code	Full scale level for VDDA = 5V	
0x00	2.0 V	
0x01	2.00196 V	
...	2.0 V + 1.96 mV * ADCSLOP	
0xFF	2.5 V	

Table 31: Maximum ADC input voltage

ADCOFF	Addr. 0x12...0x13;	R/W
Code	Function	
0x7FFF	TEMP = TEMP(int) - 32767	
...		
0x0001	TEMP = TEMP(int) - 1	
0x0000	TEMP = TEMP(int)	
0xFFFF	TEMP = TEMP(int) + 1	
...		
0x8000	TEMP = TEMP(int) + 32768	

Table 32: Digital temperature offset

The registers TEMPHI and TEMPLO define the upper and lower thresholds for the error output. If the current converter value is above TEMPHI or below TEMPLO, the ERR_TMP alarm bit is set in the error register. The internal ADC can be utilized to continuously record an external temperature, for which a temperature-dependent voltage is applied at input ADC. This voltage may be generated by a KTY temperature sensor. A temperature monitor can be created using thresholds TEMPHI and TEMPLO. For example, the following describes the evaluation of temperature sensor KTY 84.

TEMPLO	Addr. 0x14...0x15;	R/W
TEMPHI	Addr. 0x16...0x17;	R/W
Code	Temperature threshold	
0x7FFF	+3276.7 °C	
...	...	
0x07D0	+200.0 °C	
...	...	
0x0001	+0.1 °C	
0x0000	0.0 °C	
0xFFFF	-0.1 °C	
...	...	
0xFE70	-40 °C	
...	...	
0x8000	-3276.8 °C	
Note	Thresholds for example KTY 84	

Table 33: Temperature thresholds

Figure 15 shows a schematic circuit diagram for the evaluation of the KTY. A resistor of approximately 2.3 kΩ is switched in series with the KTY sensor to linearize the voltage supplied by the KTY. This results in a linear temperature voltage.

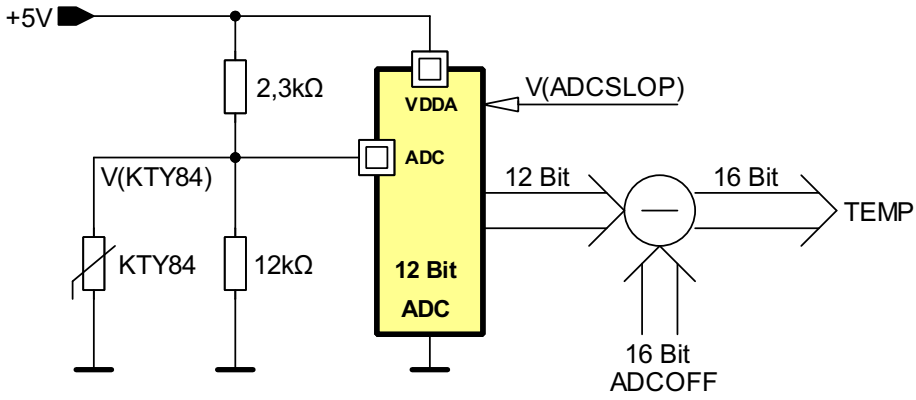

Figure 15: Schematic circuit diagram for the evaluation of KTY sensors.

The temperature is output according to Table 34 as a 16-bit value in two's complement format with a resolution of 1/10°C.

TEMP	Addr 0x6B, 0x6A, bits: 15..8, 7..0	
Code	Temperature	Validity
0x7FFF	+3276.7 °C	Out of
...	...	measuring range
0x07D0	+200.0 °C	
...	...	
0x0001	+0.1 °C	
0x0000	0.0 °C	Measuring range
0xFFFF	-0.1 °C	
...	...	
0xFE70	-40 °C	
...	...	Out of
0x8000	-3276.8 °C	measuring range

Table 34: Temperature data

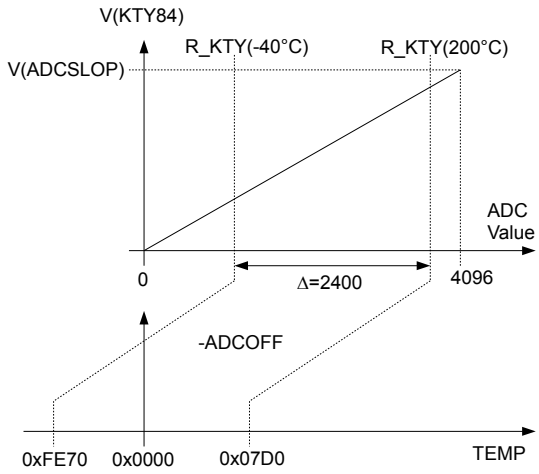

Figure 16: Calibrating the temperature sensor to the output format

To obtain the output given in Table 34 the evaluation circuitry is calibrated as follows:

1. The maximum convertible voltage is set and thus the increase in the converter using the register ADCSLOP. ADCSLOP's register is set so that there is a difference of 2,400 between the converter values at R(KTY84) = 359 Ω and R(KTY84) = 1,722 Ω.
2. To map ADC's output to the range of values given in Table 34, an offset is added through register ADCOFF. The data in register ADCOFF is set so that 0xFE70 is read at R(KTY84) = 359 Ω and, correspondingly, 0x07D0 at R(KTY84) = 1,722 Ω.
   (a) Read converter data from register TEMP with ADCOFF = 0x0000 at R(KTY84) = 359 Ω.
   (b) Calibration data = converter data + 400
   (c) Write the calibration data to register ADCOFF.

12-BIT A/D CONVERTER USING PT1000

The iC-MR3 features a 12-bit A/D converter at the ADC input pin. Its output data is stored in the TEMP register, which can be read using the interfaces.

The A/D converter operates constantly, updating the data in register TEMP after each conversion. The TEMP register at addresses 0x6A and 0x6B must be read out from the cyclic frame. Otherwise if reading bytewise, it is not guaranteed that a coherent data word is read.

The A/D converter can be calibrated using registers ADCSLOP and ADCOFF. Register ADCSLOP has 8 bits and is used to set the maximum voltage the converter can process at pin ADC. The allocation of the register data in ADCSLOP to the maximum voltage is expressed in Table 35. Using the second calibration register ADCOFF, which has 16 bits, an offset can be added to the converter's digital output data.

ADCSLOP	Addr. 0x11; bit 7...0	R/W
Code	Full scale level for VDDA = 5V	
0x00	2.0 V	
0x01	2.00196 V	
...	2.0 V + 1.96 mV * ADCSLOP	
0xFF	2.5 V	

Table 35: Maximum ADC input voltage

ADCOFF	Addr. 0x12...0x13;	R/W
Code	Function	
0x7FFF	TEMP = TEMP(int) - 32767	
...		
0x0001	TEMP = TEMP(int) - 1	
0x0000	TEMP = TEMP(int)	
0xFFFF	TEMP = TEMP(int) + 1	
...		
0x8000	TEMP = TEMP(int) + 32768	

Table 36: Digital temperature offset

The registers TEMPHI and TEMPLO define the upper and lower thresholds for the error output. If the current converter value is above TEMPHI or below TEMPLO, the ERR_TMP alarm bit is set in the error register. The internal ADC can be utilized to continuously record an external temperature, for which a temperature-dependent voltage is applied at input ADC. This voltage may be generated by a PT1000 temperature sensor. A temperature monitor can be created using thresholds TEMPHI and TEMPLO. For example, the following describes the evaluation of temperature sensor PT1000.

TEMPLO	Addr. 0x14...0x15;	R/W
TEMPHI	Addr. 0x16...0x17;	R/W
Code	Temperature threshold	
0x7FFF	+16383.5 °C	
...	...	
0x0190	+200.0 °C	
...	...	
0x0001	+0.5 °C	
0x0000	0.0 °C	
0xFFFF	-0.5 °C	
...	...	
0xFFB0	-40.0 °C	
...	...	
0x8000	-16384.0 °C	
Note	Thresholds for example PT1000	

Table 37: Temperature thresholds

Figure 17 shows a schematic circuit diagram for the evaluation of the PT1000. A resistor of approximately 15 kΩ is switched in series with the PT1000 sensor to linearize the voltage supplied by the PT1000. Another resistor of approximately 100 kΩ is switched in parallel with the PT1000 sensor. This results in a linear temperature voltage.

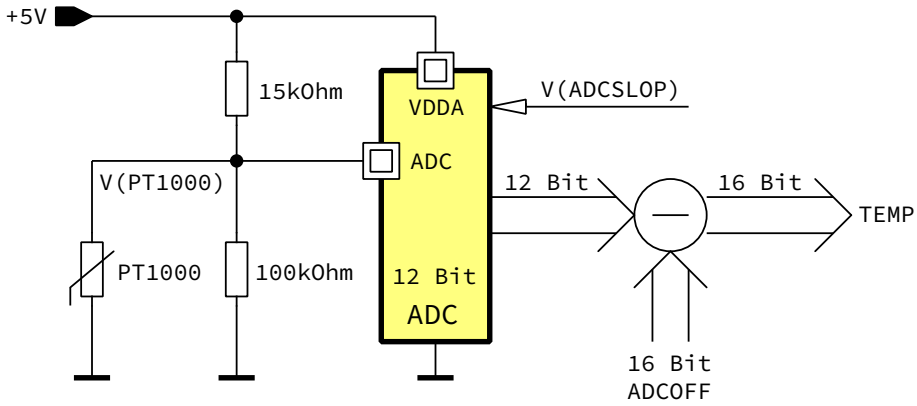

Figure 17: Schematic circuit diagram for the evaluation of PT1000 sensors.

The temperature is output according to Table 38 as a 16-bit value in two's complement format with a resolution of 0.5°C.

TEMP	Addr 0x6B, 0x6A, bits: 15..8, 7..0	
Code	Temperature	Validity
0x7FFF ...	+16383.5 °C ...	Out of measuring range
0x0190 ... 0x0001 0x0000 0xFFFF ... 0xFFB0	+200.0 °C ... +0.5 °C 0.0 °C -0.5 °C ... -40.0 °C	Measuring range
... 0x8000	... -16384.0 °C	Out of measuring range

Table 38: Temperature data

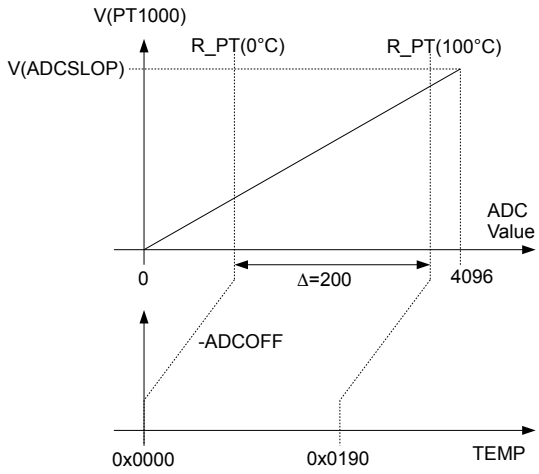

Figure 18: Calibrating the temperature sensor to the output format

To obtain the output given in Table 38 the evaluation circuitry is calibrated as follows:

1. The maximum convertible voltage is set and thus the increase in the converter using the register ADCSLOP. ADCSLOP's register is set so that there is a difference of 200 between the converter values at R(PT1000,0°C) = 1,000 Ω and R(PT1000,100°C) = 1,385 Ω.
2. To map ADC's output to the range of values given in Table 38, an offset is added through register ADCOFF. The data in register ADCOFF is set so that 0x0000 is read at R(PT1000) = 1,000 Ω and, correspondingly, 0x00C8 at R(PT1000) = 1,385 Ω.
   (a) Read converter data from register TEMP with ADCOFF = 0x0000 at R(PT1000) = 1,000 Ω.
   (b) Calibration data = converter data
   (c) Write the calibration data to register ADCOFF.

INTERPOLATION AND CYCLE COUNTING

The configurable 37-bit cycle counter is tracking the sin/cos signal cycles by a comparator, independently of the interpolation and requests of position data.

If position data is requested, the applied and conditioned sin/cos signals are further resolved by the interpolator, at a fixed resolution of 13 bit. The interpolator synchronizes the cycle counting afterwards, so that a consistent position data word is provided.

Register RESO_CC adjusts the cycle counter length, respectively the singleturn resolution which must fit the sin/cos cycle count per revolution.

RESO_CC	Addr. 0x1B; bit 1...0			R/W
Code	Counter Length	Multiturn Counting	Singleturn Counting	Sin/Cos Cycles
00	37 bit	24 bit	13 bit	8192 CPR*
01	36 bit	24 bit	12 bit	4096 CPR
10	35 bit	24 bit	11 bit	2048 CPR
11	34 bit	24 bit	10 bit	1024 CPR
Note	*) Signal cycles per revolution.			

Table 39: Cycle counter length

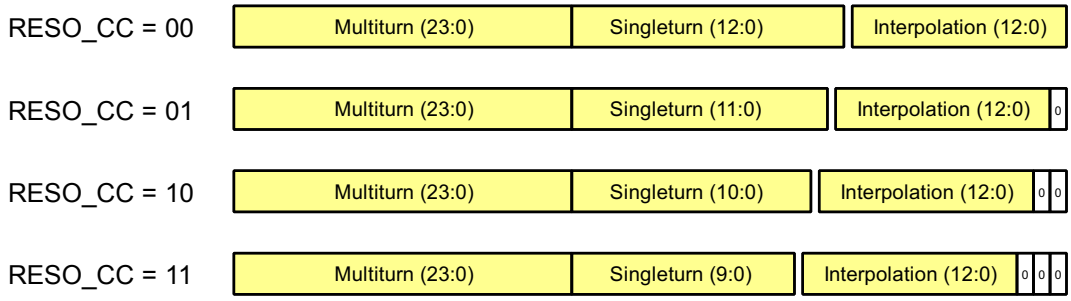

Figure 19: Adjusting the counter length

Adjustment of data direction

The parameter DIR selects between an increasing or decreasing code direction in relation to the mechanical movement, respectively the direction of rotation.

DIR	Addr. 0x1B; bit 2	R/W
Code	Code direction	
0	Code direction not inverted	
1	Code direction inverted	

Table 40: Code direction

Position preset by offset correction

An offset for singleturn (OFFS_ST) and multiturn (OFFS_MT) data can be defined to adjust the absolute position data to a mechanical position. These offsets are subtracted from the existing data.

Note: iC-MR3 does not feature a preset function to zeroize the position data.

OFFS_ST	Addr. 0x1E; bit 7...0 Addr. 0x1D; bit 7...0 Addr. 0x1C; bit 7...0 Addr. 0x1B; bit 7...6	R/W
Code	Function	
0x00 0x3FFFFFF	Offset value	

Table 41: Singleturn offset

OFFS_MT	Addr. 0x21; bit 7...0 Addr. 0x20; bit 7...0 Addr. 0x1F; bit 7...0	R/W
Code	Function	
0x00 0xFFFFFF	Offset value	

Table 42: Multiturn offset

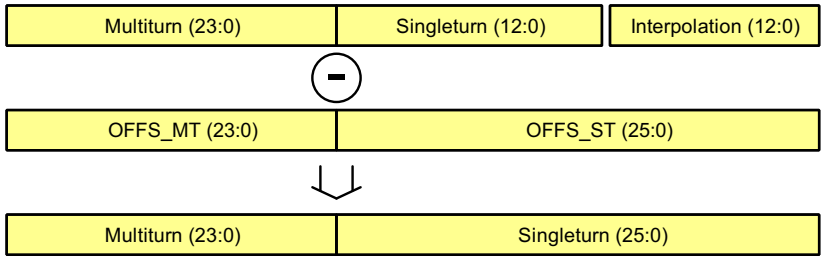

Figure 20: Position data generation with offset correction

Multiturn data length
RESO_MT selects the resolution of the multiturn data for the parallel I/O interface, the SPI, and the serial interface protocols (BiSS, extended SSI, and 13-bit/25-bit SSI).

If the MT resolution is reduced, the multiturn data is right-justified and the upper bits are zeroed. The total output data length can be longer depending on the selected output interface.

RESO_MT	Addr. 0x24; bit 7...5		R/W
Code	MT resolution: serial SPI or parallel	MT resolution: BiSS or ext. SSI	MT resolution: 13-bit / 25-bit SSI
0x0	24 bit	24 bit	n/a
0x1	20 bit	20 bit	n/a
0x2	16 bit	16 bit	n/a
0x3	12 bit	12 bit	12 bit : 25-bit SSI
0x4	8 bit	8 bit	n/a
0x5	4 bit	4 bit	n/a
0x6	0 bit	0 bit	0 bit : 13-bit SSI
0x7	0 bit	0 bit	n/a

Table 43: Multiturn resolution

Singleturn data length
RESO_ST selects the resolution of the singleturn data for the parallel I/O interface, the SPI, and the serial interface protocols (BiSS, extended SSI, and 13-bit/25-bit SSI).

If the ST resolution is reduced, the data is left-justified. If the output data length is longer, depending on the selected output interface, the data is filled with zeros. This generates a permanently coherent position data word from the right-aligned multiturn data and the left-aligned singleturn data.

The interpolator data resolution of 13 bit is fixed; only its position in the data word can be shifted by RESO_CC (Table 39).

RESO_ST	Addr. 0x24; bit 4...0		R/W
Code	ST resolution: serial SPI or parallel	ST resolution: BiSS or ext. SSI	ST resolution: 13-bit / 25-bit SSI
0x00	26 bit	26 bit	n/a
0x01	25 bit	25 bit	n/a
0x02	24 bit	24 bit	n/a
...	...	...	...
0x0D	13 bit	13 bit	13 bit
0x0E	12 bit	12 bit	n/a
...	...	...	...
0x19	1 bit	1 bit	n/a
0x1A	0 bit	0 bit	n/a
...	...	...	...
0x1F	0 bit	0 bit	n/a

Table 44: Singleturn resolution

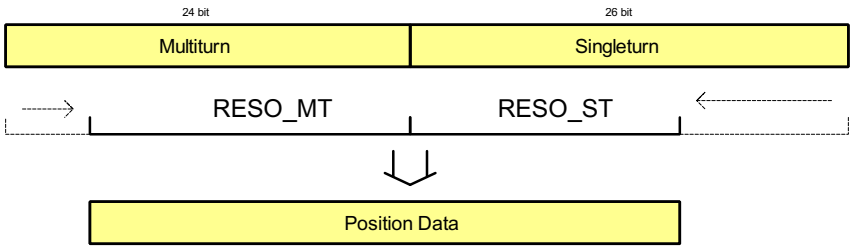

Figure 21: Reduction of data length

Position data acquisition modes
There are three different operating modes for acquiring position data which are selected by ACQMODE.

In **normal conversion** mode, new data is generated on each request for position data and then output after end of conversion.

ACQMODE	Addr. 0x19; bit 7...6	R/W
Code	Function	
00	Normal conversion with processing time	
01	Pipeline conversion without processing time	
10	Continuous conversion without processing time * (Using BiSS, data is output after the PDV bit appeared.)	
11	Continuous conversion with interpolation of interim values *	
Note	*) Only for serial I/O interface with SSI protocol	

Table 45: Position data acquisition

In **pipeline conversion** mode, data is also generated on each request, however, with each new request the data from the last conversion is output in order to hide the processing time. In this mode, the PDV bit is set statically in the status register and the ERR_IPO bit in the error register continues to signal the status or processing time of the interpolator. Pipeline mode is available in both the parallel and the serial I/O interfaces with the SSI and BiSS C protocol.

Note: Position data of a foregoing conversion is output along with error and warning bits based on current status conditions. Thus, the error and warning bits of a single data frame may not identify faulty position data.

Note: If using the ADI together with pipeline conversion, this can result in a position data jump when the startup initialization of the counting comes late.

In **continuous conversion** mode, position data is updated automatically regardless of external requests in intervals of 64 clock cycles (approx. each 4.3 µs for an oscillator frequency of 15 MHz). The data output comes from the most recent conversion with the advantage of immediate availability, but the read data is not necessarily up to date.

In **continuous conversion with interpolation** of interim values, interpolated intermediate position data can be output at any time. This conversion mode is only available with the serial I/O interface in SSI, as SSI limits the acquisition time depending on the clock rate.

If a continuous conversion mode is active (ACQMODE = 10 or 11), conversion can be temporarily interrupted by pin NL using the enable acquire function.

NL (Enable Acquire Function)	
Level	Function
1	Convert as soon as the interpolator is free
0	Do not convert

Table 46: Special function of pin NL

ABSOLUTE DATA INTERFACE (ADI)

Using the serial absolute data interface (ADI), the 37-bit cycle counter can be preloaded with a start value. For this, steady sin/cos input signals are not required as the cycle counter does not pause tracking the sin/cos signal cycles.

The ADI uses pin AMAO to output the master clock, and pin ASLI to take back the slave's data. The interface consists of a BiSS master which can be configured for BiSS C or SSI.

SSI_ADI	Addr. 0x1A; bit 0	R/W
Code	Function	
0	BiSS C protocol	
1	SSI protocol	

Table 47: Protocol of the absolute data interface

SLOW_ADI	Addr. 0x2B; bit 7	R/W
Code	Function	
0	Normal: clock division by 2 (by 16 for SSI)	
1	Slow: clock division by 8 (by 64 for SSI)	

Table 48: Clock rate absolute data interface

BiSS Master Performance		
Parameter	Symbol	Description
Clock Rate	t_C	7.5 MHz (normal, @ f_{osc} = 15 MHz) 1.875 MHz (slow)
Line Delay	t_{P0}	Not adaptive, 80 ns max. accepted
Process.T.	t_{busy}	Up to 1021 clock cycles maximum: 135 µs (normal), 540 µs (slow)
Timeout	t_{out}	Accepted between 200 ns to 40 µs
Single-cycle Data Channel		
Bits/cycle	ID	Description
0...48	DATA	Adjustable to absol. position data of: MT 0, 8, 12, 16, 24 bit (right-justified) ST 0 to 24 bit with sync. of 0 to 3 bit (left-justified)
1	nE*	Error bit: triggers ERR_ABS (refer to register ERROR)
1	nW*	Warning bit: ignored (not evaluated and not forwarded)
6	CRC	Polynomial 0x43 ($x^6 + x^1 + x^0$), start value 0x00 (bit inverted transmission)
Control Data Channel		
Bits/cycle	ID	Description
1	CDS	Not evaluated by the iC-MR3
Note	*) low active transmission.	

Table 49: BiSS master performance (ADI)

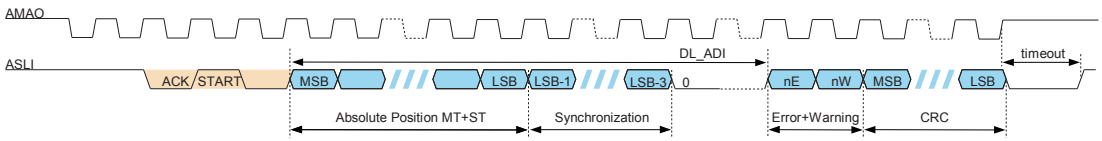

Figure 22: ADI data frame with BiSS protocol

SSI Master Performance		
Parameter	Symbol	Description
Clock Rate	t_C	940 kHz (normal, @ f_{osc} = 15 MHz) 235 kHz (slow)
Timeout	t_{out}	Accepted between 1 µs to 40 µs
Single-cycle Data Channel		
Bit/cycle	ID	Description
0...48	DATA	Adjustable to absol. position data of: MT 0, 8, 12, 16, 24 bit ST 0 to 24 bit with sync. by 0 to 3 bit

Table 50: SSI master performance (ADI)

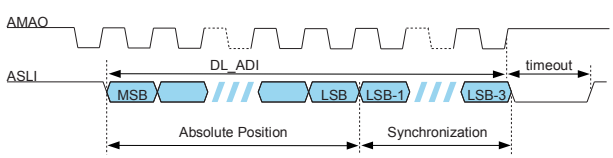

Figure 23: ADI data frame with SSI protocol

DL_ADI	Addr. 0x1A; bit 7...3	R/W
Code	Data Length*	Application Example
0x00	0 bit	
0x01	1 bit	1 bit ST
...	...	
0x0E	**14 bit**	**11 bit ST with 3 sync. bits**
...	...	
0x18	24 bit	24 bit ST*
0x19	32 bit	8 bit MT plus 24 bit ST*
0x1A	36 bit	12 bit MT plus 24 bit ST*
0x1B	**40 bit**	**16 bit MT plus 24 bit ST*** (refer to example of Fig. 24)
0x1C...1F	48 bit	24 bit MT plus 24 bit ST*
Note	*) Total bit count including synchronization bits.	

Table 51: Data length absolute data interface

The register DL_ADI defines the data length read in by the absolute data interface.

Register SBL_ADI defines how many lower significant bits of the ADI data are exceeding the period information, and thus are representing a half or less of a sin/cos signal cycle. These bits are called synchronization bits and are used for the initialization of the cycle counter depending on the interpolated angle.

SBL_ADI	Addr. 0x1A; bit 2...1	R/W
Code	Function	
00	Use 0 bit for synchronization	
01	Use 1 bit for synchronization; synchronization range ± 90 °	
10	Use 2 bit for synchronization; synchronization range ± 135 °	
11	Use 3 bit for synchronization; synchronization range ± 157.5 °	
Note	The synchronization range is the data's variation in phase relative to the sine signal's zero crossing.	

Table 52: Absolute data synchronization

The register SPO_ADI allows an alignment of the external absolute data to the sin/cos phase angle, wheras the step size depends on the setting of SBL_ADI. For SBL_ADI = 00 (no sync bits), the singleturn data is taken over unchanged. As SPO_ADI is always added onto SYNC(2:0), negative SPO_ADI values (0x9 to 0xF) may be used to substract a whole sine period from the singleturn data. Positive SPO_ADI values (0x0 to 0x7) have no effect.

For SBL_ADI = 11 (3 sync bits), SPO_ADI is again added onto SYNC(2:0), now allowing shifts of ± 1/8 sine period by values of ± 1, for example. As in Figure 24, the value of SPO_ADI is added to the 'ADI Content', i.e. to the singleturn and sync bits. If using the synchronization is desired, the ADI sensor could also supply 3 additional zero bits, on which SPO_ADI then acts with a step size of 45°.

SPO_ADI	Addr. 0x2C; bit 6...3		R/W
Code	Function	Code	Function
0x0	none	0x8	none
0x1	+ 1	0x9	– 1
0x2	+ 2	0xA	– 2
...	...	...	...
0x7	+ 7	0xF	– 7
Note	The correction value is added, respectively substracted, to the ADI Data Content (refer to Fig. 24)		

Table 53: Absolute data adjustment

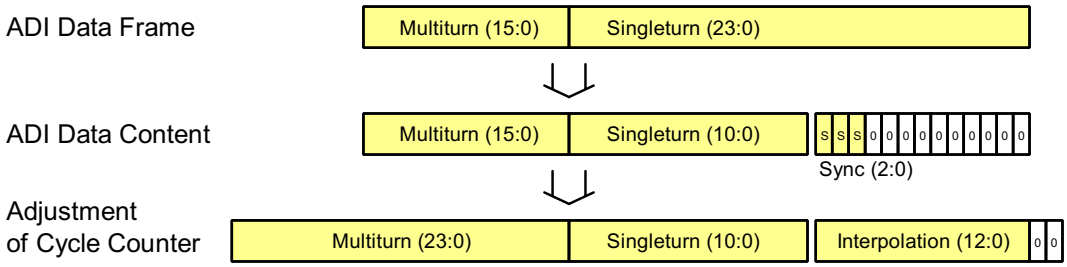

Figure 24: Initialization of the cycle counter. Example of a 16-bit multiturn encoder with a 14-bit singleturn featuring sin/cos signals of 2048 CPR. The lowest 3 bit of ST data are overlapping the sin/cos cycles and are used for synchronization.
Setup: DL_ADI = 0x1B (40 bit), SBL_ADI = 11 (3 bit), RESO_CC = 10 (35 bit)

STP_ADI	Addr. 0x18; bit 3	R/W
Code	Function	
0	Startup without reading absolute data: the cycle counter starts from zero.	
1	Startup with reading absolute data: the cycle counter is preset [1, 2].	
Notes	The startup is monitored and updates the status bit ADV (see page 60). [1] iC-MR3 Z, Z1: In case of a failure (no reply or CRC error), the read access will be repeated once. If the error persists, the cycle counter starts from zero. [2] iC-MR3 Z2: In case of a failure (no reply, CRC error, or BiSS error bit set), the read access will be repeated until the error is gone[3]. The cycle counter is kept zeroed as long as an error persists (BiSS returns only zeroes, i.e. error and warning bit is set). [3] Refer to Design Review, page 63, for details.	

Table 54: Startup with absolute data

The bit STP_ADI controls how the absolute data are read during startup. If set, and after the EEPROM has been successfully read, absolute data is read in by the ADI and the cycle counter is preset. Alternatively, absolute data can be read in at a later stage by command.

CYC_ADI	Addr. 0x18; bit 2	R/W
Code	Function	
0	No cyclic reading of absolute data	
1	Cyclic reading of absolute data: for counter verification (CHK_ADI = 1) or counter initialization (CHK_ADI = 0)	

Table 55: Cyclic reading of absolute data

The bit CYC_ADI controls the cyclic reading of absolute data. If set, the absolute data is read in intervals of approx. 550 µs, provided the absolute data interface is not busy.

Note: Use either one-time reading (startup with absolute data) or cyclic reading modes. The bit STP_ADI should not be active together with a cyclic operating mode (CYC_ADI = 1).

CHK_ADI	Addr. 0x27; bit 5	R/W
Code	Function	
0	No counter verification	
1	Cyclic counter verification against ADI absolute data	
Note	Set CYC_ADI = 0 ahead of changing CHK_ADI.	

Table 56: Cyclic check of absolute data

The bit CHK_ADI is used to check the counted value against a cyclically read absolute value. If the two values differ, error bit ERR_ABS will be set.

Suggested configurations

A) Using the ADI for initialization, and continue with cycle counting: STP_ADI = 1, CYC_ADI = 0, CHK_ADI = 0.

B) Using the ADI for initialization, continue with cycle counting and consistency checking of absolute angle: STP_ADI = 0, CYC_ADI = 1, CHK_ADI = 1.

C) Using the ADI for cyclic initialization: STP_ADI = 0, CYC_ADI = 1, CHK_ADI = 0
A possible setting at the expense of readout delays, as the ADI repeats data input.

Note: The CHK_ADI bit should not be changed while the cyclic operation is active, otherwise malfunction may occur.

Note: When using the cyclic counter initialization (CYC_ADI = 1 with CHK_ADI = 0):
When reading position data via the parallel I/O interface, triggered by a low signal at pin NL, the response may be delayed if the sin/cos interpolator is used by the ADI engine to set the cycle counter.

Note: A read command from the serial I/O interface using the BiSS C protocol will be answered immediately.
Note that the single-cycle data channel returns only zeroes (i.e. error and warning bit is set) if the internal data bus is busy (after power-on until data is available, during a CRC verification, or when writing the configuration to the EEPROM).

Note: If the serial I/O interface is operated in SPI mode in conjunction with cyclic read (CYC_ADI = 1, and CHK_ADI = 0), position values must be requested at pin NL by a low signal.

Direct communication with the sensor at ADI

In order to access the BiSS C sensor connected to the absolute data interface, the bit GET_ADI allows the interface signals to be directly connected to the I/O interface.

For this to happen, the master clock received at clock input MAI is forwarded to clock output AMAO, and the data read at ASLI is used internally in place of input SLI. The sensor connected to the ADI is then allocating slave ID 0, and iC-MR3 is taking slave ID 1 and 2.

When routing the interfaces in this manner, iC-MR3 can not process the ADI data internally. If that is required, disable bit GET_ADI first.

GET_ADI	Addr. 0x18; bit 4	R/W
Code	Function	
0	Normal operation	
1	ADI operated in BiSS chain Note that iC-MR3 can not process the data received at ADI.	

Table 57: Absolute data interface daisy chain

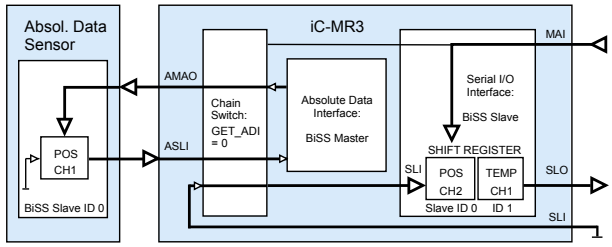

Figure 25: Normal operation

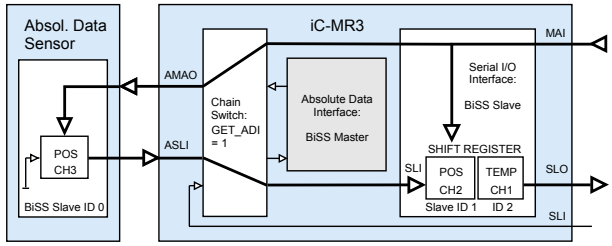

Figure 26: ADI operated in BiSS chain.
iC-MR3 now occupies slave ID 1 and 2.

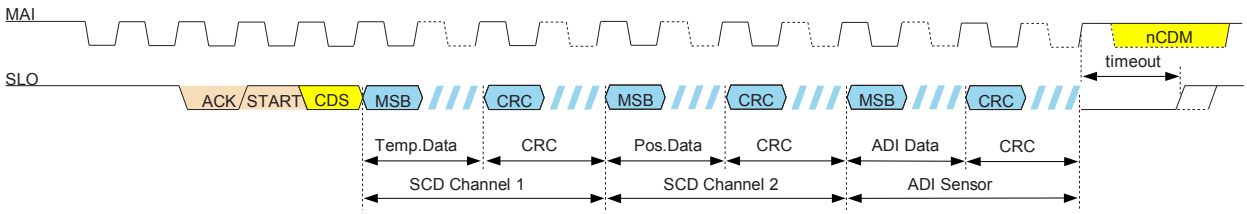

Figure 27: BiSS data output at the I/O interface during ADI chain operation.

STARTUP AND I/O INTERFACE SELECTION

Startup with EEPROM

Upon power-on and undervoltage reset, the iC-MR3 accesses the external EEPROM to source its CRC-protected configuration data.

If the configuration data is not confirmed by its CRC in the first attempt (for example when an EEPROM is connected up that has not yet been programmed), all configuration registers are zeroed, the error bit ERR_KNF is set, and the serial I/O interface is activated with the SSI protocol.

Additionally, the data output SLO is kept permanently high (at VDD level) to block the transmission of invalid position data.

Note: A locked output SLO can only be resolved by a successful CRC verification over renewed configuration data. For this purpose, the iC-MR3 evaluates the BiSS control bit CDM even during SSI.

Startup without EEPROM

Without an EEPROM, or if after three attempts no successful I^2C communication has been established with the EEPROM (lack of acknowledgement would indicate that the EEPROM is faulty or not connected), all configuration registers are zeroed and the error bit ERR_KNF is set.

In this case the pin levels of SCL and SDA are evaluated and preset register INTCFG:
INTCFG(1) is set by the pin level of SCL and
INTCFG(0) by the pin level of SDA.

Startup without EEPROM		
SCL Level	SDA Level	Activated Interface
1	1	Parallel I/O interface
1	0	Serial I/O interface with SPI protocol
0	0	Serial I/O interface with SSI protocol
0	1	Not permissible
Notes	Any change of static pin levels requires a power cyle to take impact. Note that the configuration error ERR_KNF will be set in any case.	

Table 58: Interface selection without EEPROM

I/O Interface selection

Register INTCFG selects if the parallel or the serial I/O interface is used, and which serial communication protocol (BiSS, SSI, or SPI). Only one of the two interfaces may be active.

During startup, the register INTCFG is usually configured by the connected EEPROM. However, during operation it is possible to edit INTCFG without an immediate impact on the function. The change then needs to be stored to the EEPROM and takes effect after a power cycle.

INTCFG	Addr. 0x18; bit 7...6	R/W
Code	Function	
11	Parallel I/O interface	
10	Serial I/O interface with SPI protocol	
00	Serial I/O interface with BiSS protocol (NESSI = 1) or SSI protocol (NESSI = 0)	
01	Not permissible	

Table 59: Interface selection

PARALLEL I/O INTERFACE

The parallel I/O interface enables sensor and register data to be read through pins NCS, NRD, NWR, NL, and D0 to D7. After a reset or when inactive, the interface is in read mode (data pins D(7:0) are tristate, address transfer is expected). If the internal data bus is busy due to an EEPROM read after the reset, for instance (i.e. if the BUSY bit is active in the status byte), all reads are answered by the status byte through the parallel I/O interface.

Note: The parallel I/O interface can not be simultaneously operational with a serial I/O interface, as the pins D7...0 output the status register in this case.

Note: The parallel I/O interface supports 6.25 MHz as read clock at pin NRD (for timing details refer to Elec. Char. I108 and I109 on page 15).

Reading from registers

iC-MR3's parallel I/O interface enables internal registers to be read accessed. The required register address must first be written to, after which the data at this address can be read out.

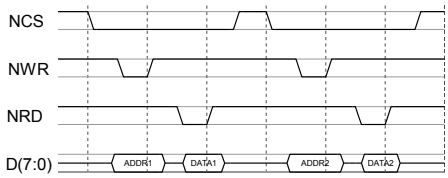

Figure 28: Read process

Writing to registers

The internal registers can be written to through the parallel I/O interface. The required register address and then the relevant data word must be written. The write mode is selected by NWR = 0. The first write sets the register address and has no effect on the register content. The second write writes the data at the bus to the addressed register.

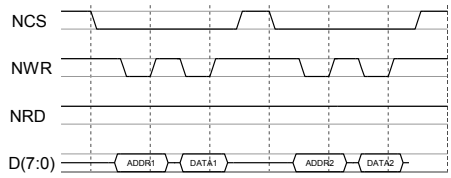

Figure 29: Write process

A simultaneous low signal for NRD and NWR is not permissible; the interface behavior is not defined for this configuration.

Reading position data

Position data can be requested through the parallel I/O interface in two different ways:

- by an implemented command
- by a low signal through pin NL.

To read position data on an implemented command, command register CMD must be written to with the request command 0x00. Depending on the set configuration, singleturn, multiturn, and interpolator data is then provided to be read. Each request command increases the sign-of-life counter by one.

Position data is marked as valid by bit PDV being set in the status register. Only after this has occurred, position data should be read from the relevant register addresses. Here, a normal read command is used to read the data.
If it is not possible to extend the NRD pulse to wait for data validity, the status register must be continually read again until pin D0 supplies a high (PDV = 1). After this, the position data can be read using a read command.

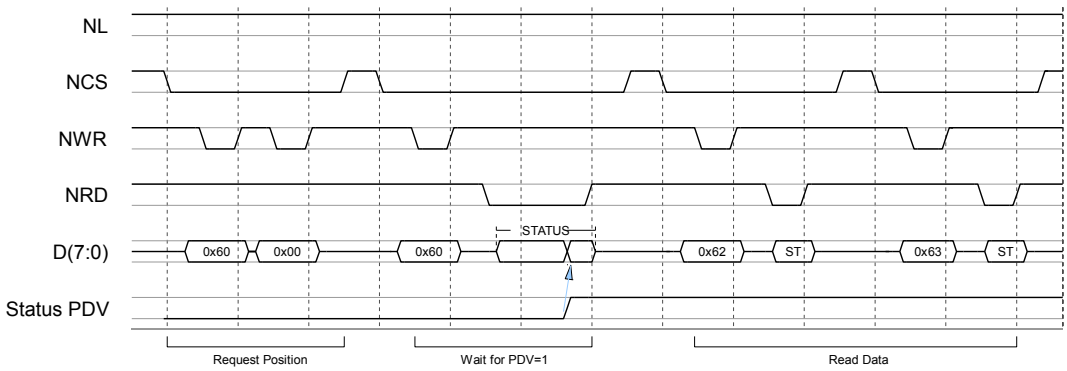

Figure 30: Position data output at request by command

As the position data registers are read individually following a request for position data by command, no CRC is formed across the position data. The sign-of-life counter function continues to be active, however.

When reading out position data through pin NL, the request is made directly on the falling edge at pin NL. While NL = low, the status and position data are output on consecutive read commands (NRD = high → low → high).

It is not necessary to write to the register addresses in this operating mode, as this is only used to read the sensor data quickly.

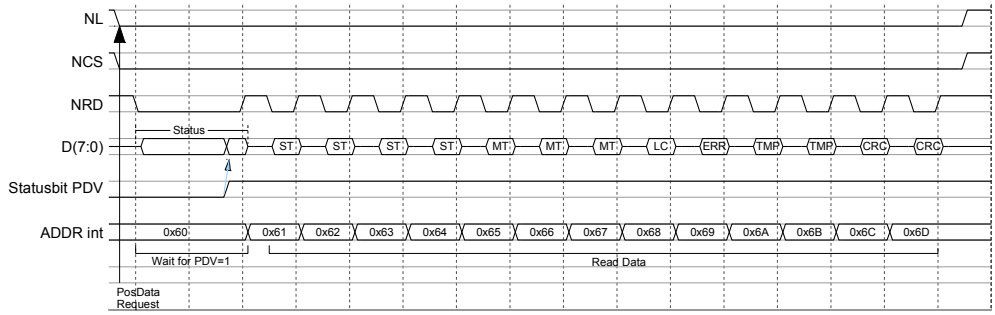

Figure 31: Position data output at request by pin NL

The status register data is output first. During the status register read, NRD should remain low until pin D0 (in this case, PDV) switches to high, as this indicates the validity of the position data.

On each rising edge at NRD the internal address is increased, after which the position data can be read with each low signal at NRD.

The various ways of outputting position data in this operating mode are set in register FULL_CYC. If the bit FULL_CYC is set (Table 60), registers 0x60-0x6D are output on each cyclic read. If this bit is disabled, registers 0x61 and 0x67 are bypassed; only 24 bits of singleturn and 16 bits of multiturn data are output.

FULL_CYC	Addr. 0x18; bit 5	R/W
Code	Function	
0	24-bit ST / 16-bit MT	
1	26-bit ST / 24-bit MT	

Table 60: Cyclic frame length

A CRC is formed across the output data (with the polynomial $x^{16} + x^{14} + x^{11} + x^{10} + x^9 + x^7 + x^5 + x^3 + x^1 + 1$ (0x14EAB), start value 0xFFFF). The checksum is reformed for each cyclic transmission and is only valid for the duration of this transmission. The following sequence applies to the shortened output format (FULL_CYC = 0):

Data sequence shortened format (FULL_CYC = 0)			
Byte No.	Data	Register	Address
1	Status byte	STAT(7:0)	0x60
2	Singleturn Lo byte	ST(9:2)	0x62
3	Singleturn Mid byte	ST(17:10)	0x63
4	Singleturn Hi byte	ST(25:18)	0x64
5	Multiturn Lo byte	MT(7:0)	0x65
6	Multiturn Mid byte	MT(15:8)	0x66
7	Sign-of-life counter	LC(7:0)	0x68
8	Error byte	ERR(7:0)	0x69
9	Temperature Lo byte	TEMP(7:0)	0x6A
10	Temperature Hi byte	TEMP(15:8)	0x6B
11	CRC Lo byte	CRC(7:0)	0x6C
12	CRC Hi byte	CRC(15:8)	0x6D

Table 61: Data sequence shortened output format

If more bytes are read out in cyclic operation, a zero is always output. In full output format (FULL_CYC = 1) the data is output in the following order:

Data sequence complete format (FULL_CYC = 1)			
Byte No.	Data	Register	Address
1	Status byte	STAT(7:0)	0x60
2	Singleturn Ext byte	ST(1:0)	0x61
3	Singleturn Lo byte	ST(9:2)	0x62
4	Singleturn Mid byte	ST(17:10)	0x63
5	Singleturn Hi byte	ST(25:18)	0x64
6	Multiturn Lo byte	MT(7:0)	0x65
7	Multiturn Mid byte	MT(15:8)	0x66
8	Multiturn Hi byte	MT(23:16)	0x67
9	Sign-of-life counter	LC(7:0)	0x68
10	Error byte	ERR(7:0)	0x69
11	Temperature Lo byte	TEMP(7:0)	0x6A
12	Temperature Hi byte	TEMP(15:8)	0x6B
13	CRC Lo byte	CRC(7:0)	0x6C
14	CRC Hi byte	CRC(15:8)	0x6D

Table 62: Data sequence complete output format

SERIAL I/O INTERFACE: BiSS C

The serial I/O interface operates using the BiSS C protocol and allows sensor data to be transmitted in repeated and uninterrupted cycles (data channel SCD1, and optional channel SCD2). Simultaneously, parameters can be exchanged through bidirectional register communication (data channel CD).

Depending on the configuration, the sensor data output by the iC-MR3 contains the cycle counter and interpolation data of up to 50 bits, two error bits, a sign-of-life counter of 6 bits, and 6 or 16 CRC bits. Another SCD channel can be linked in to transmit the temperature data from the 12-bit A/D converter at a length of 16 bits. The BiSS device data (registers PRO_ID, DEV_ID) can be programmed separately for both single-cycle data channels.

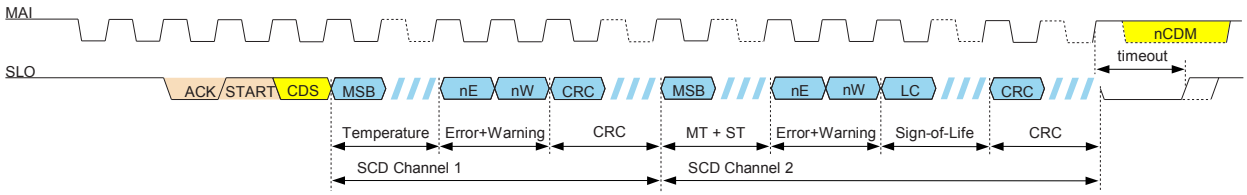

Figure 32: Example of line signals (BiSS C)

BiSS Slave Performance		
Parameter	Symbol	Description
Clock Rate	t_C	10 MHz max.
Process.T.	t_{busy}	typ. 2 µs
Timeout	t_{out}	adaptive (typ. 0.35 µs @ 10 MHz) fixed (typ. 20 µs)
Inp. Buffer		15 bit max. for SLI data buffering [5]
SCD Channel 1: Temperature Data [3]		
Bits/cycle	ID	Description
16	TEMP	Temperature Data
1	nE [1]	Error bit: ERR_TMP
1	nW [1]	Warning bit = 1 (not in use)
5	CRC [2]	Polynomial 0x25, start value zero
SCD Channel 2: Position Data [4]		
Bits/cycle	ID	Description
0, 4, 8, 12, 16, 20, 24	MT	Multiturn Data (right-justified)
0 ... 26	ST	Singleturn Data (left-justified)
1	nE [1]	Error bit ERR
1	nW [1]	Warning bit WARN
(6)	LC	Sign-of-life Counter
6 (16)	CRC [2]	Polynomial 0x43 (0x190D9), adjustable start value.
CD Channel: Control Data		
Bits/cycle	ID	Description
1	nCDM [1], CDS	Support of bidirectional register access
	Slave IDs	1 or 2 [3]
	Commands	Support of selected BiSS Commands according to Table 72.
Notes	[1] Low active. [2] Bit inverted transmission. [3] If temperature data is enabled (ENTS = 1). [4] This channel can not switch off; a minimum of 9 bits is transmitted for CDS, nE, nW and CRC. [5] When operated in BiSS chain, the max. clock rate is 5 MHz as iC-MR3 requires processing time.	

Table 63: BiSS slave performance

Configuration

The following parameters define the serial I/O interface in BiSS C protocol:

NESSI	Addr 0x19, bit 4	
Code	Protocol	Information
0 1	SSI BiSS C	BiSS INTERFACE www.biss-interface.com

Table 64: BiSS/SSI protocol selection

ENLC enables the sign-of-life counter to be transmitted on the single-cycle data channel. The counter data is sent directly after the nE and nW bit.

ENLC	Addr. 0x19; bit 5	R/W
Code	Function	
0	Sign-of-life counter disabled	
1	Output of 6-bit sign-of-life counter	

Table 65: Sign-of-life counter enable

CRC16 selects the CRC polynomial used and the number of CRC bits transmitted. Here, CRCS allows a free start value to be programmed for CRC calculation. If the 6-bit CRC is chosen, only CRCS bits 5 to 0 are used.

CRC16	Addr. 0x19; bit 3	R/W
Code	Function	
0	6-bit CRC with polynomial 0x43 = $x^6 + x^1 + 1$	
1	16-bit CRC with polynomial 0x190D9 = $x^{16} + x^{15} + x^{12} + x^7 + x^6 + x^4 + x^3 + 1$	

Table 66: 16-bit CRC polynomial

CRCS(15:8) **CRCS(7:0)**	Addr. 0x28; bit 7...0 Addr. 0x29; bit 7...0	R/W
Code	Function	
0x00 ... 0x3F	Start value for 6-bit CRC calculation Only the bits CRCS(5:0) are relevant.	
0x0000 ... 0x0460 (0xFFFF)	Start value for 16-bit CRC calculation Recommended maximum CRC start value.	

Table 67: CRC start value

If enabled by ENTS, temperature data is transmitted in an additional single-cycle data channel.

ENTS	Addr. 0x19; bit 2	R/W
Code	Function	
0	Temperature data disabled SCD channel 1: position data	
1	Temperature data enabled SCD channel 1: temperature data with 5-bit CRC (polynomial 0x25 = $x^5 + x^2 + 1$; start value 0x00) SCD channel 2: position data	

Table 68: Temperature data enable

Note: The single-cycle data channel returns only zeroes (i.e. error and warning bit is set) if the internal data bus is busy (after power-on until data is available, during a CRC verification, or when writing the configuration to the EEPROM).

NPD_SLI	Addr. 0x2C; bit 7	R/W
Code	Function	
0	Pull-down at input SLI active	
1	Pull-down at input SLI disabled	
Note	When the configuration error ERR_KNF is active, the pull-down source does not disable.	

Table 69: SLI Pull-down disable

Adaptive Timeout
The iC-MR3 can provide a fixed or adaptive BiSS timeout depending on the setting of parameter NTOA. For fastest communication speed, it is recommended to use the adaptive timeout.

NTOA	Addr. 0x2C; bit 2	R/W
Code	Function	
0	Adaptive timeout	
1	Fixed timeout	
Note	Refer to Elec.Char. O09 for timing specifications.	

Table 70: Adaptive timeout (low active)

If NTOA = 1, a fixed nominal timeout of 20 µs (with a 14 MHz system clock) is used (refer to Elec. Char. item no. M01 and O09).

If NTOA = 0, the iC-MR3 adapts the BiSS timeout length based on the period of the BiSS MA clock, T_{MA}, and its internal sampling frequency, $1/T_{CLK}$, to ensure fastest communication. In operation, the iC-MR3 measures 1.5 periods of MA (from the first falling to the second rising edge) of each BiSS frame and calculates an adaptive timeout value of

$$T_{CLK} = \frac{4}{3 * fosc}$$

Where fosc is the chip's oscillator frequency (refer to Elec. Char. item no. M01 and O09).

Timeout	**Condition**	**Min.**	**Max.**
t_{out}	$T_{CLK} \leq 1.5 * T_{MA}$	$1.5 * T_{MA}$	$1.5 * T_{MA} + 3.0 * T_{CLK}$
	$T_{CLK} \geq 1.5 * T_{MA}$	$1.0 * T_{CLK}$	$1.5 * T_{MA} + 3.0 * T_{CLK}$

Table 71: Adaptive timeout calculations

For more information on the BiSS adaptive timeout, refer to BiSS application note AN23 at www.biss-interface.com.

Register communication
According to the BiSS C protocol, slave registers are directly addressed in a reserved address area (0x40 to 0x7F). Other memory areas are addressed dynamically and in blocks. For this purpose BiSS addresses 0x00 to 0x3F aim at a register block of 64 bytes, of which, the physical storage address is determined by the bank selection parameter BSEL(4:0). The iC-MR3 supports up to 32 memory banks, enabling a 16-Kbit EEPROM to be fully used. This means that there is sufficient storage space for an ID plate (EDS) and OEM data.

Page 54 provides information on memory allocation and addressing through BiSS.

BiSS protocol commands

The following BiSS interface protocol commands are implemented. These commands cannot be executed as a broadcast command.

CD Channel: BiSS Commands		
CMD	Availability	Function
Addressed		
00	—	Activate Single-Cycle Data channels
01	—	Deactivate control communication
10	Yes	Read new data via absolute data interface
11	Yes	CRC verification of internal configuration
Broadcast (all slaves)		
00	—	Deactivate Single-Cycle Data
01	—	Activate control communication
10	—	Reserved
11	—	Reserved

Table 72: BiSS Protocol Commands

Configuration examples

Singleturn data		
Bits	ID	Description
24	ST	Singleturn value ST(23:0)
2	nE, nW	Error nE and warning nW
6	CRC	Polynomial 0x43
Config.	NESSI = 1, ENLC = 0, ENTS = 0, CRC16 = 0, RESO_ST = 0x02, RESO_MT = 0x7	

Table 73: Format example 1 for BiSS profile BP1

Singleturn and multiturn data		
Bits	ID	Description
24	MT	Multiturn value MT(23:0)
12	ST	Singleturn value ST(11:0)
2	nE, nW	Error nE and warning nW
6	CRC	Polynomial 0x43
Config.	NESSI = 1, ENLC = 0, ENTS = 0, CRC16 = 0, RESO_ST = 0x0E, RESO_MT = 0x0	

Table 74: Format example 2 for BiSS profile BP1

ST and MT data with sign-of-life counter and temperature		
Bits	ID	Description
16	TEMP	Temperature value TEMP(15:0)
2	nE, nW	Error nE and warning nW
5	CRC	Polynomial 0x25
12	MT	Multiturn value MT(11:0)
26	ST	Singleturn value ST(25:0)
2	nE, nW	Error nE and warning nW
6	LC	Sign-of-life counter LC
16	CRC	Polynomial 0x190D9
Config.	NESSI = 1, ENLC = 1, ENTS = 1, CRC16 = 1, RESO_ST = 0x00, RESO_MT = 0x3	

Table 75: Format example 3

SERIAL I/O INTERFACE: SSI

The iC-MR3 can transmit position data using the SSI protocol, for which purpose the following parameters provide the necessary settings and options. In addition, writing to registers is also possible in SSI mode as BiSS control data (CDM bit) is evaluated.

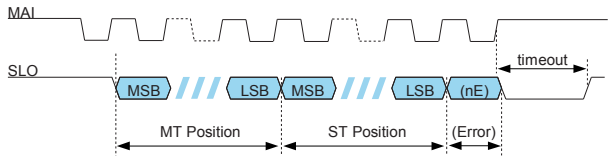

Figure 33: Example of line signals (25-bit Std. SSI)

SSI Slave Performance		
Parameter	Symbol	Description
Clock Rate	t_C	4 MHz max.
Timeout	t_{out}	adaptive (typ. 1.7 µs @ 1 MHz) fixed (typ. 20 µs)
13-bit Standard SSI		
Bits/cycle	ID	Description
13	ST	Singleturn Data
(1)	nE*	Error bit ERR
25-bit Standard SSI		
Bits/cycle	ID	Description
12 (0)	MT	Multiturn Data
13 (25)	ST	Singleturn Data
(1)	nE*	Error bit ERR
Extended SSI		
Bits/cycle	ID	Description
(16)	TEMP	Temperature Data
1	nE*	Error bit: ERR_TMP
1	nW*	Warning bit: 1 (not used)
(5)	CRC	Polynomial 0x25, start value zero (bit inverted transmission)
0, 4, 8, 12, 16, 20, 24	MT	Multiturn Data (right-justified)
0 ... 26	ST	Singleturn Data (left-justified)
1	nE*	Error bit ERR
1	nW*	Warning bit WARN
(6)	LC	Sign-of-life Counter
6 (16)	CRC	Polynomial 0x43 (0x190D9), adjustable start value (bit inverted transmission)
Note	*) low active transmission	

Table 76: SSI slave performance

Configuration

The following parameters define the serial I/O interface in SSI protocol:

NESSI	Addr 0x19, bit 4	
Code	Protocol	Information
0 1	SSI BiSS C	BiSS INTERFACE www.biss-interface.com

Table 77: BiSS/SSI protocol selection

NTOA	Addr. 0x2C; bit 2	R/W
Code	Function	
0	Self-adaptive to clock rate	
1	Fixed (recommended for SSI)	
Note	Refer to Elec.Char. O09 for timing specifications.	

Table 78: Adaptive timeout (low active)

SSIRING	Addr. 0x18; bit 1	R/W
Code	Function	
0	SSI ring mode deactivated	
1	SSI ring mode activated	
SSIERR	Addr. 0x18; bit 0	R/W
0	Standard SSI output without error bit	
1	Standard SSI output with error bit	
SSIMODE	Addr. 0x19; bit 1...0	R/W
00	13-bit SSI protocol	
01	25-bit SSI protocol	
10	Extended SSI protocol (from 8...97 bit)	

Table 79: SSI Configuration

SSIMODE(1:0) defines the data length of the serial I/O interface in SSI protocol. Possible values are a 13-bit SSI, a 25-bit SSI, or an extended mode with data contents as described for the BiSS C protocol.

In 13-bit or 25-bit SSI mode the error bit can be attached to the data by SSIERR.

SSI ring mode can be activated by SSIRING.

Note: Data output in Gray code is not featured by iC-MR3, the output format is always binary.

Configuration examples

Singleturn data		
Bits	ID	Description
13	ST	Singleturn value ST(23:11)
Config.	NESSI = 0, ENLC = 0, ENTS = 0, CRC16 = 0, SSIERR = 0, SSIMODE = 00, RESO_ST = 0x0D, RESO_MT = 0x7	

Table 80: Format example 1 for 13-bit SSI

Singleturn and multiturn data		
Bits	ID	Description
12	MT	Multiturn value MT(11:0)
13	ST	Singleturn value ST(23:11)
1	nE	Error nE
Config.	NESSI = 0, ENLC = 0, ENTS = 0, CRC16 = 0, SSIERR = 1, SSIMODE = 01, RESO_ST = 0x0D, RESO_MT = 0x3	

Table 81: Format example 2 for 25-bit SSI

ST and MT data with sign-of-life counter and temperature		
Bits	ID	Description
16	TEMP	Temperature value TEMP(15:0)
2	nE, nW	Error nE and warning nW
5	CRC	Polynomial 0x25
24	MT	Multiturn value MT(23:0)
26	ST	Singleturn value ST(25:0)
2	nE, nW	Error nE and warning nW
6	LC	Sign-of-life counter
16	CRC	Polynomial 0x190D9
Config.	NESSI = 0, ENLC = 1, ENTS = 1, CRC16 = 1, SSIERR = 0, SSIMODE = 10, RESO_ST = 0x00, RESO_MT = 0x0	

Table 82: Format example 3 for extended SSI

SERIAL I/O INTERFACE: SPI

If SPI is selected for the serial I/O interface, the iC-MR3 operates as an SPI slave supporting modes 0 and 3 (meaning clock input MAI ('SCLK') can be 0 or 1 during idle time).
Data at input SLI ('MOSI' line) is always accepted with the rising clock edge of MAI ('SCLK'), whereas data output at SLO ('MISO' line) change with the falling clock edge of MAI ('SCLK').
The idle state of output SLO ('MISO' line) is high impedance.

Register access

The access mode is initiated by the very first bit received, the CYC bit, selecting between register access and cyclic readout.

CYC	
Code	Function
0	Register access
1	Cyclic readout

Table 83: SPI access mode

If CYC = 0, register access is initiated, which consists of a 3-byte transmission. CYC is followed by a 7-bit address completing the first byte.

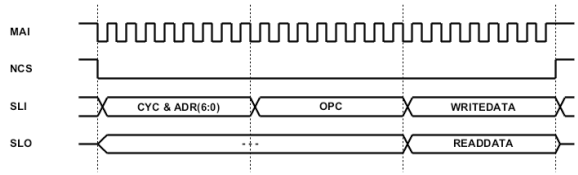

Figure 34: Register access.

The next byte contains the opcode for the transmission: with one bit for register read (RD), one bit for register write (WR), and 4 bit addressing the command register (CMD).

The third and final byte concludes the transmission to/from a register, with which either write data (WRITEDATA) is taken over at pin SLI, or read data (READDATA) is output at pin SLO.

If the internal data bus is busy, due to an EEPROM readout after reset, for instance, all read commands are answered by the status byte (with bit BUSY set).

Command execution

To execute a command, which does not require an exchange of data, the transmission can be terminated after the second byte representing the opcode.

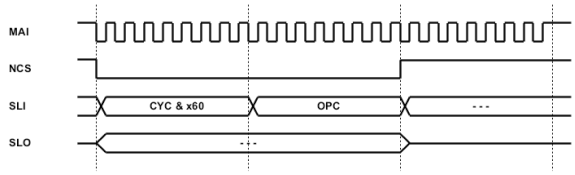

Figure 35: Accessing a command.

OPC				
Code				Function
–	RD	WR	CMD	
00	0	0	0000	Request of new position data
00	0	0	0001	Write configuration to EEPROM
00	0	0	0010	Read new data via ADI interface
00	0	0	0011	Trigger software reset
00	0	0	0100	Verify CRC of internal configuration
00	0	0	0101	Error simulation: activate ERR bit
00	0	0	0110	Error simulation: deactivate ERR bit
00	0	1	0000	Register write access
00	1	0	0000	Register read access

Table 84: Transmission opcodes (SPI commands)

Cyclic read

For CYC = 1, cyclic read is initiated for reading position data in a sequence covering the address range from 0x60 up to 0x6D (from STATUS to CRC). The setting of FULL_CYC is not relevant for SPI.

In order to generate new position data in advance

- pin NL (assigned to the parallel I/O interface) can be used, or
- the command register must be addressed by opcode 0x00 (prior to the cyclic read: request for new position data).

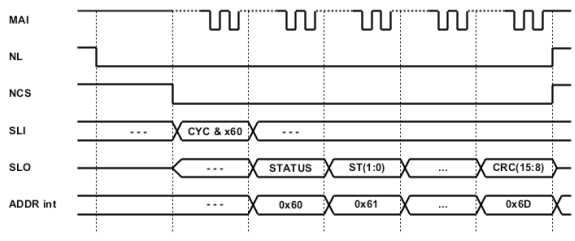

Figure 36: Cyclic read.

A CRC is formed across the output data (with the polynomial $x^{16} + x^{14} + x^{11} + x^{10} + x^9 + x^7 + x^5 + x^3 + x^1 + 1$ (0x14EAB), start value 0xFFFF). The checksum is re-

formed for each cyclic transmission and is only valid for the duration of this transmission.

SPI Output Format			
Byte No.	Data	Register	Address
1	Status byte	STAT(7:0)	0x60
2	Singleturn Ext byte	ST(1:0)	0x61
3	Singleturn Lo byte	ST(9:2)	0x62
4	Singleturn Mid byte	ST(17:10)	0x63
5	Singleturn Hi byte	ST(25:18)	0x64
6	Multiturn Lo byte	MT(7:0)	0x65
7	Multiturn Mid byte	MT(15:8)	0x66
8	Multiturn Hi byte	MT(23:16)	0x67
9	Sign-of-life counter	LC(7:0)	0x68
10	Error byte	ERR(7:0)	0x69
11	Temperature Lo byte	TEMP(7:0)	0x6A
12	Temperature Hi byte	TEMP(15:8)	0x6B
13	CRC Lo byte	CRC(7:0)	0x6C
14	CRC Hi byte	CRC(15:8)	0x6D

Table 85: SPI output format

Note: During serial I/O interface modes the pins D7...0 output the status register. A negative edge at D0 (status PDV) indicates the point of sampling, and data is ready to be read with high level.

EEPROM INTERFACE

Basic interface features

I2C Master Performance	
Protocol	Standard I²C
Clock Rate (Output)	140 kHz max. (refer to Elec.Char. N10)
Addressing	11 bit: 8 bit register address plus 3 bit block selection
Access Trials	Read: up to 3x at power-on (I²C error: acknowledge missing), 1x at byte reading, 1x at byte writing (for consecutive writing with pauses from byte to byte)
Multi-Master Capability	No

Table 86: I²C interface performance

The I²C master of iC-MR3 addresses I²C devices using an 8-bit register address plus 3 block selection bits as part of the I²C slave address.

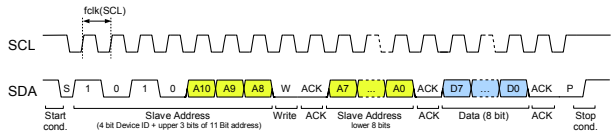

Figure 37: I²C slave addressing for writing a single byte to the EEPROM.

If addressing a memory of 1 Kbit or 2 Kbit, the block selections bits are zero and thus the I²C device address is 0x50 (for '1010 000' without the R/W bit), or 0xA0 respectively (for '1010 0000' with the R/W bit as zero).

ATTENTION: The iC-MR3 is not multi-master capable. However, if another I²C master is connected to the same bus, the iC-MR3 can be halted in reset until the bus comes available (use pin NRES for control).

EEPROM device requirements

EEPROM Device Requirements	
Supply Voltage	1.8 V to 5.5 V (respectively according to VDDP)
Power-On Threshold	< 3.3 V (due to Elec.Char. K01)
Addressing	11 bit address max.
Device Address	0x50 ('1010 000' w/o R/W bit), 0xA0 ('1010 0000' with R/W = 0)
Page Buffer	Not required
Size Min.	1 Kbit (128x8 bit), type 24C01, for configuration data
Size Max.	16 Kbit (8x 256x8 bit), type 24C16 Size limited due to 11-bit slave addressing.

Table 87: EEPROM Device Requirements

It is not relevant if the EEPROM's internal page buffer is 8 or 16 bytes. EEPROMs beyond 16 Kbit can not be used as those require a 2 byte address.

ATTENTION: EEPROMs that ignore the block select or upper address bits in the control byte (such as the Microchip 24AA0x/24LC0xB) should not be used with the iC-MR3.
With these devices, writing to an address beyond the capacity of the EEPROM will overwrite stored iC-MR3 configuration data.
EEPROMs that use the address pins as additional enable bits (such as the STMicroelectronics M24Cxx) should be used instead.
To avoid this problem altogether, use of a 16 Kbit EEPROM (which requires all 11 address bits) is recommended and also provides additional space for storage of OEM data.

ATTENTION: If further I²C slave devices are operated on the same bus, higher device addresses may be occupied.

I²C slave addressing

The BSEL register is used to switch to other memory banks on the external EEPROM. After an iC-MR3 power-on, bank 0 is selected, which mirrors the internal registers of iC-MR3. If BSEL points at a higher memory bank, the addresses 0x00-0x3F are mapped and aim at higher EEPROM registers.

BSEL	Addr. 0x40; bit 4...0	R/W
Code	binary	Memory bank addressed by BiSS Addr(5:0): 0x00...0x3F
0x0	0b 0 0000	Bank 0 (internal RAM)
0x1	0b 0 0001	Bank 1
0x2	0b 0 0010	Bank 2
...	...	... (0x4 to access iC-PVL)
0x1F	0b 1 1111	Bank 31

Table 88: Bank selection

I2CDEV	Addr. 0x40; bit 7...5	R/W
Code	I²C Slave Address [1]	Device ID
0b 000	Bank 0 to 31: 0b 1010 xxxxx xxxxxx	0x50 for EEPROM [2]
0b 001	Bank 32 to 255: 0b 1011 xxxxx xxxxxx	
0b 010	0b 1000 xxxxx xxxxxx	
0b 011	0b 1001 xxxxx xxxxxx	
0b 100	0b 1110 xxxxx xxxxxx	
0b 101	0b 1111 xxxxx xxxxxx	
0b 110	0b 1100 xxxxx xxxxxx	0xC to access iC-PVL [3]
0b 111	0b 1101 xxxxx xxxxxx	
Notes	[1] Device ID (4 bit) plus register address (11 bit): xxx xx is represented by BSEL(4:0) and xxxxxx by BiSS Addr(5:0). [2] Chip revision iC-MR3_0 requires I2CDEV = 0b 010 to access the external EEPROM at 0x50. [3] A write access may require SEC_LO = 0 if EDS banks are in use and protected (CFG_E2P > 0x00).	

Table 89: I²C device ID

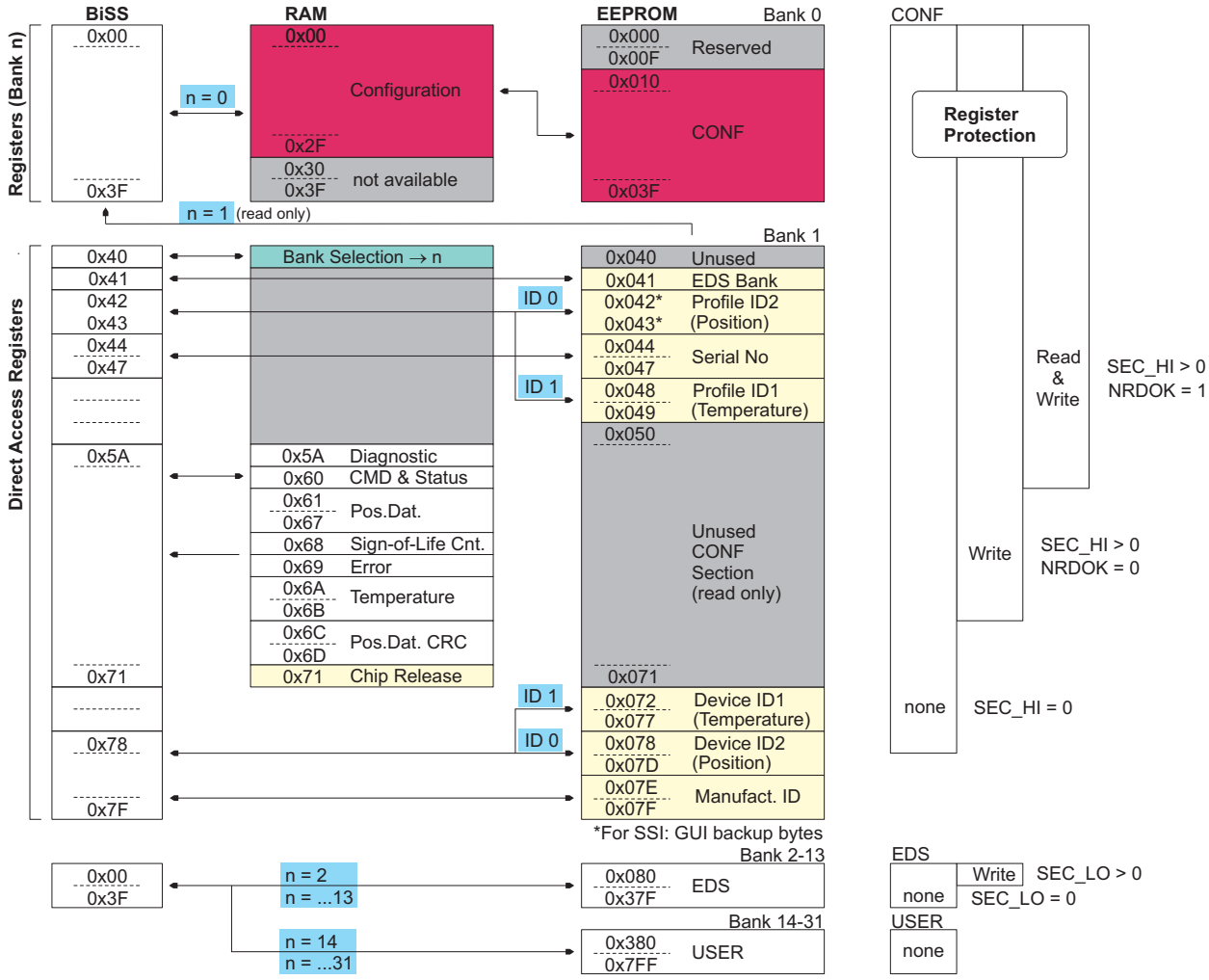

Figure 38: Bankwise memory addressing via BiSS. Example uses CFG_E2P = 0x2 for a 16 Kbit EEPROM.

Memory sections

The iC-MR3 divides external memory into three consecutive address spaces:

- CONF: iC-MR3 configuration data
- EDS: **E**lectronic **D**ata **S**heet
- USER: User section

The CONF section includes addresses 0x000 - 0x07F, i.e. memory banks 0 and 1.
The following EDS section is variable in length and needs to be configured by CFG_E2P.
Finally, the USER section coming after the EDS section takes all remaining EEPROM registers. Refer to Figure 38 for an allocation example.

CFG_E2P	Addr. 0x26; bit bit 7...6		R/W
Code	Available EDS banks	Available USER bks.	EEPROM Size (type)
00	0	0	1 Kbit, 128x8 (C01)
	1	1	2 Kbit, 256x8 (C02)
01	4	2	4 Kbit, 512x8 (C04)
	4	10	8 Kbit, 1024x8 (C08)
	4	26	16 Kbit, 2048x8 (C016)
10	12	2	8 Kbit, 1024x8 (C08)
	12	18	16 Kbit, 2048x8 (C016)
11	24	6	16 Kbit, 2048x8 (C016)
Note	As section CONF occupies 2 banks in any case, the pointer to the 1st EDS bank needs to be 0x02 or higher (configure EDSBANK $\geq$ 0x02).		

Table 90: EDS range selection

Register protection
Memory areas CONF and EDS are protected by separate write protection mechanisms. Note that USER memory, the banks following the EDS section, does not feature any read or write protection.

If the safety register SEC_HI does not equal 0x00, the status register shows zero for EWKH and NRDOK defines if write or read/write protection is active for the memory area CONF. In the latter case the configuration registers can then be neither read nor overwritten. A read command will result in 0x00.

The write protection for CONF blocks can be deleted by resetting the safety register SEC_HI to 0x00. To do so, the current data stored at address 0x25, the protection key SEC_HI and NRDOK, must be known and written again.

SEC_HI	Addr. 0x25; bit 6...0	R/W
Code	Function	
0x00	Register protection disabled	
Otherwise	Register protection according to NRDOK	

Table 91: Safety register for CONF memory

NRDOK	Addr. 0x25; bit 7	R/W
Code	Function	
0	Write protection for CONF memory	
1	Read and write protection for CONF memory	

Table 92: Read/write protection for CONF memory

If the safety register SEC_LO does not equal 0x00, the status register shows zero for EWKL and write protection is active for memory area EDS. All registers in this area can be read but not overwritten.

The write protection for EDS blocks can be deleted by resetting the safety register SEC_LO to 0x00. To do so, the current data stored at address 0x26, the protection key SEC_LO and CFG_E2P, must be known and written again.

SEC_LO	Addr. 0x26; bit 5...0	R/W
Code	Function	
0x00	Register protection disabled	
Otherwise	Write protection for EDS memory	

Table 93: Safety register for EDS memory

Accessing external memory banks

Register banks 2 to 31 store data in an external EEPROM. If an address is accessed which is not physically present on the iC-MR3 (see Figure 38), communication with the external EEPROM is initiated. If the parallel I/O interface or serial I/O interface is active in SPI mode, the end of I²C communication can be recognized by reading the status register (address 0x60, bit 2 BUSY). Only after this it is possible to again access the internal registers or external EEPROM registers. When the serial I/O interface is using the BiSS protocol, the iC-MR3 automatically requests the processing time necessary to access the EEPROM.

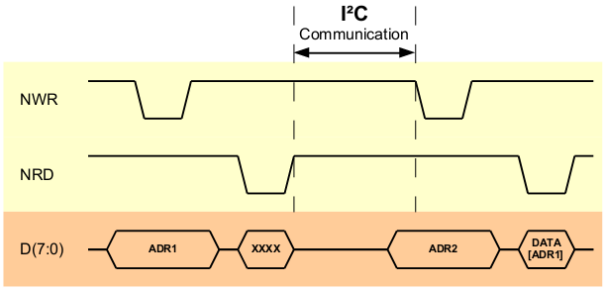

Figure 39: EEPROM read process

Two reads are needed to read data from an address on the EEPROM (for the parallel I/O interface and serial I/O interface in SPI mode only). The first read initiates communication with the EEPROM; at the end of the communication, the read data is stored in a temporary register on the iC-MR3. This temporary register data is supplied on the next read to an external address. At the same time, communication with the EEPROM is again started. This enables a large memory area to be read quickly, as the next read address can already be created when reading out the temporary register.

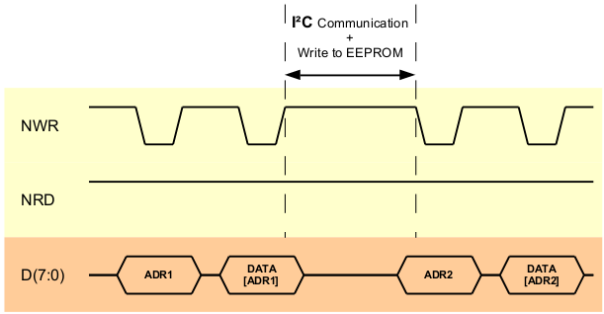

Figure 40: EEPROM write process

Reads and writes from/to data in the external EEPROM may only be made if an EEPROM is connected when the iC-MR3 is started. Autoincrement reads/writes to external addresses are not possible. The error bit ERR_KNF is updated following each external read/write (e.g. it is set if the storage time on the EEPROM is undershot, or cancelled if read/write is successful).

Note: Example of writing a range of values to the external EEPROM:

1. Write address 0x00
2. Read status register until BUSY = 0.
3. Read error register to check if ERR_KNF = 0.
4. Write address 0x01
5. Read status register until BUSY = 0.
6. Read error register to check ERR_KNF:
   If 1, repeat writing address 0x01
   If 0, continue with next address
7. Write address 0x02 ... etc.

Configuration data checksum

If an EEPROM is available, the configuration data and its checksum is read following power-on (for details refer to chapter EEPROM Interface, page 54). The checksum fills register CRCCFG at addresses 0x2E-0x2F and is then used to confirm the contents of the configuration RAM.

If no EEPROM is connected or if the checksum does not match, the configuration RAM is zeroed and must be rewritten including its checksum, followed by a CRC verification initiated on command.

If configuration data is written to the EEPROM on command, the checksum in addresses 0x2E-0x2F is newly calculated and transferred to the EEPROM.

CRCCFG(15:8) Addr. 0x2E; bit 7...0 R/W **CRCCFG(7:0)** Addr. 0x2F; bit 7...0	
Code	Function
0x0000	Checksum for address range 0x00 to 0x2D; CRC polynomial 0x1021 $x^{16} + x^{12} + x^5 + 1$ (CRC-16)
...	start value 0x0000
0xFFFF	

Table 94: Configuration data CRC

Example of CRC calculation routine:

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x1021;
unsigned short ucCRC=0;
int i = 0;

ucCRC = 0; // start value
for (iReg = 0; iReg<46; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x8000) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

ACCESSING EXTERNAL MEMORY

	Bank Access Control						
Register Address	Bank No.	Addr 0x40	I2CDEV	BSEL	BiSS Address	Contents	Remarks
RAM							
0x00 ...0x2F	0	0x00	1010	00000	0x00 ...0x2F	Configuration data	
0x40 ...0x7F	Direct access registers				0x40 ...0x7F	BiSS device data	
I²C Device: 2 Kbit EEPROM			**0x50**				CFG_E2P = 0x0
0x000 ...0x00F	0	0x00	1010	00000		Reserved[1]	Access not possible by iC-MR3.
0x010 ...0x03F	0	0x00	1010	00000	0x10 ...0x3F	CONF[2]	Configuration data
0x040 ...0x07F	1	0x01	1010	00001	0x00 ...0x3F	CONF	BiSS device data
0x080 ...0x0BF	2	0x02	1010	00010	0x00 ...0x3F	EDS (1)	
0x0C0 ...0x0FF	3	0x03	1010	00011	0x00 ...0x3F	USER (1)	max. for 2 Kbit
I²C Device: 4 Kbit EEPROM							CFG_E2P = 0x1
0x000 ...0x00F	0	0x00	1010	00000		Reserved[1]	Access not possible by iC-MR3.
0x010 ...0x03F	0	0x00	1010	00000	0x10 ...0x3F	CONF[2]	Configuration data
0x040 ...0x07F	1	0x01	1010	00001	0x00 ...0x3F	CONF	BiSS device data
0x080 ...0x0BF	2	0x02	1010	00010	0x00 ...0x3F	EDS (1)	
...0x17F	...5	...0x05	1010	00101		EDS (4)	
0x180 ...0x1BF	6	0x06	1010	00110	0x00 ...0x3F	USER (1)	
...0x1FF	...7	...0x07	1010	...00111		USER (2)	max. for 4 Kbit
I²C Device: 8 Kbit EEPROM							CFG_E2P = 0x2
0x000 ...0x00F	0	0x00	1010	00000		Reserved[1]	Access not possible by iC-MR3.
0x010 ...0x03F	0	0x00	1010	00000	0x10 ...0x3F	CONF[2]	Configuration data
0x040 ...0x07F	1	0x01	1010	00001	0x00 ...0x3F	CONF	BiSS device data
0x080 ...0x0BF	2	0x02	1010	00010	0x00 ...0x3F	EDS (1)	
...0x37F	...13	...0x0D	1010	01101		EDS (12)	
0x380 ...0x3BF	14	0x0E	1010	01110	0x00 ...0x3F	USER (1)	
...0x3FF	...15	...0x0F	1010	...01111		USER (2)	max. for 8 Kbit
I²C Device: 16 Kbit EEPROM							CFG_E2P = 0x3
0x000 ...0x00F	0	0x00	1010	00000		Reserved[1]	Access not possible by iC-MR3.
0x010 ...0x03F	0	0x00	1010	00000	0x10 ...0x3F	CONF[2]	Configuration data
0x040 ...0x07F	1	0x01	1010	00001	0x00 ...0x3F	CONF	BiSS device data
0x080 ...0x0BF	2	0x02	1010	00010	0x00 ...0x3F	EDS (1)	
...0x67F	...25	...0x19	1010	...11001		EDS (24)	
0x680 ...0x6BF	26	0x1A	1010	11010	0x00 ...0x3F	USER (1)	
...0x7FF	...31	...0x1F	1010	...11111		USER (6)	max. for 16 Kbit
I²C Device: various [3]							
0x000 ...0x03F	32	0x20	1011	00000	0x00 ...0x3F		
...0x7FF	...63	...0x3F	1011	...11111			
0x000 ...0x03F	64	0x40	1000	00000	0x00 ...0x3F		
...0x7FF	...95	...0x5F	1000	...11111			
0x000 ...0x03F	96	0x60	1001	00000	0x00 ...0x3F		
...0x7FF	...127	...0x7F	1001	...11111			
0x000 ...0x03F	128	0x80	1110	00000	0x00 ...0x3F		
...0x7FF	...159	...0x9F	1110	...11111			
0x000 ...0x03F	160	0xA0	1111	00000	0x00 ...0x3F		
...0x7FF	...191	...0xBF	1111	...11111			
0x000 ...0x03F	192	0xC0	1100	00000	0x00 ...0x3F		(iC-PVL at BSEL 0xC4)
...0x7FF	...223	...0xDF	1100	...11111			
0x000 ...0x03F	224	0xE0	1101	00000	0x00 ...0x3F		
...0x7FF	...255	...0xFF	1101	...11111			
Notes	[1] Reserved section of 16 bytes, e.g. for optional multiturn configuration data.						
	[2] There is an address offset of 16 bytes between RAM and EEPROM.						
	[3] Access may require to unlock EDS write protection.						

Table 95: External memory access using bank switching

COMMAND AND STATUS REGISTER

Command register
By writing to register 0x60, the following commands are executed.

CMD	Addr. 0x60; bit 7...0	W
Code	Function	
0x00	Request of new position data	
0x01	Write current configuration to EEPROM	
0x02	Read new data via absolute data interface	
0x03	Trigger software reset	
0x04	Verify CRC of internal configuration	
0x05	Error simulation: activate ERR status	
0x06	Error simulation: delete ERR status	

Table 96: Command register

If the command 0x00 is written, new position data is requested. As long as the new data is not yet available, the PDV (position data valid) bit in the status register shows a zero.

The command 0x01 writes the current configuration to the EEPROM: configuration registers 0x00 up to 0x2D plus **a newly generated checksum** are written. For the duration of this write process the status register indicates BUSY and the error register indicates configuration error ERR_KNF.
If an error occurs during writing, error ERR_KNF is not deleted at the end of the process.
If no EEPROM is connected on startup, the command 0x01 has no effect.

Note: When executing command 0x01 using the BiSS interface, neither the status nor the error register are available for evaluation. Monitoring the data bus pins D2 (for BUSY) and D6 (for ERR) could be considered. Alternatively, the BiSS error bit could be monitored when reading position data (for this ERR_KNF needs to be mapped onto the ERR bit of the status register using EM_KNF at address 0x22).

The command 0x02 triggers a single read of absolute data using the absolute data interface. If the read is successful, the cycle counter is set (or zeroed if not). In either case, status bit ADV and error bit ERR_ABS will be updated.
If command 0x02 is executed for the first time after startup, the reading is repeated as long as an error occurs. During this time the cycle counter is kept at zero.

Note: When using the command 0x02, the CYC_ADI function should be disabled in advance to free the ADI interface:

1. Write CYC_ADI = 0 (address 0x18, bit 2).
2. Execute CMD 0x02 for a single read at the ADI.
3. Wait until the command execution is finished. Depending on the settings of SLOW_ADI and SSI_ADI, command execution takes 0.2 ms, 0.75 ms, 1.5 ms, or 6 ms (worst case values).
4. Check STATUS at 0x60 for ADV bit is 1.
5. Write CYC_ADI = 1 to reactivate cyclic operation and checking.

The command 0x03 initiates a software reset which is also indicated by a low signal at pin NRES.

The command 0x04 triggers a CRC of the internal configuration, during which all configuration registers are reviewed and verified by the checksum in registers 0x2E-0x2F. During this process the status register indicates BUSY and the error register indicates configuration error ERR_KNF. The error ERR_KNF is only cancelled if the process ends successfully.

The commands 0x05 and 0x06 simulate errors for the ERR bit in the status register, with 0x05 setting the bit and 0x06 deleting it.

Software reset
As with a power cycle (undervoltage reset), upon a software reset command, the I/O pin NRES indicates a short low pulse (for 3 clock cycles, approx. 200 ns). With the rising edge of NRES, the iC-MR3 starts to access the external I^2C-EEPROM to read its CRC protected configuration data (see section Startup with EEPROM, page 44).

If there is no EEPROM, the internal registers are zeroed and the pin state of SDA and SCL is evaluated to select the interface (see section Startup without EEPROM, page 44).

Status register

A read to register 0x60 returns the current system status.

STATUS	Addr. 0x60; bit 7...0	R
Bit	Status message	
INIT	Configuration completed	
ERR	Error message (as selected by EMASK) If active, error pin NERR pulls low.	
WARN	Warning message (as selected by WMASK)	
EWKH	Write access permitted to memory area CONF	
EWKL	Write access permitted to memory area EDS	
BUSY	Internal data bus busy	
ADV	Absolute data valid	
PDV	Position data valid	
Logic	1 = true, 0 = false	

Table 97: Status register

INIT indicates that the configuration registers have been successfully CRC verified, and that the absolute data has been correctly read by the absolute data interface.

ERR and WARN indicate error messages which are selected by the mask registers EMASK and WMASK.

EWKH and EWKL signal an active write protection for memory areas CONF, or EDS, respectively.

BUSY indicates that the internal data bus is busy, such as when data is being read from or written to the EEPROM.

ADV indicates that absolute data has been loaded successfully through the absolute data interface. If SSI is configured, data is always accepted. If BiSS is configured, data is accepted only if the CRC is correct and the error bit inactive.

PDV signals that the current position data is valid.

Error masking for ERR and WARN status

The registers EMASK and WMASK define which messages of the error register are to be reported to the error bit or warning bit of the status register.

EMASK	Addr. 0x22; bit 7...0	R/W
Bit 7:0	Message	
EM_EXT	System Error	
EM_ABS	Absolute Data Error	
EM_IPO	Interpolation Error	
EM_KNF	Configuration Error	
EM_SYN	Synchronization Error	
EM_TMP	Temperature Error	
EM_AMP	Signal Error	
EM_RGL	Control Error	
Logic	1 = enabled, 0 = disabled	

Table 98: Error masking for status bit ERR

WMASK	Addr. 0x23; bit 7...0	R/W
Bit 7:0	Message	
WM_EXT	System Error	
WM_ABS	Absolute Data Error	
WM_IPO	Interpolation Error	
WM_KNF	Configuration Error	
WM_SYN	Synchronization Error	
WM_TMP	Temperature Error	
WM_AMP	Signal Error	
WM_RGL	Control Error	
Logic	1 = enabled, 0 = disabled	

Table 99: Error masking for status bit WARN

MONITORING AND SAFETY FEATURES

Error register

The error register at address 0x69 signals internal and external errors, whereas most error bits are stored until being reset.

ERROR	Addr. 0x69; bit 7...0	R
Bit	Error message	
ERR_EXT	**System Error** (latched*) Pin NERR was forced low by the external system or due to the STATUS bit ERR, on messages selected by EMASK.	
ERR_ABS	**Absolute Data Error** - ADI data match error (if CHK_ADI = 1) - ADI detected BiSS CRC error (if SSI_ADI = 0) - ADI received BiSS error: nE = 0 (if SSI_ADI = 0) ERR_ABS remains zero if the ADI is not in use.	
ERR_IPO	**Interpolation Error** Conversion was not finished at time of read access.	
ERR_KNF	**Configuration Error** This error will be indicated in case of: - startup without EEPROM - CRC error on power-on with EEPROM - CRC error after CRC verification on command - temporarily during I^2C write to EEPROM - the EEPROM is not responding	
ERR_SYN	**Synchronization Error** (latched **) Internal synchronization failure between cycle counter and interpolator.	
ERR_TMP	**Temperature Error** (latched*) The upper or lower temperature monitoring threshold was exceeded.	
ERR_AMP	**Signal Error** (latched*) Or-gated summary of DC_MAX, DC_MIN, CMP_MAX, CMP_MIN	
ERR_RGL	**Control Error** (latched*) Or-gated summary of RG_MAX, RG_MIN, AMP_MAX, AMP_MIN Note: The control error is not messaged when using the constant current source (ACOT = 11).	
Logic	0 = no error, 1 = error is active or latched *) Register reset is required to delete the message. **) A software reset command or power cycle is required to delete this message.	

Table 100: Error register

RES_ERR selects which action resets the error register. Either the error register is reset after each position reading cycle, or the error register is maintained until register 0x69 is read.

RES_ERR	Addr. 0x27; bit 6	R/W
Code	Function	
0	Reset upon reading position data	
1	Reset after a read from the error register	

Table 101: Error register reset action

Diagnosis register

The diagnosis register at address 0x5A further resolves the messages summarized by signal error ERR_AMP and control error ERR_RGL.

DIAG	Addr. 0x5A; bit 7...0	R
Bit	Name	Description
Signal Errors under ERR_AMP		
5	DC_MAX	DC level monitoring: maximum offset (refer to Elec.Char. No. B06)
1	DC_MIN	DC level monitoring: minimum offset (refer to Elec.Char. No. B07)
4	CMP_MAX	AC level monitoring: maximum amplitude (refer to Elec.Char. No. B03)
0	CMP_MIN	AC level monitoring: minimum amplitude (refer to Elec.Char. No. B04)
Control Errors under ERR_RGL		
7	RG_MAX	ACO control error: maximum current (refer to Elec.Char. No. 808)
3	RG_MIN	ACO control error: minimum current (refer to Elec.Char. No. 807)
6	AMP_MAX	Signal level monitoring: maximum amplitude (refer to Elec.Char. No. 810)
2	AMP_MIN	Signal level monitoring: minimum amplitude (refer to Elec.Char. No. 809)
Note: For a description of signal and control error monitoring refer to page 31.		

Table 102: Diagnosis register

Signal error filtering

Error messaging to ERR_AMP can be assigned with a digital filter enabled by EN_FAMP. The filter is implemented as an integrator with an adjustable timeout (TO_FAMP) to reset and restart the integration time. The filter threshold THR_FAMP determines how long a signal error must be active until it is passed on to the error register.

EN_FAMP	Addr. 0x2B; bit 0	R/W
Code	Function	
0	No filtering	
1	Filtering active on ERR_AMP	

Table 103: Signal error filtering

TO_FAMP	Addr. 0x2B; bit 1	R/W
Code	Function	
0	Reset every 273 µs typ.	
1	Reset every 546 µs typ.	

Table 104: Filter timeout

THR_FAMP	Addr. 0x2B; bit 3...2	R/W
Code	Function	
0x0	approx. 17 µs	
0x1	approx. 34 µs	
0x2	approx. 51 µs	
0x3	approx. 68 µs	

Table 105: Filter threshold

Sign-of-life counter
The 8-bit sign-of-life counter register is incremented by 1 when new position data was generated successfully following a request. Note that using **continuous conversion** in combination may not be useful because data generation is triggered repeatedly, which increases the sign-of-life counter.

The sign-of-life counter has a value range of 1 to 63 using BiSS, and 1 to 255 when using SPI or the parallel interface. Its reset value of zero is never output as it is bypassed during normal operation (counting order 0xFE, 0xFF, 0x01, 0x02 ...).

LC(7:0)	Addr. 0x68; bit 7...0	R
Code	Value	
0x00	Internal reset value	
0x01	Start value on first request for new position data and follow-up value after the maximum value	
0x02	Start value after power up or reset with initialization from ADI	
...	...	
0x3F	Max. value for BiSS/SSI protocol (limited to 6 bit)	
...	...	
0xFF	Max. value for SPI and parallel interface	

Table 106: Sign-of-life counter

In the BiSS and Extended SSI data frames the sign-of-life counter is transmitted after the nE and nW bits and secured by the subsequent CRC.

DESIGN REVIEW: Notes On Chip Functions

iC-MR3 Z		
No.	Function, parameter/code	Description and application notes
1	Serial I/O Interface: SPI Polling the status register (accessing external memory via I^2C)	If using the serial I/O interface in SPI mode, it is suggested to detect the end of I^2C communication by reading the BUSY bit of the status register at address 0x60 (according to page 57). This procedure does not work using SPI, it is applicable using the parallel I/O interface only. During SPI, the BUSY status is output to pin D2 and thus can be monitored. Alternatively, waiting 500 µs between SPI access cycles could be considered (a single I^2C access takes about 350 µs).
2	Absolute Data Interface (ADI): initialization of the cycle counter	When using STP_ADI = 1 and/or CYC_ADI = 1 or triggering ADI read by command: If the ADI loads external data at the same time as when the sine signal crosses zero, the cycle counter can be wrongly initialized by +/- 1 cycle. Note: When using the ADI to preload the cycle counter, the data comparison depth in a safety application needs to be limited to 33 bit, respectively to 9 bit regarding the ST position (with RESO_CC = 10 for a system of 2048 cpr sin/cos).
3	Power-up sequence for VDD and VDDP	If the supply VDD is applied ahead of VDDP, restoring the chip's setup from the EEPROM may require a reset either by a software command or using pin NRES.
4	Register UIN (Addr 0x0E, bit 0): Current/voltage signal mode	During reset the default state is 0 (current input).
5	Absolute Data Interface (ADI): function of STP_ADI for startup with abs. data	In case of a failure (e.g. no reply or CRC error), the read access will be repeated only once.

Table 107: Notes on chip functions regarding iC-MR3 chip revision Z.

iC-MR3 Z1		
No.	Function, parameter/code	Description and application notes
4	Register UIN (Addr 0x0E, bit 0): Current/voltage signal mode	During reset the default state is 0 (current input).
5	Absolute Data Interface (ADI): function of STP_ADI for startup with abs. data	In case of a failure (e.g. no reply or CRC error), the read access will be repeated only once.

Table 108: Notes on chip functions regarding iC-MR3 chip revision Z1.

iC-MR3 Z2		
No.	Function, parameter/code	Description and application notes
1	Absolute Data Interface (ADI): function of STP_ADI for startup with abs. data	The ADI activity starts regardless of the input level to ASLI. In case of an error (e.g. no response or CRC error), the read access is repeated after a clock pause of approx. 17 µs. If the connected slave has a longer timeout, it may not present updated data. In this case configure SLOW_ADI = 1 to fourfold the clock pause.

Table 109: Notes on chip functions regarding iC-MR3 chip revision Z2.

REVISION HISTORY

Rel.	Rel. Date[9]	Chapter	Modification	Page
A1	2017-11-23		Initial release	

Rel.	Rel. Date[9]	Chapter	Modification	Page
A2	2017-12-21	ELECTRICAL CHARACTERISTICS	Item N11: typ. and max. values Items O06, P06, P07, Q06: max. value to -10 µA Item O07: max. value 100 µA	8ff
		REGISTER MAP	EEPROM registers 0x50 to 0x71 are read only. Footnote added to register 0x42.	20ff
		EEPROM INTERFACE	Table 86: description of access trials corrected Figure 38: updated for bank 1 (read only) Register protection: description of safety register reset corrected	54, 55, 56
		DESIGN REVIEW: Notes On Chip Functions	Items 1 and 2 supplemented	63

Rel.	Rel. Date[9]	Chapter	Modification	Page
B1	2018-04-26	ELECTRICAL CHARACTERISTICS	Item 703, 706: min/max limits, item 707 added Item 802 for Isc()hi: condition corrected Item K07 for Vt()hi$_{CMOS}$: condition and limit added Items O12, Q09 for Isc()hi: min limit 85 mA	8ff
		CONFIGURATION PARAMETERS	Parameters renamed: GR: Coarse Gain → Coarse Gain Factor GFS, GFC: Fine Gain → Fine Gain Factor MPS, MPC: Center Potential → VDC Center Potential ORS, ORC: Offset Calibr. Range → Coarse Offset Factor OFS, OFC: Offset Calib. → Fine Offset Factors ACOT, Controller operating mode → ACO Output control mode	18
		REGISTER MAP: RAM	Description of NRES pin function added, footnote to UIN added	20ff
		OPERATING MODES	Table 3 (MODE): note added	24
		SIGNAL CONDITIONING	Fig. 10 updated to include R1, R2 Description of Current Mode updated Table 6 (UIN): note added on default state Tables 7 (RIN) and8 (TUIN): updated to mention R2 Tables 10 (SELREF), 13 (REFVOS): contents updated Tables 15 (ORS, ORC), 16 (OFS, OFC): layout and footnotes updated	25ff
		AMPLITUDE CONTROL	Table 19: min. range and note added Table 24: note added	29, 30
		ABSOL. DATA INTERFACE (ADI)	Table 54 (STP_ADI): contents updated	41
		SERIAL I/O INTERFACE: BiSS C	Description to NTOA added	48
		SERIAL I/O INTERFACE: SSI	Table 79 (SSI): up to 97 bit; note box added on binary output format	50
		EEPROM INTERFACE	Fig. 38: updated for footnote to 0x43 Note box added for programming example	55, 57
		ACCESSING EXTERNAL MEM.	Table 95: footnote added	58
		COMMAND AND STATUS REG.	Commands 0x01, 0x02: note box added	59
		DESIGN REVIEW: Notes On Chip Functions	Section updated, chip revision MR3_Z2 added	63

Rel.	Rel. Date[9]	Chapter	Modification	Page
C1	2018-10-16	ELECTRICAL CHARACTERISTICS	Items 605, 606, 607 added	8ff
		ABSOL. DATA INTERFACE (ADI)	Note box added on STD_ADI, and CHK_ADI	41, 42
		SIGNAL FILTERING AND SIN/COS OUTPUT DRIVERS	Note boxes #1 and #2 updated Note box #3 added on sin/cos output states.	32
		ACCESSING EXTERNAL MEM.	Correction: access to iC-PVL at 0xC4	58

Rel.	Rel. Date[9]	Chapter	Modification	Page
C2	2019-05-16	ABSOLUTE MAXIMUM RATINGS	Item G012 (Ts): name change, item G013 (Ts) moved to Thermal Data	7
		SIGNAL CONDITIONING	Tables 11, 12: subtitel supplemented for clarity	26

		ABSOLUTE DATA INTERFACE (ADI)	Note below Table 55 updated for clarity. Table 56: note added Note box added on Suggested Configurations Subsequent note boxes: updates of 1st and 2nd box	41, 42
		EEPROM INTERFACE	Table 89: access to iC-PVL at 0xC4 Table 90: headline and note updated Figures 39 and 40 updated Example of CRC calculation routine corrected to 16-bit polynomial	56, 57
		COMMAND AND STATUS REGISTER	Note box on command 0x02 updated	59
		MONITORING AND SAFETY FEATURES	Table 100: description addded to ERR_EXT, footnote added to ERR_SYN	61

Rel.	Rel. Date[9]	Chapter	Modification	Page
C3	2020-08-13	DESCRIPTION	Note box added	2
		ABSOLUTE MAXIMUM RATINGS	Item G010: added as new item	7
		ELECTRICAL CHARACTERISTICS	Item O08: minimum BiSS/SSI clock frequency added Item C01: typ. value moved to max.	8ff
		Serial I/O Interface: BiSS/SSI Protocol	Item I201 moved to I207, parameter renamed Item I208 moved to I218, parameter renamed Item I211, I212: parameters renamed	16
		REGISTER MAP, DESIGN REVIEW	Name change: chip release (CHIP_REL) to chip revision (CHIP_REV)	20ff
		ABSOL. DATA INTERFACE (ADI)	Table 54 (STP_ADI): Note 2 updated	41
		12-BIT ADC USING PT1000	Section added	35ff
		SERIAL I/O INTERFACE: SPI	Update of Figures 34, 35, 36 for pin-state of SLO	52
		COMMAND AND STATUS REGISTER	Command 0x02: description added	59

Rel.	Rel. Date[9]	Chapter	Modification	Page
C4	2021-03-15	TITLE, FEATURES, APPLICATIONS DESCRIPTION	Change of title, safety applications added Note box added on safety applications	1, 2
		OPERATING REQUIREM. ADI	Item I001 moved to I009, udpate of name Item I110 moved to I015	14
		OPERATING REQUIR. SSI, BiSS	Figures 5 and 8: latching point added	16
		INTERPOLATION AND CYCLE COUNTING	Note boxes added for pipeline conversion	39
		ABSOL. DATA INTERFACE (ADI)	Table 54: footnote 3 added	41
		SERIAL I/O INTERFACE: BiSS C	Table 63: footnote 5 added	47
		MONITORING AND SAFETY FEATURES	Table 100: description of ERR_ABS updated Description of sign-of-life counter updated	61, 62
		DESIGN REVIEW: Notes On Chip Functions	Item 1 added to MR3_Z2	63

Rel.	Rel. Date[9]	Chapter	Modification	Page
D1	2021-12-08	ELECTRICAL CHARACTERISTICS	Item A02: condition corrected Item 805: condition corrected Item O12, Q09: min. limit	8ff
		REGISTER MAP: RAM	Footnote 1 updated	20ff
		ABSOL. DATA INTERFACE (ADI)	Description of SPO_ADI supplemented	41

[9] Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-MR3	48-pin QFN, 7 mm x 7 mm, thickness 0.9 mm, RoHS compliant	iC-MR3 QFN48-7x7
Evaluation Board		iC-MR3 EVAL MR3D

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