# iC-MG

## 8-Bit Sin/Cos INTERPOLATION IC WITH RS422 DRIVER



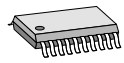
### FEATURES

- Real-time tracking, no-missing-code interpolation with selectable factors: x1, x2, x4, x5, x8, x10, x16, x20, x25, x50
- High input frequency of up to 500 kHz at x1 and x2 (200 kHz at x4 and x5, 100 kHz at x10, 20 kHz for x50)
- Excellent accuracy (typ. 0.6 LSB) and repeatability (typ. 0.1 LSB)
- Differential PGA inputs with selectable input resistance for voltage and current signals
- Adjustable signal conditioning for offset, amplitude, phase
- Unique signal and calibration stabilization feature: supply of encoder LED or MR bridge via controlled 40 mA current source
- Fail-safe RS422 encoder quadrature outputs with index signal
- Adjustable index position and length (from 1/4 to 1 T)
- Preselectable minimum phase distance for fail-safe counting
- Clipping, loss-of-signal and loss-of-tracking indication
- Setup via serial EEPROM interface
- Sub-system power switch offers reverse polarity protection for the overall system
- Single 5 V supply, operation from -25 °C to +100 °C

### APPLICATIONS

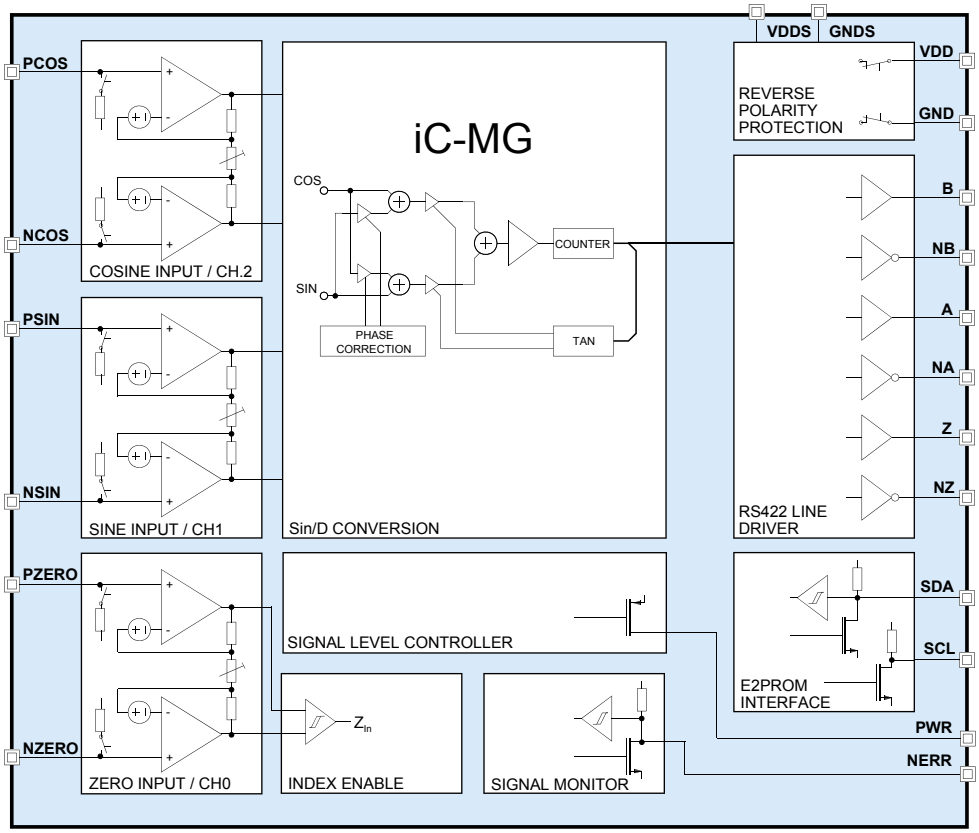
- Optical and magnetic position sensors
- Rotary encoders
- Linear encoders

### PACKAGES



TSSOP20

### BLOCK DIAGRAM



## DESCRIPTION

iC-MG is a non-linear A/D converter which, by applying a count-safe vector principle, digitizes sine/cosine sensor signals with selectable resolution and hysteresis. The angle position is output incrementally via differential RS422 drivers as an encoder quadrature signal with an index pulse. The minimum phase distance can be preselected, to enhance the systems's noise immunity and to allow for fail-safe counting.

The PGA front-end permits differential (VDIFF or IDIFF mode) or single-ended input signals (VREF or IREF mode); high impedance (V modes) and low impedance (I modes) can be selected. By this adaptation MR sensor bridges or photosensors can be directly connected.

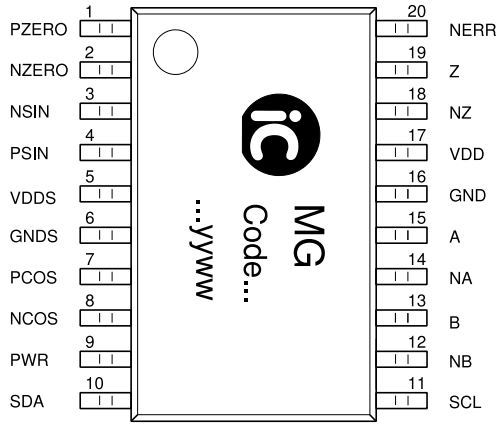
The integrated signal conditioning unit allows signal amplitudes and offset voltages to be calibrated and also any phase error between the sine and cosine signals to be corrected.

For the purpose of signal stabilization (to minimize the effects of temperature and aging), the chip's power supply controller can take over LED control in optical systems (40 mA current-source output PWR). If MR sensors are connected this driver stage also powers the measuring bridges. If the control thresholds are reached this is signaled at alarm message output NERR (signal loss due to wire breakage, short circuiting, dirt or aging, for example).

iC-MG is protected against a reversed power supply voltage; the integrated supply switch for loads of up to 20 mA extends this protection to cover the overall system. The device is configured via an external EEPROM.

## PACKAGING INFORMATION

### PIN CONFIGURATION TSSOP20




### PIN FUNCTIONS

| No. | Name | Function |
|---|---|---|
| 1 | PZERO | Input Zero Signal + |
| 2 | NZERO | Input Zero Signal - |
| 3 | NSIN | Input Sine Signal - |
| 4 | PSIN | Input Sine Signal + |
| 5 | VDDS[1] | Switched Supply Output and Internal Analog Supply Voltage (reverse pol. proof, load 20 mA max.) |
| 6 | GNDS[1] | Switched Ground (reverse pol. proof) |
| 7 | PCOS | Input Cosine Signal + |
| 8 | NCOS | Input Cosine Signal - |
| 9 | PWR | Controlled Power Supply Output (high-side current source) |
| 10 | SDA | Serial E2PROM Interface, data line |
| 11 | SCL | Serial E2PROM Interface, clock line |
| 12 | NB | Incremental Output B- |
| 13 | B | Incremental Output B+ |
| 14 | NA | Incremental Output A- |
| 15 | A | Incremental Output A+ |
| 16 | GND | Ground |
| 17 | VDD | +4.3 ... 5.5 V Supply Voltage |
| 18 | NZ | Incremental Index Output Z- |
| 19 | Z | Incremental Index Output Z+ |
| 20 | NERR | Alarm Message and Test Signal Output (e.g. index enable signal Zin) |

[1] It is advicable to connect a bypass capacitor of about 100 nF (up to 1 µF max.) close to the chip's analog supply terminals.

## ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

| Item No. | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| G001 | V() | Voltage at VDD, A, NA, B, NB, Z, NZ, SCL, SDA, PWR | | -6 | 6 | V |
| G002 | V() | Voltage at NERR | | -6 | 8 | V |
| G003 | V() | Voltage Pin vs. Pin | | | 6 | V |
| G004 | V() | Voltage at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, SCL, SDA | | -0.3 | VDDS +0.3 | V V |
| G005 | I(VDD) | Current in VDD | | -20 | 400 | mA |
| G006 | I() | Current in VDDS, GNDS | | -50 | 50 | mA |
| G007 | I() | Current in PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, SCL, SDA, NERR | | -20 | 20 | mA |
| G008 | I() | Current in A, NA, B, NB, Z, NZ | | -100 | 100 | mA |
| G009 | I(PWR) | Current in PWR | | -100 | 20 | mA |
| G010 | Vd() | ESD Susceptibility at all pins | HBM, 100 pF discharged through 1.5 kΩ | | 2 | kV |
| G011 | Tj | Junction Temperature | | -40 | 150 | °C |
| G012 | Ts | Storage Temperature | | -40 | 150 | °C |

## THERMAL DATA

Operating Conditions: VDD = 4.3...5.5 V

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| T01 | Ta | Operating Ambient Temperature Range | | -25 | | 100 | °C |

All voltages are referenced to pin GNDS unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

## ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3...5.5 V, $T_j$ = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise noted.

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **General** | | | | | | | |
| 001 | V(VDD) | Permissible Supply Voltage | Load current I(VDDS) to 10 mA<br>Load current I(VDDS) to 20 mA | 4.3<br>4.5 | | 5.5<br>5.5 | V<br>V |
| 002 | I(VDD) | Supply Current | $T_j$ = -40...125 °C, no load<br>$T_j$ = 27 °C, no load | | <br>12 | 25 | mA<br>mA |
| 003 | VDDon | Turn-on Threshold VDD | | 3.6 | 4.0 | 4.3 | V |
| 004 | VDDoff | Turn-off Threshold VDD | | 3.0 | 3.5 | 3.8 | V |
| 005 | VDDhys | Turn-on Threshold Hysteresis | | 0.4 | | | V |
| 006 | Vcz()hi | Clamp Voltage hi at all pins | | | | 11 | V |
| 007 | Vc()hi | Clamp Voltage hi at inputs SCL, SDA | Vc()hi = V() - V(VDD), I() = 1 mA | 0.4 | | 1.5 | V |
| 008 | Vc()hi | Clamp Voltage hi at inputs PSIN, NSIN, PCOS, NCOS, PZERO, NZERO | Vc()hi = V() - V(VDD), I() = 4 mA | 0.3 | | 1.2 | V |
| 009 | VC()lo | Clamp Voltage lo at all pins | I() = -4 mA | -1.2 | | -0.3 | V |
| 010 | Irev(VDD) | Reverse-Polarity Current VDD vs. GND | V(VDD) = −5.5V...−4.3 V | -1 | | 1 | mA |
| **Inputs and Signal Conditioning: PSIN, NSIN, PCOS, NCOS, PZERO, NZERO** | | | | | | | |
| 101 | Vin()sig | Permissible Input Voltage Range | RSC, RZ = 0x1<br><br>RSC, RZ = 0x9 | 0.75<br><br>0 | | VDDS - 1.5<br><br>VDDS | V<br><br>V |
| 102 | Iin()sig | Permissible Input Current Range | RSC(0), RZ(0) = 0, BIASSC = 0<br>RSC(0), RZ(0) = 0, BIASSC = 1 | -300<br>10 | | -10<br>300 | µA<br>µA |
| 103 | Iin() | Input Current | RSC, RZ = 0x1 | -10 | | 10 | µA |
| 104 | Rin() | Input Resistance vs. VREFin() | Nominal values following Table 8 | 70 | 100 | 130 | % |
| 105 | TCRin() | Input Resistance Temperature Coefficient | | | 0.15 | | %/K |
| 106 | VREFin() | Input Reference Voltage | No load, nominal values following Table 9 | 90 | 100 | 110 | % |
| 107 | G | Gain Factor (Coarse x Fine) | RSC(3), RZ(3) = 0, GRx = 0x0, GFx = 0x00<br>RSC(3), RZ(3) = 0, GRx = 0x7, GFx = max.<br><br>RSC(3), RZ(3) = 1, GRx = 0x0, GFx = 0x00<br>RSC(3), RZ(3) = 1, GRx = 0x7, GFx = max. | | 2<br>100<br><br>0.5<br>25 | | |
| 108 | G-LSB | Least Significant Gain Factor Cal. Step | Sine channel<br>Cosine channel<br>Zero channel | | 1.015<br>1.06<br>1.06 | | |
| 109 | G-INL | Integral Non-Linearity of Gain Factor Cal. | | -1 | | 1 | LSB |
| 110 | GR-CR | S/C-Chan. Gain Ratio Calibration Range | GFC = 0x10, GFS = 0x00...0xFF | 39 | | 255 | % |
| 111 | Vin()diff | Recommended Diff. Input Signal Level | Vin()diff = V(PCHx) - V(NCHx);<br>RSC, RZ ≠ 0x9<br>RSC, RZ = 0x9 | <br>10<br>40 | | <br>500<br>2000 | <br>mVpp<br>mVpp |
| 112 | Vin()os | Input Offset Voltage | Referenced to side of input pins | | 25 | | µV |
| 113 | OFS/C-CR | S/C Offset Calibration Range | Referenced to source VOSSC;<br>ORS, ORC = 00<br>ORS, ORC = 01<br>ORS, ORC = 10<br>ORS, ORC = 11 | | <br>±100<br>±200<br>±600<br>±1200 | | <br>%V()<br>%V()<br>%V()<br>%V() |
| 114 | OFS/C-LSB | Least Significant S/C-Offset Cal. Step | Referenced to source VOSSC; ORS, ORC= 00 | | 0.79 | | % |
| 115 | OFZ-LSB | Least Significant Z-Offset Cal. Step | Referenced to VOSZ; ORZ = 00 | | 3.2 | | % |
| 116 | OFx-INL | Integral Non-Linearity of Offset Cal. | | -5 | | 5 | LSB |
| 117 | PH-CR | S/C Phase Calibration Range | | | ±20 | | ° |

## ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3...5.5 V, $T_j$ = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise noted.

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| 118 | PH-LSB | Least Significant S/C Phase Cal. Step | | | 0.63 | | ° |
| 119 | PH-INL | Integral Non-Linearity of S/C Phase Cal. | | -0.8 | | 0.8 | ° |
| 120 | fin()max | Permissible Max. Inp. Frequency | <br>with interpolation of x1, x2 | 200<br>500 | | | kHz<br>kHz |
| **Sine-to-Digital Conversion** | | | | | | | |
| 201 | AAabs | Absolute Angle Accuracy (following calibration) | Referred to 360 deg input signal, ideal and quasi-stable input signals, SELHYS = 0 | | 1 | 2 | ° |
| 202 | AArel | Relative Angle Accuracy | Referred to A/B output period, ideal and quasi-stable input signals | -10 | | +10 | % |
| 203 | AAR | Absolute Angle Repeatability | See 201; VDD = const., Tj = const. | | 0.2 | | ° |
| **Output Line Drivers: A, NA, B, NB, Z, NZ** | | | | | | | |
| 501 | Vs()hi | Saturation Voltage hi | Vs()hi = VDD - V(); I() = -20 mA | | | 400 | mV |
| 502 | Vs()lo | Saturation Voltage lo | I() = 20 mA | | | 400 | mV |
| 503 | Isc()hi | Short-Circuit Current hi | | -60 | -40 | -20 | mA |
| 504 | Isc()lo | Short-Circuit Current lo | | 20 | 40 | 60 | mA |
| 505 | Ilk()tri | Tristate Leakage Current | TRIHL(1:0) = 11 | | 20 | 100 | µA |
| 506 | tr() | Rise Time hi | RL = 100 Ω to GNDS;<br>SSR(1:0) = 01<br>SSR(1:0) = 10 | <br>5<br>20 | | <br>40<br>140 | <br>ns<br>ns |
| 507 | tf() | Rise Time lo | RL = 100 Ω to VDD;<br>SSR(1:0) = 01<br>SSR(1:0) = 10 | <br>5<br>30 | | <br>40<br>140 | <br>ns<br>ns |
| 508 | Ri()cal | Source Impedance | With calibration modes | | 2.5 | 4 | kΩ |
| 509 | I()cal | Permissible Load Current | With calibration modes | -3 | | 3 | µA |
| 510 | Ilk() | Leakage Current with Reversed Supply Voltage | | | | 100 | µA |
| 511 | MTD() | Min. Phase Distance Tolerance | referred to nominal value | -25 | | +25 | % |
| **Controlled Power Supply: PWR** | | | | | | | |
| 601 | Vs()hi | Saturation Voltage hi | Vs()hi = VDD - V();<br>ADJ(8:0) = 0x19F, I() = -5 mA<br>ADJ(8:0) = 0x1BF, I() = -10 mA<br>ADJ(8:0) = 0x1DF, I() = -25 mA<br>ADJ(8:0) = 0x1FF, I() = -40 mA | | | <br>1<br>1<br>1<br>1.2 | <br>V<br>V<br>V<br>V |
| 602 | Isc()hi | Short-Circuit Current hi | V() = 0...VDD - 1 V;<br>ADJ(8:0) = 0x19F<br>ADJ(8:0) = 0x1BF<br>ADJ(8:0) = 0x1DF<br>V(PWR) = 0...VDD - 1.2 V;<br>ADJ(8:0) = 0x1FF | <br>-10<br>-20<br>-50<br><br>-100 | | <br>-4<br>-8<br>-20<br><br>-40 | <br>mA<br>mA<br>mA<br><br>mA |
| **Bias Current Source and Reference Voltages** | | | | | | | |
| 801 | VBG | Bandgap Reference Voltage | | 1.2 | 1.25 | 1.3 | V |
| 802 | VPAH | Reference Voltage Source | | 45 | 50 | 55 | %VDDS |
| 803 | VOSref | S/C a. Z Offset Cal. Reference Voltage Source | | 450 | 500 | 550 | mV |
| 804 | IBN | Bias Current Source | CFGIBN = 0x0<br>CFGIBN = 0xF<br>calibrated at Tj = 25 °C | 110<br><br>180 | <br><br>200 | <br>370<br>220 | µA<br>µA<br>µA |

## ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3...5.5 V, $T_j$ = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise noted.

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Alarm Message Output: NERR** | | | | | | | |
| B01 | Vs()lo | Saturation Voltage lo | Versus GND; I() = 4 mA | | | 0.4 | V |
| B02 | Isc()lo | Short-Circuit Current lo | Versus GND; V(NERR) ≤ VDD<br>V(NERR) > VTMon | 4 | 5<br>2 | 8 | mA<br>mA |
| B03 | Ipu() | Pull-Up Current Source | V() = 0...VDD - 1 V; EPU = 1 | -400 | -300 | -200 | µA |
| B04 | VTMon | Setup Preparation Threshold | Increasing voltage at NERR | | | VDD +2 | V<br>V |
| B05 | VTMoff | Setup Trigger Threshold | Decreasing voltage at NERR | VDD + 0.5 | | | V |
| B06 | VTMhys | Setup Trigger Threshold Hysteresis | VTMhys = VTMon - VTMoff | 0.15 | 0.3 | | V |
| B07 | dt()lo | Alarm Indication Time Tolerance | Nominal time see Table 37 | -25 | | +25 | % |
| **Supply Switch and Reverse Polarity Protection: VDDS, GNDS** | | | | | | | |
| C01 | I(VDDS) | Permissible VDDS Load Current | | -20 | | 0 | mA |
| C02 | Vs() | Saturation Voltage VDDS vs. VDD | Vs() = VDD - V(VDSS); I(VDDS) = -20 mA | | | 250 | mV |
| C03 | Vs() | Saturation Voltage GNDS vs. GNDS | Vs() = V(GNDS) - GND; I(GNDS) = 20 mA | | | 250 | mV |
| C04 | C() | Backup Capacitor Analog Supply VDDS vs. GNDS | | 100 | | | nF |
| **Serial EEPROM Interface: SDA, SCL** | | | | | | | |
| D01 | Vs()lo | Saturation Voltage lo | I() = 4 mA | | | 400 | mV |
| D02 | Isc() | Short-Circuit Current lo | | 4 | | 75 | mA |
| D03 | Vt()hi | Input Threshold Voltage hi | | | | 2 | V |
| D04 | Vt()lo | Input Threshold Voltage lo | | 0.8 | | | V |
| D05 | Vt()hys | Input Threshold Hysteresis | Vt()hys = Vt()hi - Vt()lo | 300 | 500 | | mV |
| D06 | Ipu() | Input Pull-Up Current | V() = 0...VDDS - 1 V | -600 | -300 | -60 | µA |
| D07 | Vpu() | Input Pull-Up Voltage | V() = VDDS - V(); I() = -5 µA | | | 0.4 | V |
| D08 | f(SCL) | Clock Frequency SCL | | 60 | 80 | 100 | kHz |
| D09 | tbusy()cfg | Configuration Sequence | Single reading sequence | | 36 | 48 | ms |
| **Temperature Monitoring** | | | | | | | |
| E01 | Toff | Shutdown Temperature | | | 155 | | °C |
| E02 | Thys | Shutdown Temperature Hysteresis | | | 15 | | °C |

## DEVICE SETUP

| Register Map | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| **Serial EEPROM Interface** | | | | | | | | |
| 0x00 | 0 | DEVID(6:0) | | | | | | |
| **Bias Current Source** | | | | | | | | |
| 0x01 | CFGIBN(3:0) | | | | 0 | 0 | 0 | 0 |
| **Operating Modes** | | | | | | | | |
| 0x02 | 1 | 1 | 0 | 0 | MODE(3:0) | | | |
| **Input Configurations** | | | | | | | | |
| 0x03 | 0 | 0 | 0 | 0 | 0 | INMODE | 1 | 1 |
| **S/C Signal Path, Input Configuration** | | | | | | | | |
| 0x04 | GFC(4:0) | | | | | GRSC(2:0) | | |
| 0x05 | GFS(3:0) | | | | 0 | 0 | 0 | 0 |
| 0x06 | VDCS(0) | 0 | 0 | 0 | 0 | GFS(6:4) | | |
| 0x07 | 0 | 0 | 0 | VDCS(5:1) | | | | |
| 0x08 | ORS(0) | VDCC(5:0) | | | | | | 0 |
| 0x09 | OFS(3:0) | | | | 0 | 0 | 0 | ORS(1) |
| 0x0A | 0 | 0 | ORC(1:0) | | OFS(7:4) | | | |
| 0x0B | OFC(6:0) | | | | | | | 0 |
| 0x0C | PHSC(2:0) | | | 0 | 0 | 0 | 0 | OFC(7) |
| 0x0D | 0 | 0 | 0 | 1 | 1 | PHSC(5:3) | | |
| 0x0E | 1 | BIASSC | VOSSC(1:0) | | RSC(3:0) | | | |
| **Controlled Power Supply** | | | | | | | | |
| 0x0F | ADJ(0) | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0x10 | ADJ(8:1) | | | | | | | |
| **Z Signal Path, Input Configuration** | | | | | | | | |
| 0x11 | GFZ(4:0) | | | | | GRZ(2:0) | | |
| 0x12 | OFZ(5:0) | | | | | | ORZ(1:0) | |
| 0x13 | 0 | BIASZ | VOSZ(1:0) | | RZ(3:0) | | | |
| **Error Monitoring** | | | | | | | | |
| 0x14 | EMASKA(7:0) | | | | | | | |
| 0x15 | 1 | 0 | EMTD(2:0) | | | EPH | 0 | EMASKA(8) |
| 0x16 | EMASKO(7:0) | | | | | | | |
| 0x17 | 0 | 0 | 0 | 0 | 0 | EPU | 0 | EMASKO(8) |
| 0x18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **Zero Signal Setup** | | | | | | | | |
| 0x19 | 0 | 0 | 0 | 0 | CFGZ(3:0) | | | |
| 0x1A | CFGZPOS(7:0) | | | | | | | |
| **Sine-to-Digital Conversion, Minimum Phase Distance** | | | | | | | | |
| 0x1B | SELRES(7:0) | | | | | | | |
| 0x1C | 0 | SELRES(14:8) | | | | | | |
| 0x1D | MTD(3:0) | | | | SELHYS(3:0) | | | |
| **Output Settings** | | | | | | | | |
| 0x1E | 0 | 0 | 1 | 0 | SSR(1:0) | | TRIHL(1:0) | |

| Register Map | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| **Reserved Memory Section 1** | | | | | | | | |
| 0x1F | Internal use only; keep all bits at zero for initialization | | | | | | | |
| 0x20 | Internal use only; keep all bits at zero for initialization | | | | | | | |
| **Reserved Memory Section 2** | | | | | | | | |
| 0x21 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0x22 | Internal use only; keep all bits at zero for initialization | | | | | | | |
| 0x23 | Internal use only; keep all bits at zero for initialization | | | | | | | |
| 0x24 | Application-specific OEM data | | | | | | | |
| 0x25 | Application-specific OEM data | | | | | | | |
| 0x26 | Application-specific OEM data | | | | | | | |
| 0x27 | Application-specific OEM data | | | | | | | |
| 0x28 | Application-specific OEM data | | | | | | | |
| 0x29 | Application-specific OEM data | | | | | | | |
| 0x2A | Application-specific OEM data | | | | | | | |
| 0x2B | Application-specific OEM data | | | | | | | |
| 0x2C | Application-specific OEM data | | | | | | | |
| 0x2D | Application-specific OEM data | | | | | | | |
| 0x2E | Application-specific OEM data | | | | | | | |
| **CRC Data** | | | | | | | | |
| 0x2F | CHKSUM(7:0) | | | | | | | |
| **Reserved Memory Section 3** | | | | | | | | |
| 0x30 | Internal use only; keep all bits at zero for initialization | | | | | | | |
| 0x31 | Internal use only; keep all bits at zero for initialization | | | | | | | |
| 0x32 | Internal use only; keep all bits at zero for initialization | | | | | | | |
| 0x33 | Internal use only; keep all bits at zero for initialization | | | | | | | |
| Notes | All 0 and 1 entries are mandatory for device initialization | | | | | | | |

Table 4: Register Map

## SERIAL EEPROM INTERFACE

### External EEPROM

The serial configuration interface consists of the two pins SCL and SDA and enables read access to a serial $I^2C$ EEPROM. This EEPROM must comply with the following specifications:

Operation from 3.3 V to 5 V
Min. size 512 bit, 64x8
Max. size 8 kbit, 1024x8
device ID 0x50 = 1010 000 (without R/W bit)
device ID 0xA0 = 1010 0000 (with R/W bit of 0)

**Recommended devices:**
Atmel AT24C01, ST M24C01, ST M24C02 (2K), ROHM BR24L01A-W, BR24L02-W

**NOTE:**
Devices ignoring A2...0 address bits are not suitable. Devices using a Word Address with don't care bits are not suitable.

### Power Up Configuration

Once the supply has been switched on iC-MG reads the configuration from the external EEPROM which has the device ID 0x50. Bit errors in the 0x00 to 0x2F memory area are monitored by the CRC deposited in register CHKSUM (see program example; the polynomial used is "1 0001 1101"). Should an error occur while the data is being read in the readin process is repeated; the system aborts following a fourth faulty attempt and tristates the output drivers.

### Triggering Reboot

As an alternative to a power down reset iC-MG can be triggered to again read in the configuration via pin NERR. To this end pin voltage V(NERR) must initially exceed threshold voltage VTMon (Elec. Char. item B04). Once the pin voltage has dropped to below VTMoff (Elec. Char. item B05) iC-MG starts communicating with the EEPROM. The device ID stored in register DEVID is used to address the EEPROM.

**NOTE:**
Connecting pin NERR to a cable can not be recommended as this pin is sensitive to the function described above.

### Example of CRC Calculation Routine

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x11D;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 1; // start value !!!
for (iReg = 0; iReg<47; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

## OPERATING MODES

| **MODE** | Adr 0x02, bit 3:0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Code | Operating Mode | Pin A | Pin NA | Pin B | Pin NB | Pin Z | Pin NZ | NERR |
| 0x00 | ABZ Mode | A | NA | B | NB | Z | NZ | NERR |
| 0x01 | Calibration Mode 1 | | reserved | reserved | IBN | Pz | Nz | |
| 0x02 | Calibration Mode 2 | Ps | Ns | Pc | Nc | VDCs | VDCc | |
| 0x0B | System Test Mode * | $A_4$ | $A_8$ | $B_4$ | $B_8$ | $Z_{ln}$ | | NERR |
| | * Note: Setting SELRES = 0x1B0 and SELHYS = 0xF is mandatory. | | | | | | | |

Table 5: Operating Modes

iC-MG has several modes of operation which are set via MODE. In addition to the primary operational mode *ABZ Mode* for the output of encoder quadrature signals via differential line drivers both analog and digital calibration signals can be selected which can be used to set up the integrated signal conditioning unit.

**ABZ Mode**
In *ABZ Mode* complementary signals are always output. Here, converter setting SELRES determines the A/B pulse count and zero signal settings CFGZ and CFGPOS the width and position of the generated zero signal (dependent on an enable from $Z_{ln}$).

**Calibration Mode 1, Mode 2**
So that signal amplitudes and offset voltages can be calibrated internal analog signals are switched to the output pins directly and the digital line drivers shut down. Due to internal resistances of up to 4 kΩ a high-impedance measurement is advisable.

In *Calibration Mode 1* bias current source IBN and the internal zero signal are available after the input amplifier (signals PCH-Z and NCH-Z). The calibration of IBN is described on page 11, that of the zero signal on page 15.

In *Calibration Mode 2* the conditioned sine and cosine signals are output (signals PCH-S, NCH-S, PCH-C and NCH-C). Additionally, the intermediate potentials of both input channels are also available, with VDCS for the sine and VDCC for the cosine channel. The calibration of these intermediate voltages is described on page 14.

**System Test Mode**
*System Test Mode* permits the fine adjustment of the sine and cosine input signals using digital signals. The registers mentioned above must also be set for this mode.

The $A_4$ duty cycle acts as a measure for the offset of the sine channel, with the $B_4$ duty cycle a measure for that of the cosine channel. The duty cycle at $A_8$ represents the phase error between sine and cosine or any deviation from the ideal value of 90°. The calibration of differing signal amplitudes enables the duty cycle at $B_8$. A duty cycle of 50 % is the calibration target for all digital test signals.

Signal $Z_{ln}$ is the unmasked digitized zero signal.

## BIAS CURRENT SOURCE CALIBRATION

The calibration of the bias current source in operation mode *Calibration 1* is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. clock frequency at SCL). For setup purposes the IBN bias current is measured using a 10 kΩ resistor by pin VDDS connected to pin NB. The setpoint is 200 µA which is equivalent to a voltage drop of 2 V.

**NOTE:** The measurement delivers a false reading when outputs are tristate (due to a configuration error after cycling power, for instance).

| **CFGIBN** | Adr 0x01, bit 7:4 | | |
|---|---|---|---|
| Code k | $IBN \sim \frac{31}{39-k}$ | Code k | $IBN \sim \frac{31}{39-k}$ |
| 0x0 | 79 % | 0x8 | 100 % |
| 0x1 | 81 % | 0x9 | 103 % |
| 0x2 | 84 % | 0xA | 107 % |
| 0x3 | 86 % | 0xB | 111 % |
| 0x4 | 88 % | 0xC | 115 % |
| 0x5 | 91 % | 0xD | 119 % |
| 0x6 | 94 % | 0xE | 124 % |
| 0x7 | 97 % | 0xF | 129 % |

Table 6: Bias Current Source Calibration

## INPUT CONFIGURATIONS

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Single-ended input signals can be processed by applying the input signals' reference voltage to the negative inputs, respectively to NZERO, when using the single-ended input configuration.

Both voltage and current signals can be accepted as input signals. For selection, use registers RSC and RZ.

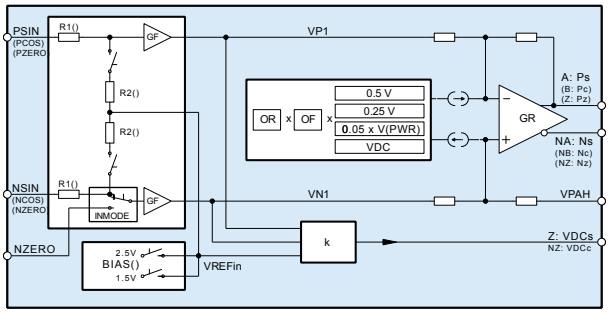



Figure 1: Input instrumentation amplifier and signal conditioning

### Voltage Signals

In voltage mode (V Mode), an optional voltage divider can be selected for high input amplitudes. This voltage divider reduces the input signal's amplitude to 25 % of the original. The internal circuit corresponds to the circuit in current mode, just the in-line resistor R1 is altered.

### Current Signals

In current mode (I Mode), an internal resistor R2() becomes active at each input, converting the current signal into a voltage signal. The effective input resistance Rin() is now determined by the sum of R1 and R2, whereas R2 is linking to the selectable reference voltage VREFin.

**Note:** The input circuit is not suitable for back-to-back photodiodes.

| **INMODE** | Adr 0x03, bit 2 |
|---|---|
| Code | Function |
| 0 | Differential input signals |
| 1 | Single-ended input signals * |
| Note | * Input NZERO is reference for all inputs. |

Table 7: Input Signal Mode

| **RSC**<br>**RZ** | Adr 0x0E, bit 3:0<br>Adr 0x13, bit 3:0 | | |
|---|---|---|---|
| Code | In-line R1() | Internal R2() | I/V Mode |
| –000 | 0.1 kΩ | 1.6 kΩ | Current input |
| –010 | 0.2 kΩ | 2.3 kΩ | Current input |
| –100 | 0.3 kΩ | 3.2 kΩ | Current input |
| –110 | 0.3 kΩ | 4.6 kΩ | Current input |
| 0—1 | 3.5 kΩ | High impedance | Voltage input 1:1 |
| 1—1 | 15 kΩ | 5 kΩ | Voltage input 4:1* |
| Notes | Nominal values; Rin = R1() + R2(); for tolerances refer to Elec.Char. No. 104, and 105.<br>For single-ended signals identical settings of RSC and RZ are required.<br>*) VREFin is the voltage divider's footpoint. Input currents may be positive or negative (Vin > VREFin, or Vin < VREFin) | | |

Table 8: I/V Mode and Input Resistance

| **BIASSC**<br>**BIASZ** | Adr 0x0E, bit 6<br>Adr 0x13, bit 6 |
|---|---|
| Code | Function |
| 0 | VREFin = 2.5 V<br>for low-side current sinks (e.g. photodiodes with common anode at GNDS) |
| 1 | VREFin = 1.5 V<br>for high-side currrent-sources (e.g. photodiodes with common cathode at VDDS)<br>for voltage sources versus ground<br>(e.g. iC-SM2, Wheatstone sensor bridges) |

Table 9: Input Bias Voltage

## S/C SIGNAL PATH and CALIBRATION

The analog voltage signals needed to calibrate the sine signals can be measured in *Calibration Mode 2*. The characteristic digital parameters for offset, amplitude and phase errors can be measured in *System Test Mode*.

### S/C Gain Settings

The gain is set in four stages:

1. The sensor supply tracking is shut down and the constant current source for the PWR output set to a suitable output current (register ADJ; current value close to the later operating point).

2. The coarse gain is selected so that differential signal amplitudes of ca. 1 Vpp are produced internally (signal PCHx vs. NCHx for the sine or cosine channel).

3. Using fine gain factor GFC the cosine signal amplitude is then adjusted to 1 Vpp.

4. The sine signal amplitude can then be calibrated to the cosine signal amplitude via fine gain factor GFS.

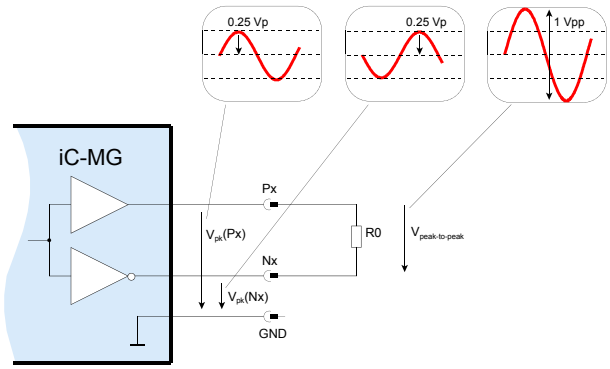



Figure 2: Definition of 1 Vpp signal. Termination R0 must be high-ohmic during all *Test* and *Calibration* modes.

| **GRSC** | Adr 0x04, bit 2:0 | |
|---|---|---|
| Code | Range with RSC=0x9 | Range with RSC≠0x9 |
| 0x0 | 0.5 | 2.0 |
| 0x1 | 1.0 | 4.1 |
| 0x2 | 1.3 | 5.3 |
| 0x3 | 1.7 | 6.7 |
| 0x4 | 2.2 | 8.7 |
| 0x5 | 2.6 | 10.5 |
| 0x6 | 3.3 | 13.2 |
| 0x7 | 4.0 | 16.0 |

Table 10: S/C-Channel Gain Range

| **GFC** | Adr 0x04, bit 7:3 |
|---|---|
| Code | Factor |
| 0x00 | 1.00 |
| 0x01 | 1.06 |
| ... | $6.25^{\frac{GFC}{31}}$ |
| 0x1F | 6.25 |

Table 11: Gain Factor Cosine

| **GFS** | Adr 0x06, bit 2:0, Adr 0x05, bit 7:4 |
|---|---|
| Code | Factor |
| 0x00 | 1.0 |
| 0x01 | 1.015 |
| ... | $6.25^{\frac{GFS}{124}}$ |
| 0x7F | 6.53 |

Table 12: Gain Factor Sine

### S/C Offset Calibration

To calibrate the offset the reference source must first be selected using VOSSC. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which already provide stable, self-regulating signals.

For the operation of photosensors in optical encoders, iC-MG tracks changes in offset voltages via the signal-dependent source VDC when used in conjunction with the controlled power supply output supplying the encoder LED (pin PWR). The VDC potential automatically tracks higher DC photocurrents. To this end intermediate potentials VDCS and VDCC must be adjusted to a minimal AC ripple using the selectable k factor (this calibration must be repeated when the gain setting is altered).

The feedback of pin voltage V(PWR) fulfills the same task as source VDC when MR bridge sensors are supplied by the controlled power supply output. In this instance the VDC sources do not need adjusting.

| **VOSSC** | Adr 0x0E, bit 5:4 |
|---|---|
| Code | Type of source |
| 0x0 | Feedback of PWR pin voltage: V(PWR)/20<br>for supply-dependent differential voltage signals<br>for Wheatstone sensor bridges<br>to measure VDDS |
| 0x1, 0x2 | Fixed reference of 500 mV, 250 mV<br>for single-ended current or voltage signals<br>for single-ended or differential stabilized signals<br>(regulated sensor or waveform generator) |
| 0x3 | Self-tracking sources VDCS, VDCC (125...250 mV)<br>for differential current signals of photodiode arrays |

Table 13: S/C-Channel Offset Reference Source

| **VDCS**<br>**VDCC** | Adr 0x07, bit 4:0; Adr 0x06, bit 7<br>Adr 0x08, bit 6:1 |
|---|---|
| Code | $VDCi = (1 - k) \cdot VPi + k \cdot VNi$ |
| 0x00 | $k = 1/3$ |
| 0x01 | $k = 0.3386$ |
| ... | $k = 1/3 + 1/3 \cdot Code/63$ |
| 0x20 | $k = 0.5026$ (center setting) |
| ... | ... |
| 0x3F | $k = 2/3$ |
| Notes | Adjustment is required only if VOSSC = 0x3. |

Table 14: S/C-Channel Intermediate Voltages

The calibration range for the S/C offset is dependent on the selected VOSSC source and is set using ORS and ORC. Both sine and cosine signals are then calibrated using factors OFS and OFC. The calibration target is reached when the DC fraction of the differential signals PCHx versus NCHx is zero.

| **ORS**<br>**ORC** | Adr 0x09, bit 0; Adr 0x08, bit 7<br>Adr 0x0A, bit 5:4 |
|---|---|
| Code | Range |
| 00 | x1 |
| 01 | x2 |
| 10 | x6 |
| 11 | x12 |

Table 15: S/C-Channel Offset Range

| **OFS**<br>**OFC** | Adr 0xA, bit 3:0; Adr 0x9, bit 7:4<br>Adr 0xC, bit 0; Adr 0xB, bit 7:1 | | |
|---|---|---|---|
| Code | Factor | Code | Factor |
| 0x00 | 0 | 0x80 | 0 |
| 0x01 | 0.0079 | 0x81 | -0.0079 |
| ... | ... | ... | ... |
| 0x7F | 1 | 0xFF | -1 |

Table 16: S/C-Channel Offset Factors

### S/C Phase Correction

If the phase shift between the sine and cosine signal deviates from the ideal 90° this can be compensated for using parameter PHSC. Following this the calibration of the amplitude compensation, intermediate potentials and offset voltages may have to be corrected.

| **PHSC** | Adr 0xD, bit 2:0; Adr 0xC, bit 7:5 | | |
|---|---|---|---|
| Code | Correction angle | Code | Correction angle |
| 0x00 | + 0 ° | 0x20 | - 0 ° |
| 0x01 | + 0.65 ° | 0x21 | - 0.65 ° |
| ... | ... | ... | ... |
| 0x1F | + 20.2 ° | 0x3F | - 20.2 ° |

Table 17: Phase Correction

## Z SIGNAL PATH and CALIBRATION

The analog voltage signals needed to calibrate the zero signal are available in *Calibration Mode 1*. In addition it is possible to check the phase position of the PZERO/NZERO enable signal in *System Test Mode*.

### Gain Settings

Parallel to the conditioning process for the S/C signals the zero signal gain is also set step by step:

1. The tracking of the sensor supply is shut down and the constant current source for the PWR output set to a suitable output current (register ADJ; current value close to the later operating point).

2. Coarse gain is selected so that differential signal amplitudes of ca. 1 Vpp are generated internally (signal PCHx vs. NCHx).

3. GFC then permits fine gain adjustment to 1 Vpp.

| **GRZ** | Adr 0x11, bit 2:0 | |
|---|---|---|
| Code | Range with RZ=0x9 | Range with RZ≠0x9 |
| 0x0 | 0.5 | 2.0 |
| 0x1 | 1.0 | 4.1 |
| 0x2 | 1.3 | 5.3 |
| 0x3 | 1.7 | 6.7 |
| 0x4 | 2.2 | 8.7 |
| 0x5 | 2.6 | 10.5 |
| 0x6 | 3.3 | 13.2 |
| 0x7 | 4.0 | 16.0 |

Table 18: Z-Channel Gain Range

| **GFZ** | Adr 0x11, bit 7:3 |
|---|---|
| Code | Factor |
| 0x00 | 1.00 |
| 0x01 | 1.06 |
| ... | $6.25^{\frac{GFZ}{31}}$ |
| 0x1F | 6.25 |

Table 19: Z-Channel Gain Factor

### Offset Calibration

To calibrate the offset the source of supply must first be selected using VOSZ (see S/C Offset Calibration for further information). For the zero signal path the signal dependent source is VDCS.

| **VOSZ** | Adr 0x13, bit 5:4 |
|---|---|
| Code | Type of source |
| 0x0 | 0.05 · V(PWR) |
| 0x1 | 0.5 V |
| 0x2 | 0.25 V |
| 0x3 | VDC= VDCS |

Table 20: Z-Channel Offset Reference Source

| **ORZ** | Adr 0x12, bit 1:0 |
|---|---|
| Code | Range |
| 00 | x1 |
| 01 | x2 |
| 10 | x6 |
| 11 | x12 |

Table 21: Z-Channel Offset Range

| **OFZ** | Adr 0x12, bit 7:2 | | |
|---|---|---|---|
| Code | Factor | Code | Factor |
| 0x00 | 0 | 0x20 | 0 |
| 0x01 | 0.032 | 0x21 | -0.032 |
| ... | ... | ... | ... |
| 0x1F | 1 | 0x3F | -1 |

Table 22: Z-Channel Offset Factor

## SIGNAL LEVEL CONTROL and SIGNAL MONITORING

Via the controlled sensor current source (pin PWR) iC-MG can keep the input signals for the internal sine-to-digital converter constant regardless of temperature and aging effects by tracking the sensor supply.

Both the controller operating range and input signal amplitude for the controller are monitored and can be enabled for error messaging. A constant current source can be selected for the PWR output when setting the signal conditioning; the current range for the highside current source is adjusted using ADJ(6:5).

| **ADJ (6:5)** | Adr 0x10, bit 5:4 |
|---|---|
| Code | Function |
| 00 | 5 mA range |
| 01 | 10 mA range |
| 10 | 25 mA range |
| 11 | 50 mA range |

Table 23: PWR Output Current Range (applies for control modes and constant current source)

| **ADJ (8:7)** | Adr 0x10, bit 7:6 |
|---|---|
| Code | Function |
| 00 | Control to sine/cosine square |
| 01 | Control to sum of sine/cosine |
| 10 | Constant current source |
| 11 | Not permitted |

Table 24: PWR Output Operating Mode

**Notice:** Excessive input signals or internal signal clipping can interfere control operation, so that the preset operating point may not be reached (upon power up) or maintained (upon disturbances). Use Loss-of-Signal Error and PWR Control Out-of-Range Error (at max. limit) for monitoring and configure EMASKA accordingly.

| **ADJ (4:0)** | Adr 0x10, bit 3:0; Adr 0x0F, bit 7 |
|---|---|
| Code | **Square control** ADJ(8:7) = 00 |
| 0x00 | Vpp() ca. 300 mV (60 %) |
| 0x01 | Vpp() ca. 305 mV (61 %) |
| ... | ... $\approx 300\,mV\,\frac{77}{77-(1.25*Code)}$ |
| 0x19 | Vpp() ca. 500 mV (98 %) |
| ... | ... |
| 0x1F | Vpp() ca. 600 mV (120 %) |

Table 25: Setpoint Square Control (internal sin/cos signal amplitude)

In operation with the active square control mode ADJ(4:0) sets the internal signal amplitudes according to the relation $(PCHS-NCHS)^2 + (PCHC-NCHC)^2$; these should be set to 0.25 Vpk.

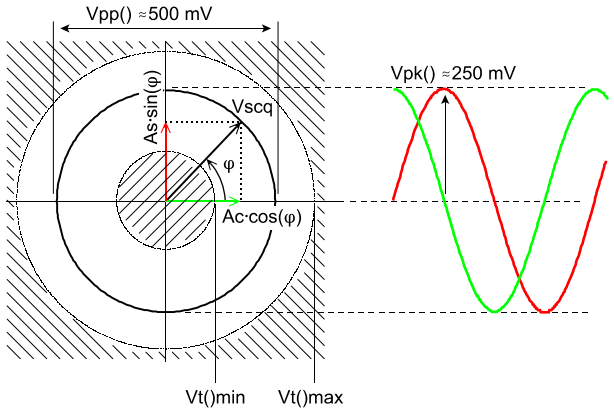



Figure 3: Internal signal monitoring and test signals in *Calibration 2* mode (example for ADJ(8:0) = 0x19).

| Signal monitoring and limits | | | |
|---|---|---|---|
| ADJ (4:0) | Vt()min ... max | ADJ (4:0) | Vt()min ... max |
| 0x00 | 120 mV...390 mV | 0x19 | 200 mV ...650 mV |
| 0x01 | 122 mV...397 mV | ... | ... |
| ... | ... | 0x1F | 240 mV...780 mV |

Table 26: Signal Monitoring (nominal values)

The signal monitoring limits are tracked according to ADJ (4:0) and fit for square control mode. When using sum control mode a different operating point can be required for which the monitoring limits may not be suitable. In this case signal monitoring should be disabled via the error mask (see EMASKA etc.).

| **ADJ (4:0)** | Adr 0x10, bit 3:0; Adr 0x0F, bit 7 |
|---|---|
| Code | **Sum control** ADJ(8:7) = 01 |
| 0x00 | VDCS + VDCC ca. 245 mV |
| 0x01 | VDCS + VDCC ca. 249 mV |
| ... | ... $\approx 245mV\,\frac{77}{77-(1.25*Code)}$ |
| 0x1F | VDCS + VDCC ca. 490 mV |

Table 27: Setpoint Sum Control (DC value)

| **ADJ (4:0)** | Adr 0x10, bit 3:0; Adr 0x0F, bit 7 |
|---|---|
| Code | **Constant current source** ADJ(8:7) = 10 |
| 0x00 | I(PWR) ca. 3.125% Isc(PWR) |
| 0x01 | I(PWR) ca. 6.25% Isc(PWR) |
| ... | ... $\approx 3.125\% * (Code + 1) * Isc(PWR)$ |
| 0x1F | I(PWR) ca. 100% Isc(PWR) |
| Notes | See Elec. Char. No. 602 for Isc(PWR) |

Table 28: Setpoint Current Source

## SINE-TO-DIGITAL CONVERSION

| **SELRES** | Adr 0x1C, bit 6:0; Adr 0x1B, bit 7:0 | | |
|---|---|---|---|
| Code | Angle Steps (per period) | Interpolation Factor | Permiss. Input Frequency |
| 0x00E0 | 4 | x1 | 500 kHz |
| 0x01B0 | 8 | x2 | 500 kHz |
| 0x0398 | 16 | x4 | 200 kHz |
| 0x0414 | 20 | x5 | 200 kHz |
| 0x078C | 32 | x8 | 125 kHz |
| 0x090A | 40 | x10 | 100 kHz |
| 0x0F86 | 64 | x16 | 62.5 kHz |
| 0x1305 | 80 | x20 | 50 kHz |
| 0x1804 | 100 | x25 | 40 kHz |
| 0x3102 | 200 | x50 | 20 kHz |

Table 29: Converter Resolution

| **SELHYS** | Adr 0x1D, bit 3:0 |
|---|---|
| Code | Function |
| 0x0 to 0x1 | Device test only |
| 0x2 | 1 conversion increment (≈ 1.8°) |
| 0x3 to 0xD | 1.5 to 6.5 conversion increments (≈ 2.7°-11.7°) |
| 0xE | 1/2 angle step increment |
| 0xF* | 1 angle step increment |
| Notes | *) Permissible from 8 angle steps upwards. |

Table 30: Converter Hysteresis

The programmable converter hysteresis is determined by SELHYS. It is set in multiples of the increment size and may have a maximum of 45° of the input signal period.

## OUTPUT SETTINGS

### Configuration of Output Drivers

The output drivers can be used as push-pull, lowside or highside drivers. TRIHL(1:0) selects the mode of operation. In order to avoid steep edges during transmission via short cables the slew rate can be reduced using SSR (tolerances as given in Electrical Characteristics).

| **TRIHL** | Adr 0x1E, bit 1:0 |
|---|---|
| Code | Function |
| 00 | Push-pull operation |
| 01 | Highside driver mode (P channel open drain) |
| 10 | Lowside driver mode (N channel open drain) |
| 11 | Not permitted |

Table 31: Output Drive Mode

| **SSR** | Adr 0x1E, bit 3:2 |
|---|---|
| Code | Function |
| 01 | Nominal value 25 ns |
| 10 | Nominal value 80 ns |
| Note | Entries 00 and 11 are not permitted |

Table 32: Output Slew Rate

### Minimum Phase Distance

The minimum phase distance for the A/B and Z output signals can be preselected using MTD(3:0). This setting limits the maximum possible output frequency for secure transmission to counters which are either unable to debounce noise spikes or only permit low input frequencies.

| **MTD** | Adr 0x1D, bit 7:4 |
|---|---|
| Code | Function |
| 0x8 | 200 ns |
| 0x9 | 400 ns |
| ... | ... |
| 0xE | 1.4 µs |
| 0xF | 1.6 µs |
| Note | Codes 0x0 to 0x7 are not permitted.<br>All timing specifications are nominal values, see Elec. Char. No. 511 for tolerances. |

Table 33: Minimum Phase Distance

When selecting the minimum phase distance the slew rate setting of the RS422 output drivers and the length of cable used must be taken into consideration.

### Zero Signal Positioning

The output of the zero pulse, generated internally, is based on an enable from $Z_{In}$ which can be observed in *System Test Mode* and in *ABZ Mode* at pin NERR (via EMASKA= 0x010 and EMTD= 0x0). As the offset calibration of the zero signal alters the signal width the correct position and width of signal $Z_{In}$ should be checked before the digital configuration parameters are determined.

The zero pulse output position can be selected via CFGZPOS(6:0); the cycle count begins with the sine zero crossing. No zero pulse is output for all values which are either greater than or equal to the interpolation factor.

| **CFGZPOS** | Adr 0x1A, bit 7:0 |
|---|---|
| Bit | Function |
| 7 | Enables the selection below |
| 6:0 | Count of A/B period releasing the Z output |

Table 34: Zero Signal Positioning

| **CFGZ** | Adr 0x19, bit 3:0 |
|---|---|
| Code | Function |
| 1ddd | Enables Z= 1 with A= 1, B= 1 |
| d1dd | Enables Z= 1 with A= 1, B= 0 |
| dd1d | Enables Z= 1 with A= 0, B= 0 |
| ddd1 | Enables Z= 1 with A= 0, B= 1 |
| Notes | d = don't care; any combination is permissible. |

Table 35: Zero Signal Logic

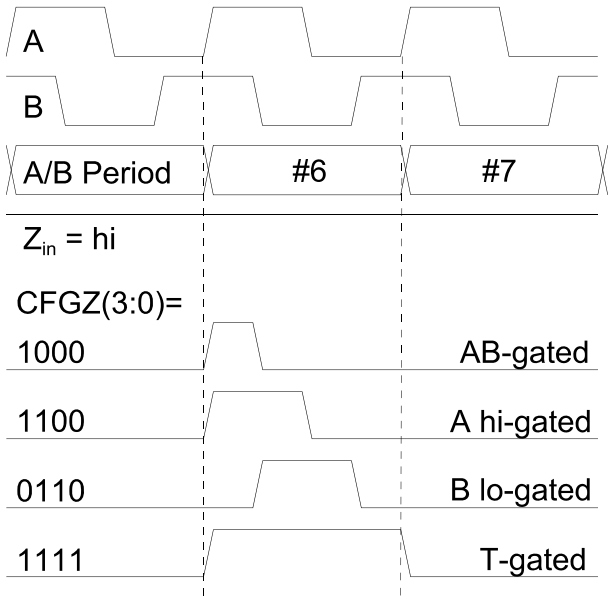



Figure 4: Zero Signal Gating Examples (example for CFGZPOS(7)=1, CFGZPOS(6:0)=0x6)

## ERROR MONITORING and ALARM OUTPUT

iC-MG monitors input signals, the internal interpolator and the controlled sensor supply via which the input signal levels are stabilized. Should the sensor supply tracking reach control limits this can be interpreted as an end-of-life message, for example.

Two separate error masks determine whether error events cause the RS422 output drivers to shutdown (mask EMASKO) or are signaled as an alarm via the current-limited open drain I/O pin NERR (mask EMASKA).

The display logic and minimum indication time are settable; an internal pull-up current source can be switched in. At the same time pin NERR has an input function to trigger a new configuration run (see Serial EEPROM Interface).

| **EPH** | Addr 0x15, bit 2 | |
|---|---|---|
| Code | State on error | State w/o error |
| 0 * | active low | high impedance, with input function for a low-active system error; |
| 1 | high impedance | active low |
| Notes | *) Pin ERR is disabled during driver shutdown and cannot indicate errors in this case. | |

Table 36: Alarm Output Logic

| **EMTD** | Adr 0x15, bit 5:3 | | |
|---|---|---|---|
| Code | Indication time | Code | Indication time |
| 0x0 | 0 ms | 0x4 | 50 ms |
| 0x1 | 12.5 ms | 0x5 | 62.5 ms |
| 0x2 | 25 ms | 0x6 | 75 ms |
| 0x3 | 37.5 ms | 0x7 | 87.5 ms |

Table 37: Minimal Alarm Indication Time

| **EPU** | Adr 0x17, bit 2 |
|---|---|
| Code | Function |
| 0 | No internal pull-up active |
| 1 | Internal 300 µA pull-up source active |

Table 38: Alarm Output Pull-Up Enable

| **EMASKA** | Adr 0x15, bit 0; Adr 0x14, bit 7:0 |
|---|---|
| Bit | Error event |
| 8 | Temporal tracking error (out-of-sync: position output differs from actual angle, e.g. after cycling power) |
| 7 | Loss of tracking due to excessive input frequency |
| 6* | Configuration error (SDA or SCL pin error, no acknowledge signal from EEPROM or invalid check sum) |
| 5 | Excessive temperature warning |
| 4 | Ungated index enable signal Zin |
| 3 | PWR control out of range (at max. limit) |
| 2 | PWR control out of range (at min. limit) |
| 1 | Signal clipping (excessive input level) |
| 0 | Loss of signal (poor differential level**, wrong s/c phase) |
| Code | Function |
| 1 | Enable: event changes state of pin ERR (if EMASKO does not disable the output function). |
| 0 | Disable: event does not affect pin ERR. |
| Notes | *) Pin ERR can not pull low on configuration error, use high-active error logic instead (EPH = 1); **) Also due to excessive input signals or internal signal clipping. |

Table 39: Error Event Mask for Alarm Output

### Driver Shutdown

Driver shutdown is a precaution to protect iC-MG. Pin PWR is set to the 5 mA range, the line drivers and pin ERR are tristate during driver shutdown.
Driver shutdown due to overheating or due to a configuration error is always enabled. Configuration errors are SDA or SCL pin error, no acknowledge signal from EEPROM or invalid checksum. EMASKO is used program driver shutdown due to other error events.

| **EMASKO** | Adr 0x17, bit 0; Adr 0x16, bit 7:0 |
|---|---|
| Bit | Error event |
| 8 | Temporal tracking error (out-of-sync: position output differs from actual angle, e.g. after cycling power) |
| 7 | Loss of tracking due to excessive input frequency |
| 6 | (Configuration error, always enabled) |
| 5 | Excessive temperature warning |
| 4 | System error: I/O pin NERR pulled to low by an external error signal (only permitted with EPH = 0) |
| 3 | PWR control out of range (at max. limit) |
| 2 | PWR control out of range (at min. limit) |
| 1 | Signal clipping (excessive input level) |
| 0 | Loss of signal (poor differential level**, wrong s/c phase) |
| Code | Function |
| 1 | Enable: event causes a driver shutdown |
| 0 | Disable: output drivers remain active |
| Notes | **) Also due to excessive input signals or internal signal clipping. |

Table 40: Error Event Mask for Driver Shutdown

## APPLICATION NOTES

### Circuit example for 1 Vpp sensors

Figure 5 introduces the principle input wiring to 1 Vpp sensors. Here, resistor RS1 provides line termination, and serial resistors RS2 and RS4 are providing ESD and overvoltage protection together with iC-MG's internal clamping circuit.

Resistor RS3 reduces the incoming signal levels to one third, so that iC-MG can be operated at a total gain of x3. The filter capacitors can be adapted, either depending on the sensor's noise level, or in accordance with the desired maximum input frequency.

Using the analog ground GNDS for the filter circuit can be recommend; the cable shield should be linked to the external ground of the IC's power supply.

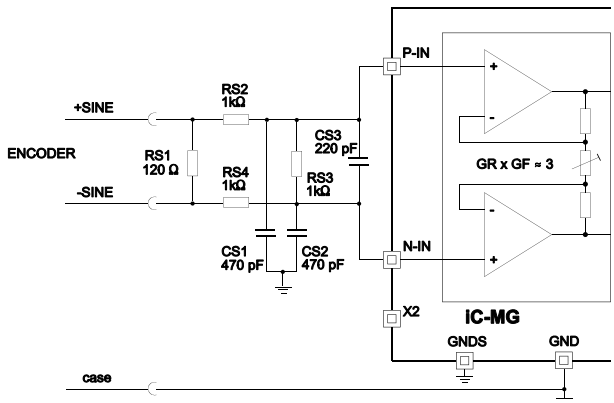



Figure 5: Principle input wiring for 1 Vpp sensors.

| CS1 | CS2 | CS3 | fc -3 dB |
|---|---|---|---|
| 2.2 nF | 2.2 nF | 470 pF | ca. 115 kHz |
| 470 pF | 470 pF | 470 pF | ca. 170 kHz |
| 470 pF | 470 pF | 220 pF | ca. 180 kHz |
| 220 pF | 220 pF | — | ca. 205 kHz |
| — | — | — | ca. 210 kHz |
| Notes | GRSC = 2, GFS = 1.5, GFC = 1.5 | | |

Table 41: Filter Cut-off Frequency (-3 dB)

### In-circuit programming of the EEPROM

To avoid bus conflicts during in-circuit programming of the EEPROM using external programming tools, iC-MG should be supplied first and must have finished its I2C master communication.

Alternatively, access to the EEPROM is unhindered as long as iC-MG's supply voltage remains below turn-off threshold VDDoff. Programming of a 2.5V-capable EEPROM can thus be possible. As iC-MG can be back biased by I2C pull-up resistors, its supply voltage may not exceed turn-on threshold VDDon.

## REVISION HISTORY

| Rel. | Rel. Date* | Chapter | Modification | Page |
|---|---|---|---|---|
| C1 | 2008-06-12 | ... | | |

| Rel. | Rel. Date* | Chapter | Modification | Page |
|---|---|---|---|---|
| D1 | 2014-08-11 | ... | See revision history of release D1 | |

| Rel. | Rel. Date* | Chapter | Modification | Page |
|---|---|---|---|---|
| D3 | 2018-04-20 | PACKAGING INFORMATION | Footnote: value of bypass cap | 2 |
| | | OPERATING MODES | Table 5: fields changed to reserved | 11 |
| | | INPUT CONFIGURATIONS | Update of description, Figure 1, Table 8 | 12 |
| | | S/C SIGNAL PATH and CALIBRATION | Figure 2 updated<br>Table 16: OFS, OFC: Code corrected | 14 |
| | | ORDERING INFORMATION | Listing updated | 22 |



* Release Date format: *YYYY-MM-DD*

## ORDERING INFORMATION

| Type | Package | Order Designation |
|---|---|---|
| iC-MG | TSSOP20 | iC-MG TSSOP20 |

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