iC-LTA
6-CH. INCREMENTAL OPTO ENCODER ARRAY

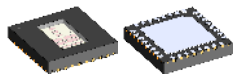
FEATURES

- Monolithic photodiode array with excellent signal matching
- Very compact size for small encoders
- Moderate track pitch for relaxed assembly tolerances
- Low noise signal amplifiers with high EMI tolerance
- Pin-selectable operating modes:
  analog, comparated (x1), interpolated (x2, x4)
- Pin-selectable index gating:
  ungated (1 T), B-gated (0.5 T), AB-gated (0.25 T)
- Complementary quadrature outputs: A, B, Z and NA, NB, NZ
- Commutation signal outputs: U, V, W
- Short-circuit-proof, current-limited, +/- 4 mA push-pull
- Analog signal output for ease of alignment and resolution enhancement by external interpolation
- LED power control with 40 mA high-side driver
- Low power consumption from single 3.5 V to 5.5 V supply
- Operating temperature range of -40 °C to +120 °C
- Space saving optoQFN / optoBGA packages (RoHS compliant)
- Custom made code disc and reticle designs on request

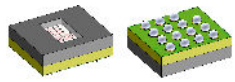
APPLICATIONS

- Incremental encoder
- Brushless DC motor commutation
- Industrial drives

PACKAGES

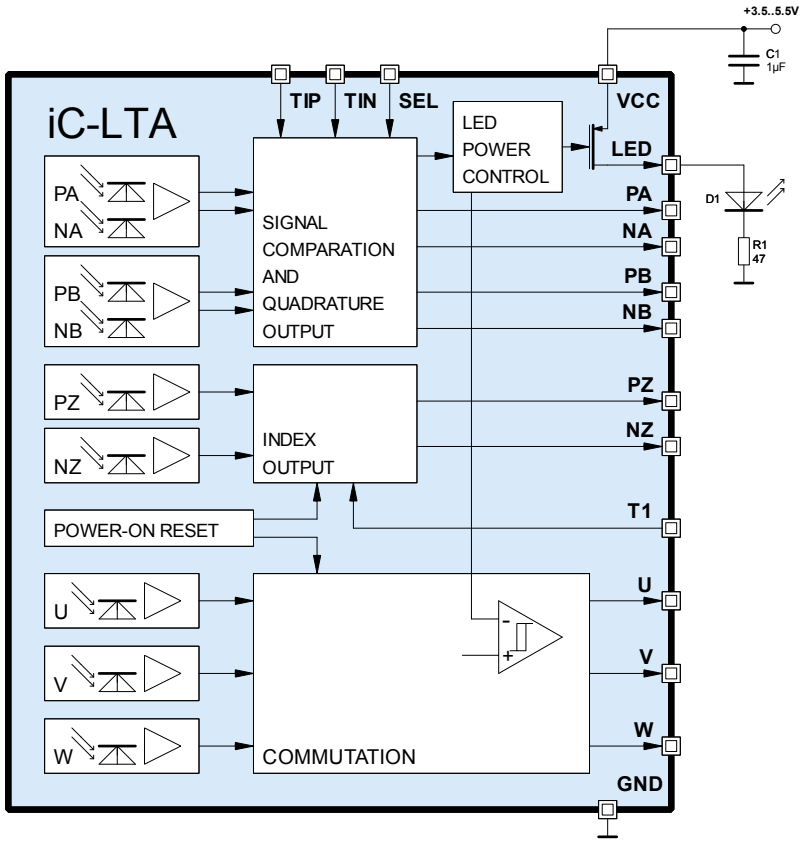


32-pin optoQFN
5 mm x 5 mm x 0.9 mm



15-pin optoBGA
6.2 mm x 5.2 mm x 1.7 mm

BLOCK DIAGRAM



DESCRIPTION

iC-LTA represents an advanced optical encoder IC featuring an array of integrated photosensors evaluated by a fast on-chip interpolation circuit to higher resolution.

Its typical application are incremental encoders for motor speed control and commutation. To this end, the device provides differential A/B tracks, a differential index track and three more tracks to generate block commutation signals.

The optical radius and the native cycles per revolution (CPR) can be freely determined by the applied code design, i.e. the code wheel and reticle (applied externally, or molded to IC as package option). The adaption to the motor polecount is also carried out by the code disc, for instance with 4 CPR and 90 degree phase shift to operate 4-phase brushless motors.

Low-noise transimpedance amplifiers, arranged in a paired layout to ensure excellent channel matching, are used to convert the scanner's signals into voltages of several hundred millivolts[1].

Precision comparators with hysteresis generate the digital signals subsequently, either native or interpolated, which are then output by differential ±4 mA push-pull drivers.

The built-in averaging LED power controller with its 40 mA driver permits a direct connection of the encoder LED. The received optical power is kept constant regardless of aging effects or changes in temperature.

Various operating modes are selectable at multi-level input SEL[2]: digital output with native (x1) or interpolated resolution (x2 or x4), analog output or mixed analog/digital output; the latter combines an output of sine/cosine signals with comparated UVW commutation signals. During analog operation the amplified signal voltages are available at the outputs for inspection and monitoring of encoder assembly, or to feed external interplation circuits.

Index gating is also pin-selectable at input T1[2, 3]: the options are ungated, respectively T-gated if using interpolated output, B-gated and AB-gated.

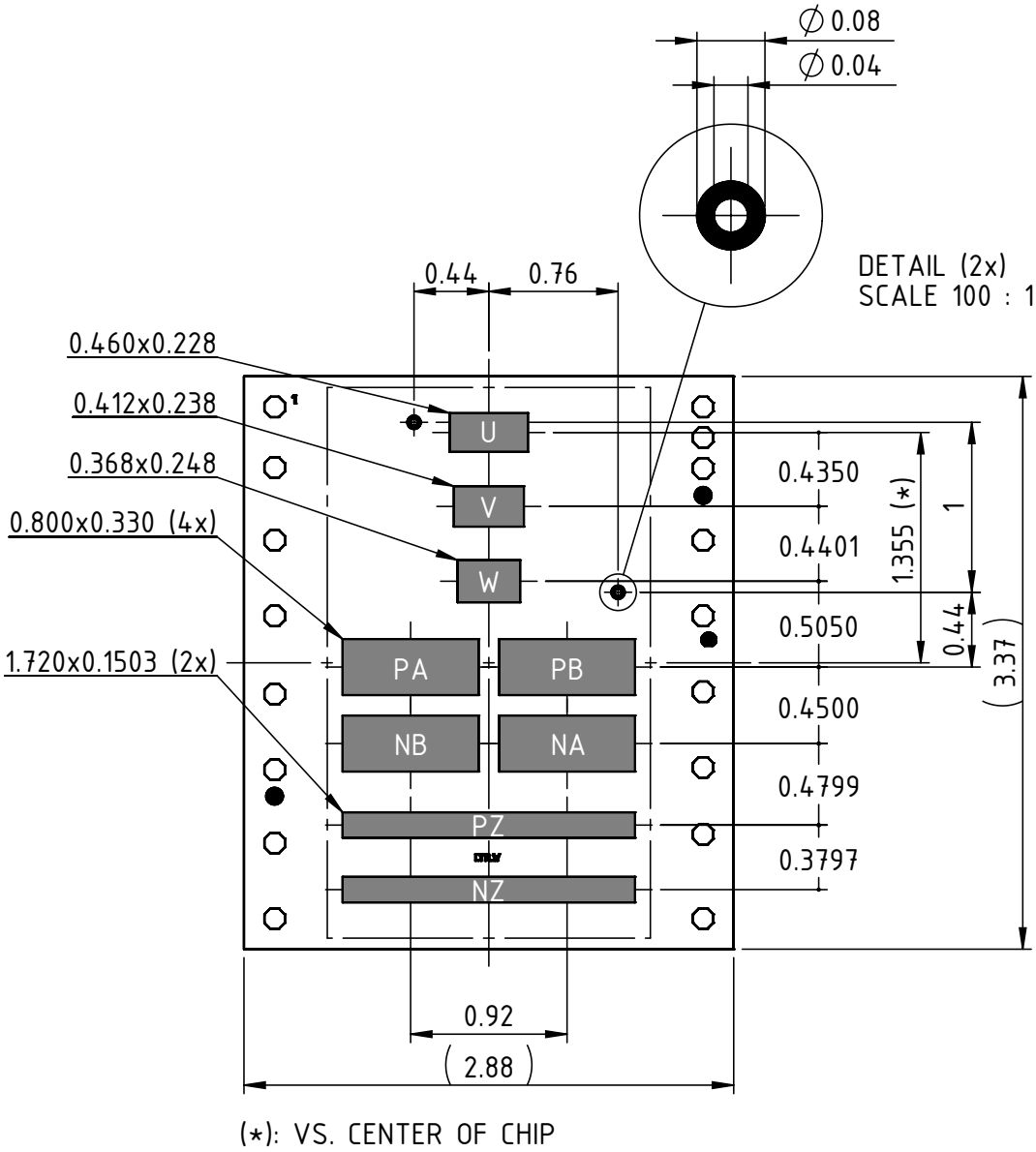
The device runs at single-sided supplies from 3.5 V up to 5.5 V and features a low power consumption.

[1] Operating point varies by code design applied.
[2] For ease of replacement, the pin functions of iC-LTA chip release W are backwards compatible to iC-LTA chip release X, and compatible to iC-PT H-Series devices.
[3] Pin T1 is not available on the oBGA LSH2C package (AB-gated index output is preset).

PACKAGING INFORMATION

Chip Layout

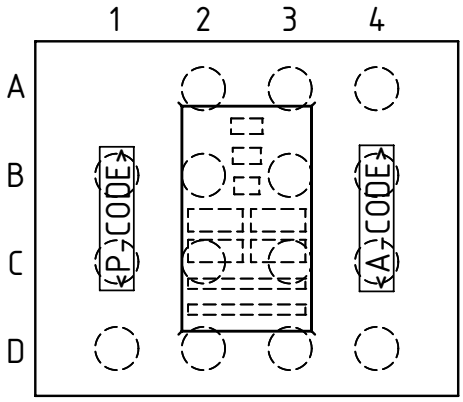
Chip release W1, chip size 2.88 mm x 3.37 mm



Notes: The center of the A/B photodiodes of the iC-LTA, as well as the ICs of the iC-PT H-Series, is located 250 µm below the chip center.
A central placement of the LED above the center of the A/B photodiodes is recommended.

To operate the LED sum control, 50 % of the total area of the AB photodiodes must be illuminated.

PIN CONFIGURATION
oBGA LSH2C (6.2 mm x 5.2 mm)

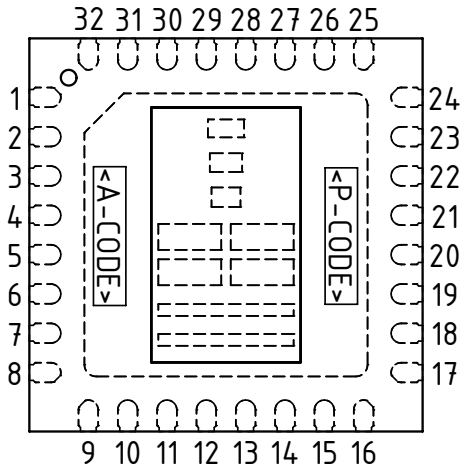


PIN FUNCTIONS

No.	Name	Function
A2	VCC	+3.5..5.5 V Supply Voltage
A3	LED	LED Controller, High-Side Current Source Output
A4	GND	Ground
B1	PA	Push-Pull Output A+ (Sin+)
B2	NA	Push-Pull Output A- (Sin-)
B3	TIP	Positive Test Current Input
B4	U	Push-Pull Output U
C1	PB	Push-Pull Output B+ (Cos+)
C2	NB	Push-Pull Output B- (Cos-)
C3	TIN	Negative Test Current Input
C4	V	Push-Pull Output V
D1	PZ	Push-Pull Output Z+ (Index+)
D2	NZ	Push-Pull Output Z- (Index-)
D3	SEL	OOp. Mode Selection Input: 100% VCC = x2 interpolated 75% VCC = ABZ analog, UVW digital 50% VCC = ABZ, UVW analog 25% VCC = x4 interpolated 0% VCC = x1 interpolated
D4	W	Push-Pull Output W

Note that this package does not feature pin T1, and AB-gated index output is preset.
For dimensional specifications refer to the relevant package data sheet, available separately.

PIN CONFIGURATION
oQFN32-5x5 (5 mm x 5 mm)

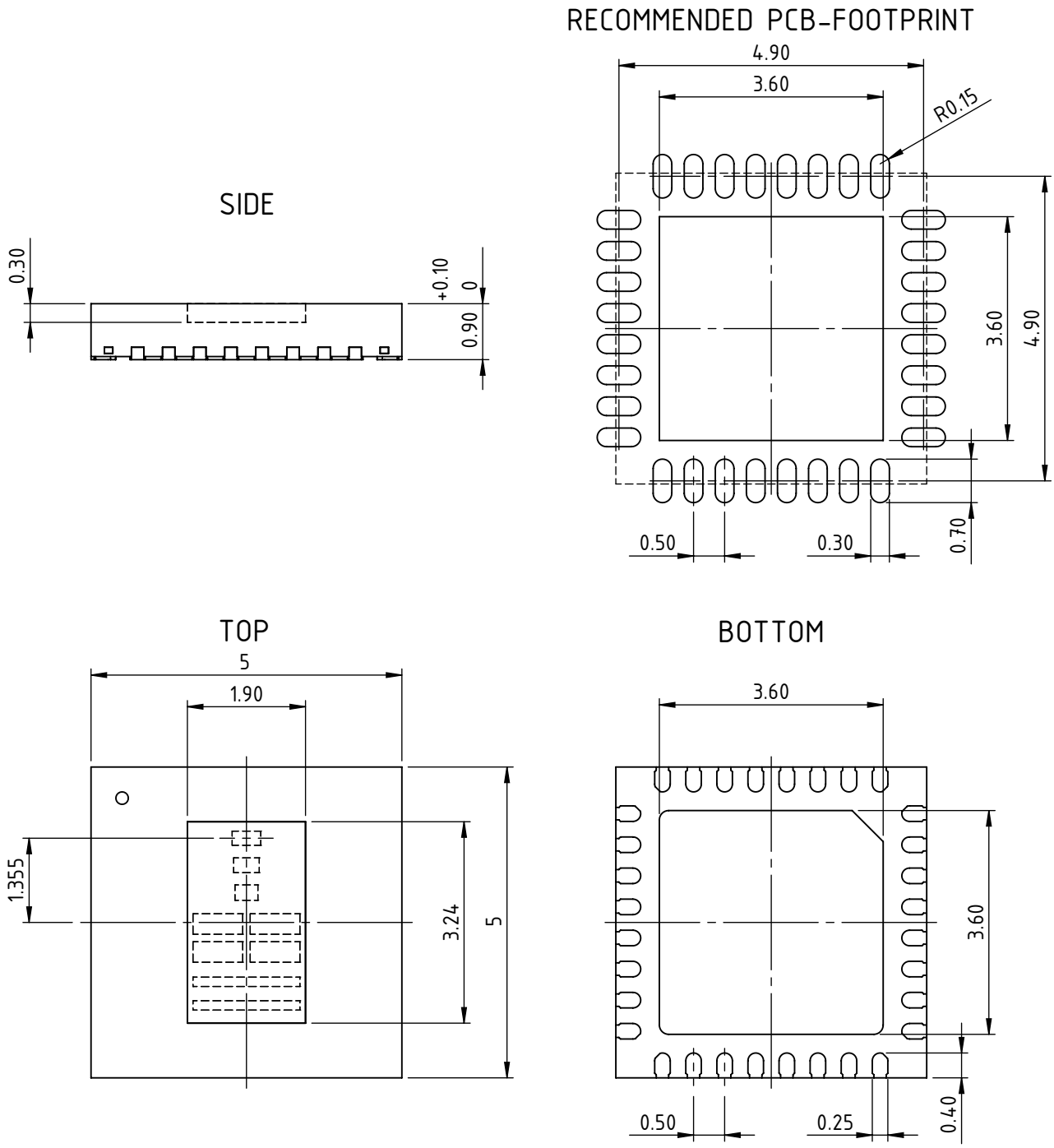


PIN FUNCTIONS

No.	Name	Function
1	VCC	+3.5..5.5 V Supply Voltage
2	LED	LED Controller, High-Side Current Source Output
3	PA	Push-Pull Output A+ / Analog Sin+ [1]
4	NA	Push-Pull Output A- / Analog Sin-
5	PB	Push-Pull Output B+ / Analog Cos+
6	NB	Push-Pull Output B- / Analog Cos-
7	PZ	Push-Pull Output Z+ / Analog Z+
8	NZ	Push-Pull Output Z- / Analog Z-
9..16	n.c.[2]	
17	SEL	Op. Mode Selection Input: 100% VCC = x2 interpolated 75% VCC = ABZ analog, UVW digital 50% VCC = ABZ, UVW analog 25% VCC = x4 interpolated 0% VCC = x1 interpolated
18	W	Push-Pull Output W / Analog W
19	TIN	Negative Test Current Input [3]
20	V	Push-Pull Output V / Analog V
21	TIP	Positive Test Current Input [3]
22	U	Push-Pull Output U / Analog U
23	T1	Index Length Selection Input: lo = 0.5 T (B-gated), hi = 1 T (ungated/T-gated), open = 0.25 T (A and B-gated)
24	GND	Ground
25..32	n.c.	
	BP	Backside Paddle [4]

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
[1] Capacitive pin loads must be avoided when using the analog output signals.
[2] Pin numbers marked n.c. are not connected.
[3] The test pins TIP and TIN may remain unconnected. If connecting traces, ensure a proper ground level to avoid unwanted functions.
[4] Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS : oQFN32-5x5



All dimensions given in mm. General Tolerances of form and position according to JEDEC MO-220.
Positional tolerance of sensor pattern: ±70µm / ±1° (with respect to center of backside pad).
Maximum molding excess +20µm / -75µm versus surface of glass. Small pits in the mold surface, which may occasionally appear due to the manufacturing process, are cosmetic in nature and do not affect reliability.

dra_oqfn32-5x5-4_lta_w_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Voltage at VCC		-0.3	6	V
G002	I(VCC)	Current in VCC		-20	20	mA
G003	V()	Voltage at Output Pins PA, NA, PB, NB, PZ, NZ, U, V, W		-0.3	VCC + 0.3	V
G004	I()	Current in Output Pins PA, NA, PB, NB, PZ, NZ, U, V, W		-20	20	mA
G005	V()	Voltage at LED		-0.3	VCC + 0.3	V
G006	I()	Current in LED		-120	20	mA
G007	V()	Voltage at TIP, TIN, SEL, T1		-0.3	VCC + 0.3	V
G008	I()	Current in TIP, TIN, SEL, T1		-20	20	mA
G009	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G010	Tj	Junction Temperature		-40	150	°C

THERMAL DATA

Operating conditions: VCC = 3.5...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package oQFN32-5x5, oBGA LSH2C	-40		120	°C
T02	Ts	Permissible Storage Temperature Range	package oQFN32-5x5, oBGA LSH2C	-40		120	°C
T03	Tpk	Soldering Peak Temperature	package oBGA LSH2C; tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering TOL (time on label) 8 h; Refer to Handling and Soldering Conditions for details.			245 230	°C °C
T04	Tpk	Soldering Peak Temperature	package oQFN32-5x5; tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering MSL 5A (max. floor life 24 h at 30 °C and 60 % RH); Refer to Handling and Soldering Conditions for details.			245 230	°C °C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 3.5...5.5 V, Tj = -40...125 °C, λ_{LED} = λr = 740 nm, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VCC	Permissible Supply Voltage		3.5		5.5	V
002	I(VCC)	Supply Current in VCC	no load, photocurrents within op. range		6	10	mA
Photosensors							
101	λar	Spectral Application Range	Se(λar) = 0.25 x S(λ)max	400		950	nm
102	λpk	Peak Sensitivity Wavelength			680		nm
103	Aph()	Radiant Sensitive Area	PA, PB, NA, NB PZ, NZ U, V, W		0.264 0.26 0.105		mm^2 mm^2 mm^2
104	S(λr)	Spectral Sensitivity	λ_{LED} = 740 nm λ_{LED} = 850 nm, 460 nm		0.5 0.3		A/W A/W
106	E()mxpk	Permissible Irradiance	λ_{LED}= λpk, Vout() < Vout()mx; PA, PB, NA, NB U, V, W PZ, NZ		 1.0 2.5 0.4		 mW/cm^2 mW/cm^2 mW/cm^2
Photocurrent Amplifiers							
201	Iph()	Permissible Photocurrent Operating Range	for PA, PB, NA, NB, U, V, W for PZ, NZ	0 0		1200 480	nA nA
202	η()r	Photo Sensitivity (light-to-voltage conversion ratio)	for PA, PB, NA, NB, U, V, W for PZ, NZ	0.15 0.4	0.25 0.65	0.35 0.9	V/µW V/µW
203	Z()	Equivalent Transimpedance Gain	Z = Vout() / Iph(), Tj = 27 °C; for PA, PB, NA, NB, U, V, W for PZ, NZ	 0.35 0.87	 0.5 1.25	 0.65 1.63	 MΩ MΩ
204	TCZ	Temperature Coefficient Of Transimpedance Gain			-0.12		%/°C
205	ΔZ()pn	Transimpedance Gain Matching	SEL open, P vs. N path per diff. channel	-0.2		0.2	%
206	ΔVout()	Dark Signal Matching of A, B	SEL open, output vs. output	-8		8	mV
207	ΔVout()	Dark Signal Matching of U, V, W	SEL open, output vs. output	-12		12	mV
208	ΔVout()	Dark Signal Matching of A, B, Z, U, V, W	SEL open, any output vs. any output	-24		24	mV
209	ΔVout()pn	Dark Signal Matching	SEL open, P vs. N path per diff. channel	-2.5		2.5	mV
211	fc()hi	Cut-off Frequency (-3 dB)		400	500		kHz
Analog Outputs: PA, NA, PB, NB, PZ, NZ, U, V, W							
301	Vout()mx	Permissible Maximum Output Voltage	illumination to E()mxpk			1.8	V
302	Iout()mx	Permissible Maximum Output Load	sink current (load to IC) source current (load to ground)	 -500		50	µA µA
303	Vout()d	Dark Signal Level	load 100 kΩ vs. +2 V	560	770	985	mV
304	Vout()acmx	Maximum Signal Level	Vout()acmx = Vout()mx - Vout()d	0.3	0.5	0.75	V
307	Ri()	Internal Output Resistance	f = 1 kHz	250	750	2250	Ω
Comparators							
401	Vt()hys	Comparator Hysteresis	Vt()hys = Vt()hi - Vt()lo		24		mV
LED Power Control							
501	Iop()	Permissible LED Output Current		-40		0	mA
502	Vs()hi	Saturation Voltage hi	Vs()hi = VCC - V(LED), I() = -40 mA		0.4	0.6	V
503	Isc()hi	Short-Circuit Current hi	V() = 0 V	-150		-50	mA
Digital Outputs: PA, NA, PB, NB, PZ, NZ, U, V, W							
601	fout	Maximum Output Frequency	x1 comparated (native resolution) x2 interpolated x4 interpolated	400 800 1600			kHz kHz kHz
602	AArel	Relative Angular Accuracy	AC signal >200 mVpp, comparated or interpolated, see Figure 1	-10		10	%

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 3.5...5.5 V, Tj = -40...125 °C, $\lambda_{LED} = \lambda r = 740$ nm, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
603	Vs()lo	Saturation Voltage lo	VCC = 4.5...5.5 V, I() = 4mA, Tj = 70 °C VCC = 4.5...5.5 V, I() = 4mA, Tj = 85 °C VCC = 3.5...4.5 V, I() = 4mA			0.4 0.5 0.6	V V V
604	Isc()lo	Short-Circuit Current lo	V() = VCC	7		70	mA
605	Vs()hi	Saturation Voltage hi	Vs()hi = VCC - V(), I() = -4 mA; VCC = 4.5...5.5 V VCC = 3.5...4.5 V			 0.4 0.6	 V V
606	Isc()hi	Short-Circuit Current hi	V() = 0 V	-70		-7	mA
Operating Mode Selection Input: SEL							
701	Vmod()	Mode Selection (see Figure 2)	x2 interpolated analog ABZ, digital UVW all analog x4 interpolated x1 comparated (native resolution)	95 70 45 20 0		100 80 55 30 5	%VCC %VCC %VCC %VCC %VCC
702	Vmod()hys	Hysteresis			10		%VCC
703	V0()	Pin-Open Voltage		45	50	55	%VCC
704	Rpd()	Pull-Down Resistor	SEL to GND, V(SEL) = VCC	65			kΩ
705	Rpu()	Pull-Up Resistor	VCC to SEL, V(SEL) = 0 V	65			kΩ
Index Gating Selection Input: T1							
801	Vgate()	Gating Selection (see Figure 3)	ungated (1 T with interpolation) AB-gated (0.25 T) B-gated (0.5 T)	82 32 0		100 68 18	%VCC %VCC %VCC
802	Vgate()hys	Hysteresis			10		%VCC
803	V0()	Pin-Open Voltage	for index length 0.25 T (AB-gated)	45	50	55	%VCC
804	Rpu()	Pull-Up Resistor	VCC to T1, V(T1) = 0 V	65			kΩ
805	Rpd()	Pull-Down Resistor	T1 to GND, V(T1) = VCC	65			kΩ
Power-On-Reset Circuit							
901	VCCon	Turn-on Threshold VCC (power-on release)	increasing voltage at VCC		2.6	3.45	V
902	VCCoff	Turn-off Threshold VCC (power-down reset)	decreasing voltage at VCC	1.4	2.4		V
903	VCChys	Threshold Hysteresis	VCChys = VCCon - VCCoff	50	170	300	mV
Test Inputs: TIP, TIN							
Z01	Ipd()	Pull-Down Current	test mode not active; V() = 0.4 V V() = VCC	60 700	100 2000	160 3000	µA µA
Z02	It()on	Test Mode Activation Threshold		80	130	190	µA
Z03	V()test	Test Pin Operating Voltage	test mode active, I() = 200 µA	1.25	1.5	1.75	V
Z04	I()test	Permissible Test Current	test mode active	10		600	µA
Z05	CR()	Current Ratio I()test/Iph()	test mode active, I() = 200 µA		1000		

ELECTRICAL CHARACTERISTICS: Diagrams

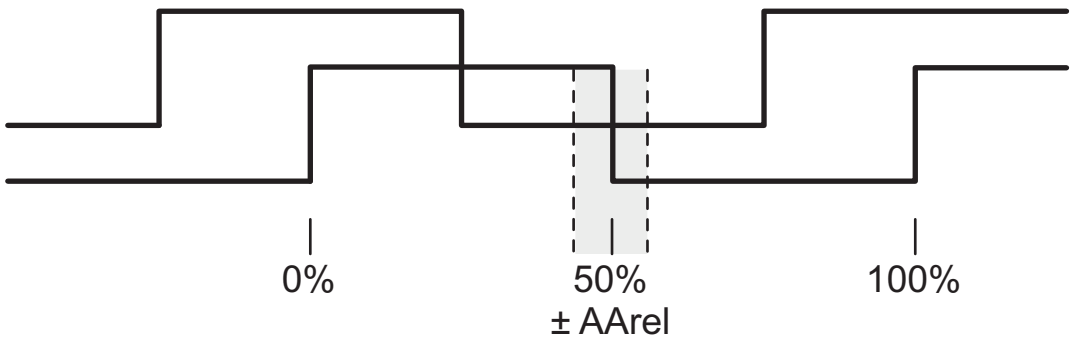


Figure 1: Definition of relative angular accuracy AArel

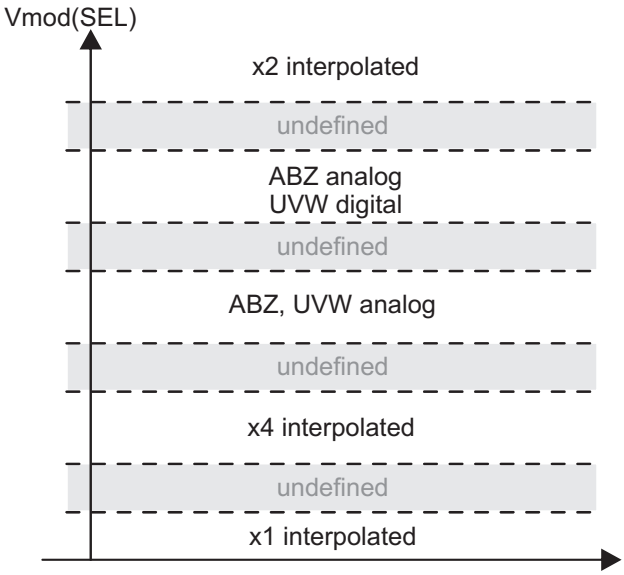


Figure 2: Operating mode selection at pin SEL.

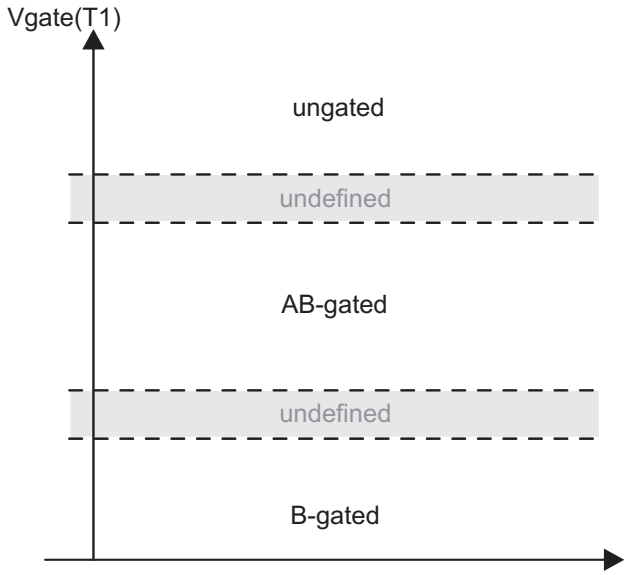


Figure 3: Index gating selection at pin T1.

DIGITAL OUTPUT SIGNALS

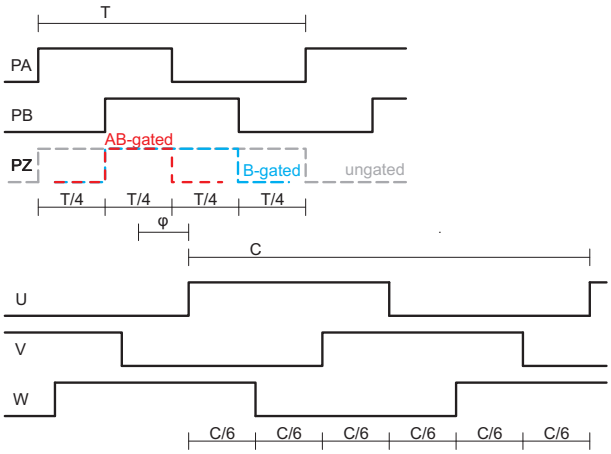


Figure 4: Typical encoder quadrature and motor commutation signals.

iC-LTA's photo-sensor array requires an external reticle (placed either on side of the IC or on side of the LED), and thus allows for a free definition of the optical radius and cycles per revolution for the A and B encoder quadrature signals.

The pulse count, period length and phase shift for the U, V, W commutation signals is also determined by the code disc design.

Contracted code disc designs and IC packaging with custom reticle can be offered on request; contact iC-Haus for details.

ANALOG OUTPUT SIGNALS

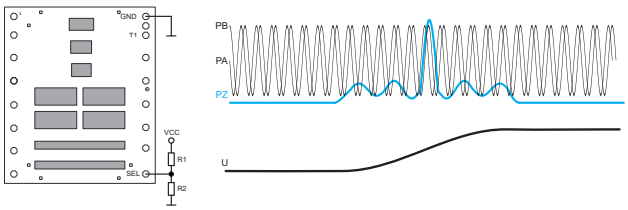


Figure 5: Example of analog ABZ / analog UVW (pin SEL = 50% VCC)

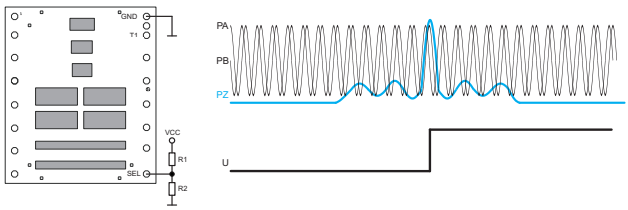


Figure 6: Example of analog ABZ / digital UVW (pin SEL = 75% VCC)

iC-LTA features 5 principle operation modes which are selectable by the voltage applied to pin SEL. A voltage divider as suggested by Table 4 is the easiest way to obtain this.

SEL	R1[1)]	R2[1)]	Operation Mode
100 % VCC	0 Ω	open	x2 interpolated
75 % VCC	2.7 kΩ	8.2 kΩ	analog ABZ, dig. UVW
50 % VCC	4.7 kΩ (open)	4.7 kΩ (open)	all analog
25 % VCC	8.2 kΩ	2.7 kΩ	x4 interpolated
0 % VCC	open	0Ω	x1 comparated
1) Exemplary values.			

Table 4: Selection of operation mode by pin SEL.

If input SEL is left open, the IC biases its input at 50% VCC and analog output signals are available for test and alignment.

Analog output signals may also be used to increase the encoder's resolution by connecting an external interpolation IC. In this case the analog signals are required permanently, so that noise immunity should be improved by wiring pin SEL to an external reference providing VCC/2.

Setting 75 % VCC may be considered to obtain analog signals at PA/PB/PZ and NA/NB/NZ outputs feeding the external interpolation IC, together with digital signals at U/V/W directly connecting a line driver. Special attention to the PCB layout should be paid to avoid cross talk; analog and digital lines should be separated carefully.

INDEX GATING AND INTERPOLATION

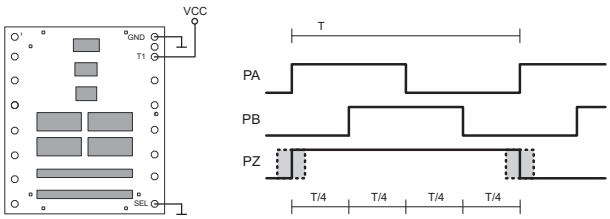


Figure 7: Ungated index (T1 = high),
x1 comparated (SEL = low).

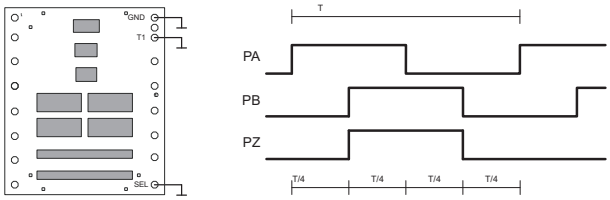


Figure 8: B-gated index (T1 = low),
x1 comparated (SEL = low).

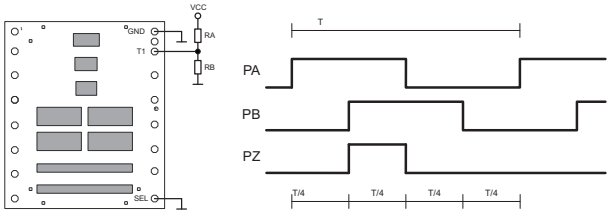


Figure 9: AB-gated index (T1 = open or VCC/2),
x1 comparated (SEL = low).

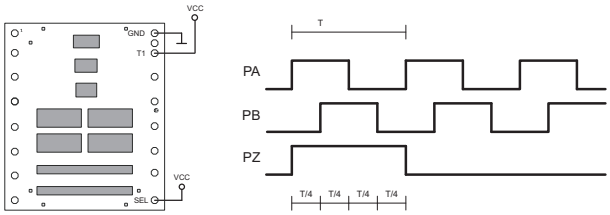


Figure 10: T-gated index (T1 = high),
x2 interpolated (SEL = high).

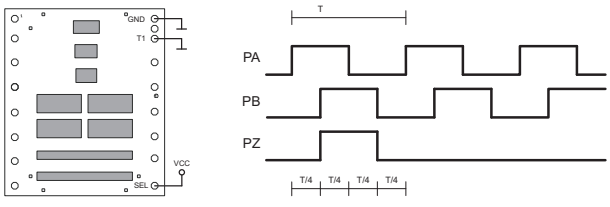


Figure 11: B-gated index (T1 = low),
x2 interpolated (SEL = high).

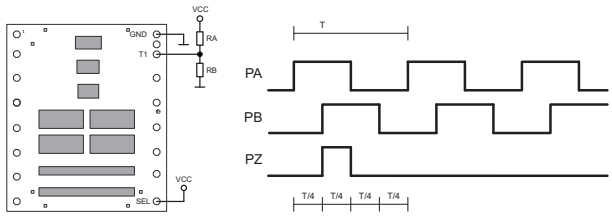


Figure 12: AB-gated index (T1 = open or VCC/2),
x2 interpolated (SEL = high).

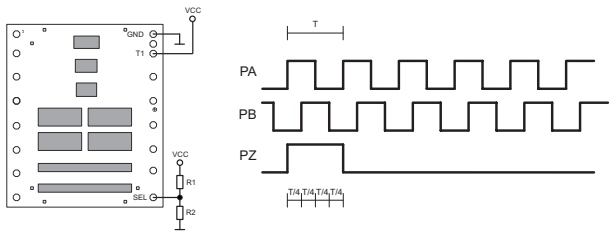


Figure 13: T-gated index (T1 = high),
x4 interpolated (SEL = 25% VCC).

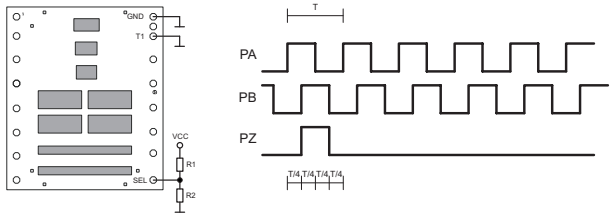


Figure 14: B-gated index (T1 = low)
x4 interpolated (SEL = 25% VCC).

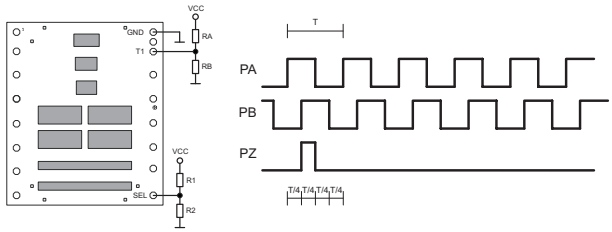


Figure 15: AB-gated index (T1 = open or VCC/2)
x4 interpolated (SEL = 25% VCC).

TEST MODE

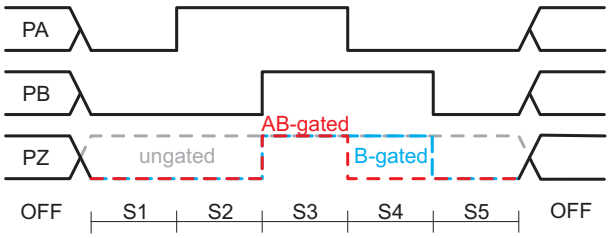


Figure 16: Output states during test mode
(SEL = low: x1 comparated)

State	I(TIP)	I(TIN)	Function	Wiring Instruction
OFF	I(TIP) $\leq$ 10 µA	I(TIN) $\leq$ 10 µA	Normal operation	
S1	I(TIP) $\geq$ 190 µA I(TIP) $\approx$ 300 µA	I(TIN) $\geq$ 190 µA I(TIN) $\approx$ 300 µA	Test mode activation (low-level at PA, PB)	 Pull-up TIN and TIN by 10 kΩ each to 5 V.
S2	I(TIP) $\approx$ 700 µA	I(TIN) $\approx$ 300 µA	Force high-level at PA	Add pull-up to TIP of 4.7 kΩ to 5 V.
S3	I(TIP) $\approx$ 700 µA	I(TIN) $\approx$ 700 µA	Force high-level at PA, PB, PZ	Add pull-up to TIN of 4.7 kΩ to 5 V.
S4	I(TIP) $\approx$ 300 µA	I(TIN) $\approx$ 700 µA	Keep high-level at PB (and PZ if B-gated)	Disconnect 4k7 pull-up from TIP.
S5	I(TIP) $\approx$ 300 µA	I(TIN) $\approx$ 300 µA	(low-level at all outputs)	Disconnect 4k7 pull-up from TIN.
OFF	I(TIP) $\leq$ 10 µA	I(TIN) $\leq$ 10 µA	Normal operation	All pull-ups removed.

Table 5: Selection of output states.

DESIGN REVIEW: Notes on Chip Functions

iC-LTA_X		
No.	Function, Parameter/Code	Description and Application Hints
		Refer to iC-LTA datasheet release B1, 2013

Table 6: Chip release iC-LTA_X

iC-LTA_W1		
No.	Function, Parameter/Code	Description and Application Hints
		None at time of printing.

Table 7: Chip release iC-LTA_W1

APPLICATION CIRCUITS

Please refer to iC-PTxx series IC's application notes which are available separately.

REVISION HISTORY

Rel.	Rel. Date[1]	Chapter	Modification	Page
C1	2016-04-18	all	New release for iC-LTA's advanced chip releases W, W1.	all

Rel.	Rel. Date[1]	Chapter	Modification	Page
C2	2019-02-01	ABSOLUTE MAXIMUM RATINGS	Item G007, G008: pin T1 added; Redundant item G011 (Ts) deleted	7
		DESIGN REVIEW: Notes on Chip Functions	Chip release W corrected to W1	13
		ORDERING INFORMATION	P/O code updated for eval board (LT14RS)	15

Rel.	Rel. Date[1]	Chapter	Modification	Page
C3	2021-06-21	PACKAGING INFORMATION	Notes added to chip layout	3
		PACKAGE DIMENSIONS	Update of oQFN package drawing and footnote	6
		THERMAL DATA	Item T03, T04: hyperlink to customer information	7

[1] Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-LTA	15-pin optoBGA, 6.2 mm x 5.2 mm, thickness 1.7 mm	AB-gated index, glass lid	iC-LTA oBGA LSH2C
		AB-gated index, on-chip reticle	iC-LTA oBGA LSH2C-xR
iC-LTA	32-pin optoQFN, 5 mm x 5 mm, thickness 0.9 mm	selectable index gating, glass lid	iC-LTA oQFN32-5x5
		selectable index gating, on-chip reticle	iC-LTA oQFN32-5x5-xR
Code Disc	glass disc 1.0 mm film disc 0.18 mm	(for contracted designs only)	LTAnnS aa-xxxx_u LTAnnFS aa-xxxx_u
Evaluation Kit	Kit with Scanner Module IC273 (61 mm x 64 mm), LED Module IC274	selectable index gating, glass lid	iC-LTA EVAL IC273
	Kit with Scanner Module IC273 (61 mm x 64 mm), LED Module IC274 and Code Disc LT14S 39-1024	selectable index gating, on-chip reticle	iC-LTA EVAL IC273 LT14RS
Illumination	Infrared LED module (28 mm x 29 mm) Blue LED module (28 mm x 29 mm)		iC-SD85 EVAL IC274 iC-TL46 EVAL IC274
Mother Board	Adapter PCB (80 mm x 110 mm)		iC277 EVAL IC277

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