iC-LNB 18-BIT OPTICAL ENCODER
WITH SPI, SERIAL, AND PARALLEL INTERFACES

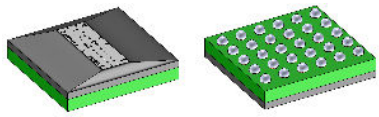
FEATURES

- System-on-chip design for excellent reliability
- Leading/trailing sampling of 10 binary tracks pitched at 400 µm
- Analog sine/cosine scanning with enlarged photodiodes, signal conditioning and fast 8-bit vector-tracking interpolation
- Absolute singleturn resolution up to 18 bits
- FlexCount® provides programmable resolution for absolute and incremental data
- Incremental quadrature outputs with 1 to 65,536 CPR and programmable index signal
- LED illumination control using 50 mA high-side current source ($\sin^2+\cos^2$ or sum control modes)
- Alarm indication for configuration or illumination error
- Permanent RAM monitoring by parity bits
- 3.3 V-compatible SPI and I/O ports for configuration and data
- Serial position readout in 1 µs cycles at 16 MHz clock frequency
- Parallel position output resolution up to 16 bits
- Operation at 4 V to 5.5 V within –40 °C to 110 °C
- 30-pin optoBGA or 38-pin optoQFN package for SMT
- Illumination: iC-SN85 BLCC SN1C (850 nm encoder LED)
- Code discs: LNB1S 42-1024 (1024 PPR, ⌀ 42 mm/18 mm), LNB4S 26-1024 (1024 PPR, ⌀ 26 mm/9.6 mm)

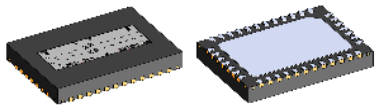
APPLICATIONS

- Programmable incremental encoders
- Optical position sensors
- Absolute rotary encoders
- Motor feedback systems
- Linear scales

PACKAGES

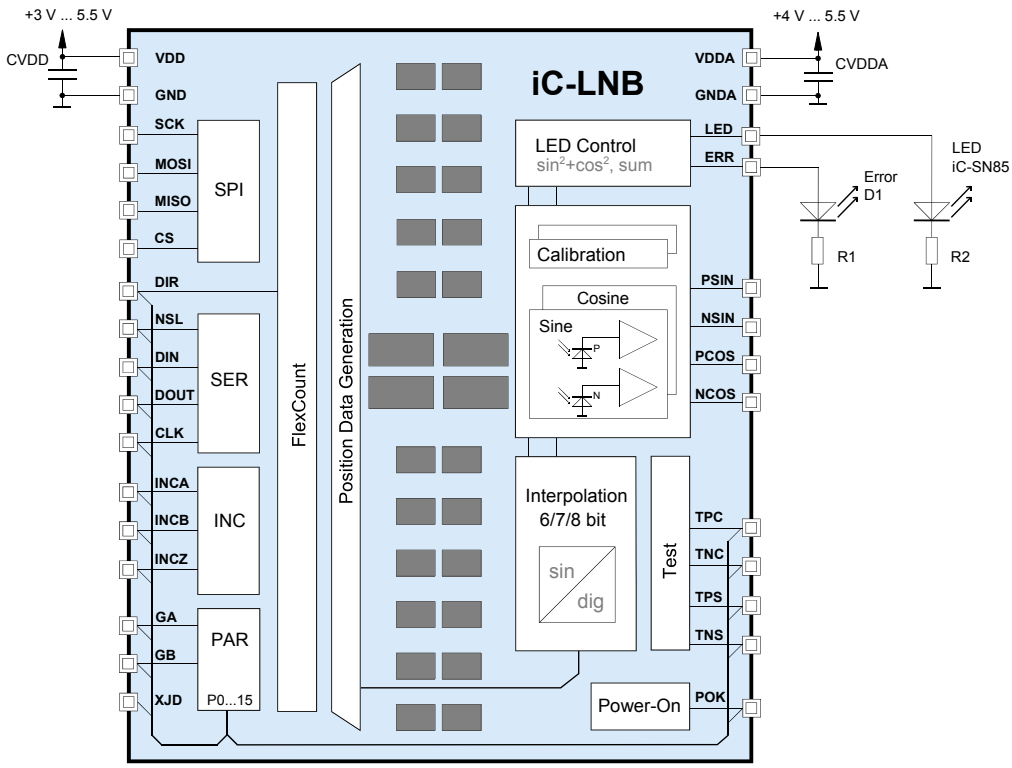


30-pin optoBGA
7.6 mm x 7.1 mm x 1.6 mm



38-pin optoQFN
7.0 mm x 5.0 mm x 0.9 mm

BLOCK DIAGRAM



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DESCRIPTION

The iC-LNB is an optoelectronic encoder IC for absolute linear and angle measuring systems. When combined with a linear scale or rotary encoder disc, the iC-LNB provides complete encoder functionality. Photodiodes, amplifiers, comparators, a complete signal conditioning unit, and multiple interfaces for position data output are monolithically integrated into the device.

The iC-LNB reads ten absolute tracks as well as an incremental track from the disc or scale. The incremental track provides sine and cosine signals which can be calibrated to compensate the offset and scale the amplitude of the photodiodes. These calibrated signals are used by the integrated vector-tracking interpolator to provide up to 8 bits of additional resolution and are also available on dedicated output pins. Combined with the 10 bits of absolute position, the interpolator provides resolution of up to 18 bits.

An integrated LED current control with a built-in driver allows direct connection of the illumination LED (iC-SN85 or other). The optical power received by the iC-LNB is kept constant by the current control, regardless of temperature and aging effects of the LED. The received power setpoint is programmable and an end-of-life alarm and error pin output indicate when the LED current control has exceeded its operating range.

The iC-LNB synchronizes the interpolator output and the absolute data to form a contiguous Gray-coded position data word. This position or angle data is output as incremental ABZ signals, absolute position via a scalable shift-register, and through the SPI interface. Alternatively, a 16-bit parallel position output is also available. FlexCount® allows the output position (incremental and absolute) resolution to be programmed to any value between 4 and 2^{18} steps (edges) per revolution.

After startup, the iC-LNB must be configured via the SPI interface. The SPI interface (as well as all the other digital I/O) operates at 3.3 V, allowing direct connection to 3.3 V microcontrollers.

General notice on application-specific programming
Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

The chip's performance in application is impacted by system conditions like the quality of the optical target, the illumination, temperature and mechanical stress, sensor alignment and initial calibration.

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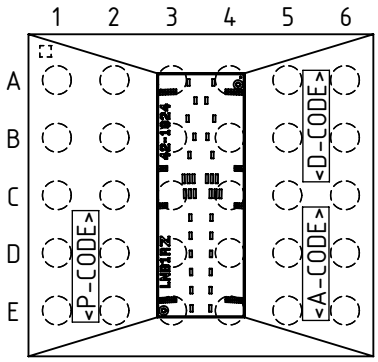
PACKAGING INFORMATION

PIN CONFIGURATION
oBGA LNB2C
(7.6 mm x 7.1 mm x 1.6 mm)



PIN FUNCTIONS

No.	Name	Function
A1	SCLK	SPI Clock Input
A2	VDD	+ 3 V ... +5.5 V I/O Ports Supply Voltage
A3	GND	I/O Ports Ground
A4	LED	LED High-Side Current Source
A5	VDDA	+ 4 V ... +5.5 V Supply Voltage
A6	GNDA	Ground
B1	CS	SPI Chip Select Input
B2	MISO	SPI Data Output
B3	MOSI	SPI Data Input
B4	PCOS	Analog Voltage Output PCOS
B5	NSIN	Analog Voltage Output NSIN
B6	PSIN	Analog Voltage Output PSIN

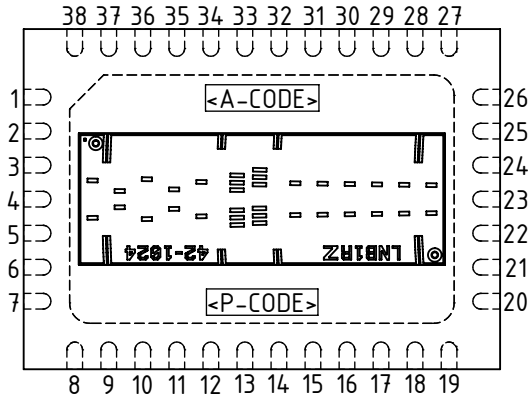
PIN FUNCTIONS

No.	Name	Function
C1	DIR	Code Inversion Input / Parallel Output Bit 13
C2	TNS	Test Input NSIN / Parallel Output Bit 14
C3	TNC	Test Input NCOS / Parallel Output Bit 15
C4	TPS	Test Input PSIN / Parallel Output Bit 1
C5	TPC	Test Input PCOS / Parallel Output Bit 0
C6	NCOS	Analog Voltage Output NCOS
D1	DOUT	Shift Register Data Output / Parallel Output Bit 10
D2	DIN	Shift Register Data Input / Parallel Output Bit 11
D3	NSL	Shift Register Load Input (active low) / Parallel Output Bit 12
D4	INCB	Incremental Output B / Parallel Output Bit 3
D5	INCA	Incremental Output A / Parallel Output Bit 2
D6	ERR	Error Message Output (active high)
E1	GB	Gray Code Output B (MSB-1) / Parallel Output Bit 7
E2	GA	Gray Code Output A (MSB) / Parallel Output Bit 8
E3	CLK	Shift Register Clock Input / Parallel Output Bit 9
E4	XJD	Adjustment Signal / Parallel Output Bit 6
E5	POK	Power OK Indication/ Parallel Output Bit 5
E6	INCZ	Incremental Output Z / Parallel Output Bit 4

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);
Grounding unused inputs (10 kΩ to GNDA) is recommended, especially for pins DIR, TPS, TNS, TPC, and TNC.
For dimensional specifications, refer to package datasheet iC-LNB oBGA LNB2C, available separately.

PIN CONFIGURATION

oQFN38-7x5 (7.0 mm x 5.0 mm x 0.9 mm)
(in qualification)



PIN FUNCTIONS

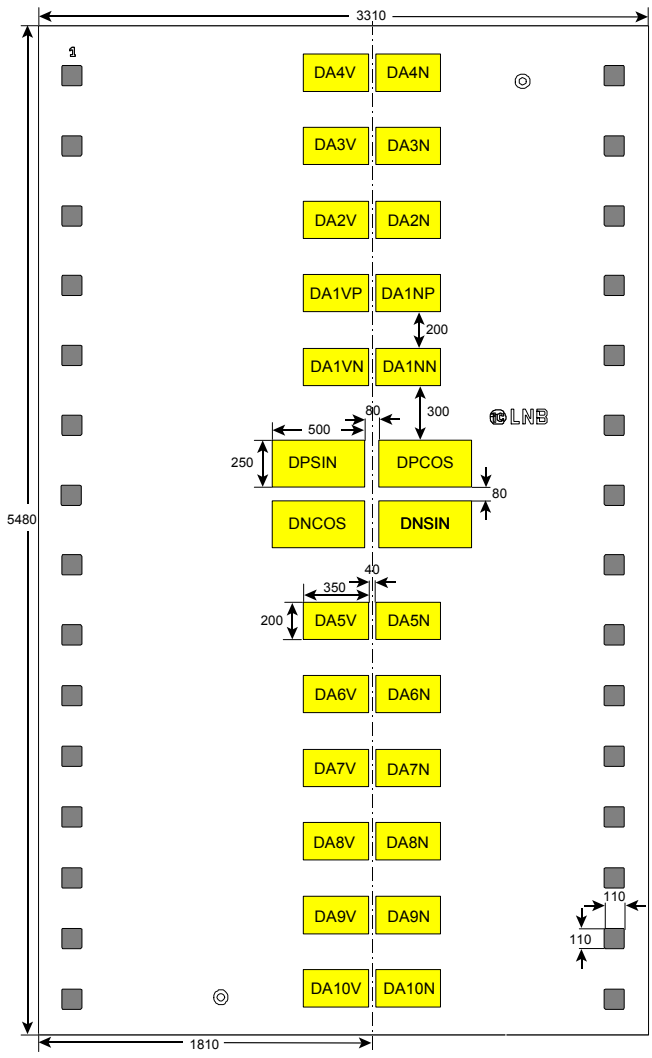
No.	Name	Function
1	GNDA	Ground
2-6	n.c. [1]	Not Connected
7	GND	I/O Ports Ground
8	VDD	+ 3 V ... +5.5 V I/O Ports Supply Voltage
9	SCLK	SPI Clock Input
10	MOSI	SPI Data Input
11	MISO	SPI Data Output
12	CS	SPI Chip Select Input
13	TNC	Test Input NCOS / Parallel Output Bit 15
14	TNS	Test Input NSIN / Parallel Output Bit 14
15	DIR	Code Inversion Input / Parallel Output Bit 13
16	NSL	Shift Register Load Input (active low) / Parallel Output Bit 12
17	DIN	Shift Register Data Input / Parallel Output Bit 11
18	DOUT	Shift Register Data Output / Parallel Output Bit 10
19	CLK	Shift Register Clock Input / Parallel Output Bit 9
20	GB	Gray Code Output B (MSB-1) / Parallel Output Bit 7
21	GA	Gray Code Output A (MSB) / Parallel Output Bit 8
22-24	n.c. [1]	Not Connected
25	POK	Power OK Indication/ Parallel Output Bit 5
26	XJD	Adjustment Signal / Parallel Output Bit 6
27	INCZ	Incremental Output Z / Parallel Output Bit 4
28	INCB	Incremental Output B / Parallel Output Bit 3
29	INCA	Incremental Output A / Parallel Output Bit 2
30	ERR	Error Message Output (active high)
31	TPS	Test Input PSIN / Parallel Output Bit 1
32	TPC	Test Input PCOS / Parallel Output Bit 0
33	NCOS	Analog Voltage Output NCOS
34	PCOS	Analog Voltage Output PCOS
35	NSIN	Analog Voltage Output NSIN
36	PSIN	Analog Voltage Output PSIN
37	LED	LED High-Side Current Source
38	VDDA	+ 4 V ... +5.5 V Supply Voltage
	BP [2]	Backside paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
Grounding unused inputs (10 kΩ to GNDA) is recommended, especially for pins DIR, TPS, TNS, TPC, and TNC.

[1] Pin numbers marked n.c. are not connected.

[2] Connecting the backside paddle is recommended by a single link to GNDA. A current flow across the paddle is not permissible.

PAD LAYOUT

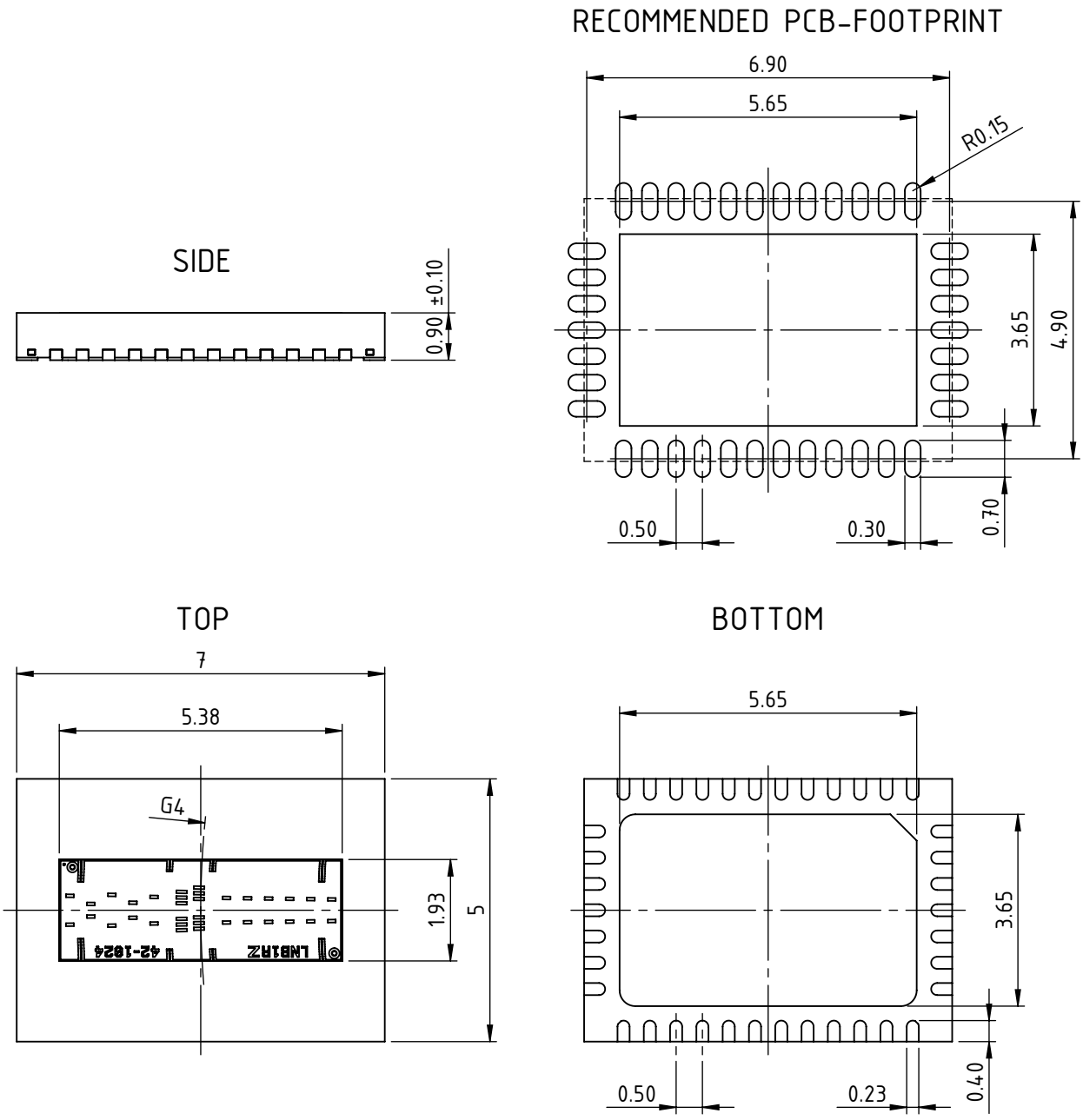


PAD FUNCTIONS

No.	Name	Function
1	GND	I/O Ports Ground
2	VDD	+ 3 V ... +5.5 V I/O Ports Supply Voltage
3	SCLK	SPI Clock Input
4	MOSI	SPI Data Input
5	MISO	SPI Data Output
6	CS	SPI Chip Select Input
7	TNC	Test Input NCOS / Parallel Output Bit 15
8	TNS	Test Input NSIN / Parallel Output Bit 14
9	DIR	Code Inversion Input / Parallel Output Bit 13
10	NSL	Shift Register Load Input (active low) / Parallel Output Bit 12
11	DIN	Shift Register Data Input / Parallel Output Bit 11
12	DOUT	Shift Register Data Output / Parallel Output Bit 10
13	CLK	Shift Register Clock Input / Parallel Output Bit 9
14	GA	Gray Code Output A (MSB) / Parallel Output Bit 8
15	GB	Gray Code Output B (MSB-1) / Parallel Output Bit 7
16	XJD	Adjustment Signal / Parallel Output Bit 6
17	POK	Power OK Indication/ Parallel Output Bit 5
18	INCZ	Incremental Output Z / Parallel Output Bit 4
19	INCB	Incremental Output B / Parallel Output Bit 3
20	INCA	Incremental Output A / Parallel Output Bit 2
21	ERR	Error Message Output (active high)
22	TPS	Test Input PSIN / Parallel Output Bit 1
23	TPC	Test Input PCOS / Parallel Output Bit 0
24	NCOS	Analog Voltage Output NCOS
25	PCOS	Analog Voltage Output PCOS
26	NSIN	Analog Voltage Output NSIN
27	PSIN	Analog Voltage Output PSIN
28	LED	LED High-Side Current Source
29	VDDA	+ 4 V ... +5.5 V Supply Voltage
30	GNDA	Ground

Grounding unused inputs (10 kΩ to GNDA) is recommended, especially for pins DIR, TPS, TNS, TPC, and TNC.

PACKAGE DIMENSIONS oQFN38-7x5



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
Positional tolerance of reticle pattern: ±90µm / ±1° (with respect to center of backside pad).
G4: radius of chip center (refer to the relevant encoder disc and code description).
Maximum molding excess +20µm / -75µm versus surface of glass/reticle.

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ABSOLUTE MAXIMUM RATINGS

These ratings do not imply permissible operating conditions; functional operation is not guaranteed.
Exceeding these ratings may damage the device.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDDA	Voltage at VDDA		-0.3	6	V
G002	VDD	Voltage at VDD		-0.3	VDDA+0.3	V
G003	V(GND)	Voltage at GND		-0.3	0.3	V
G004	V()	Voltage at LED, PCOS, NCOS, PSIN, NSIN, TPC, TNC, TPS, TNS		-0.3	VDDA+0.3	V
G005	V()	Voltage at INCA, INCB, INCZ, ERR, DIR, CLK, DOUT, DIN, NSL, CS, MOSI, MISO, SCK, POK, XJD, GA, GB		-0.3	VDD+0.3	V
G006	I(VDDA)	Current in VDDA		-100	100	mA
G007	I(VDD)	Current in VDD		-50	50	mA
G008	I(GND)	Current in GND		-20	20	mA
G009	I(LED)	Current in LED		-100	20	mA
G010	I()	Current in INCA, INCB, INCZ, ERR, DIR, CLK, DOUT, DIN, NSL, CS, MOSI, MISO, SCK, POK, XJD, GA, GB, TPC, TNC, TPS, TNS		-35	35	mA
G011	I()	Current in PCOS, NCOS, PSIN, NSIN		-35	35	mA
G012	Vd()	ESD Susceptibility at all pins	HBM 100pF discharged through 1.5 kΩ		2	kV
G013	Tj	Junction Temperature		-40	125	°C
G014	Ts	Chip Storage Temperature		-40	125	°C

THERMAL DATA

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	packages oBGA LNB2C, oQFN38-7x5	-40		110	°C
T02	Ts	Permissible Storage Temperature Range	packages oBGA LNB2C, oQFN38-7x5	-40		110	°C
T03	Tpk	Soldering Peak Temperature	package oBGA LSH2C tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering TOL (time on label) 8 h; Please refer to customer information file No. 7 for details.			 245 230	 °C °C
T04	Tpk	Soldering Peak Temperature	package oQFN38-7x5 tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering MSL 5A (max. floor life 24 h at 30 °C and 60% RH); Please refer to customer information file No. 7 for details.			 245 230	 °C °C

All voltages are referenced to ground (GNDA) unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDDA	Permissible Supply Voltage		4	5	5.5	V
002	VDD	Permissible I/O Supply Voltage	VDD ≤ VDDA	3	5	5.5	V
003	VDDA, VDD	Permissible Supply Voltage Ripple	at 150 kHz		10		mV
004	I(VDDA), I(VDD)	Supply Current in VDDA and VDD (sum)	without currents I(LED) and I(ERR), Tj = 27 °C		25	40	mA
005	Vcz()hi	Clamp Voltage hi at all Pins	I() = 4 mA			11	V
006	Vc()hi	Clamp Voltage hi at CLK, DIN, NSL, INCA, INCB, INCZ, ERR, DIR, MISO, DOUT, POK, XJD, GA, GB, TPS, TNS, TPC, TNC	Vc()hi = V() − V(VDD), I() = 4 mA	0.3		1.2	V
007	Vc()hi	Clamp Voltage hi at CS, MOSI, SCK	Vc()hi = V() − V(VDD), I() = 4 mA	1.2		2.2	V
008	Vc()lo	Clamp Voltage lo at all Pins	I() = -4 mA	-1.2		-0.3	V
009	CVDDA, CVDD	Required Backup Capacitors at VDDA, VDD	placed near by pin, recommended low ESR		1		µF
Photodiodes							
101	Se(λ)	Spectral Application Range	Se(λ) = 0.25 x S(λ)max	400		950	nm
102	S(λ)max	Spectral Sensitivity	λ = 690 nm		0.45		A/W
103	S(λ)	Spectral Sensitivity	λ = 850 nm		0.30		A/W
104	Aph()	Radiant Sensitive Area DPSIN, DNSIN, DPCOS, DNCOS	0.5 mm x 0.25 mm		0.125		mm^2
105	Aph()	Radiant Sensitive Area Digital DA1VP, DA1VN, DA1NP, DA1NN, DA2V ... DA10V, DA2N ... DA10N	0.35 mm x 0.2 mm		0.07		mm^2
Photocurrent Amplifier							
201	Iph()	Permissible Photocurrent Operating Range		0		200	nA
202	Z()	Equivalent Transimpedance Gain	Z() = Vout() / Iph()	1.8	3.0	4.2	MΩ
203	ΔZ()pn	Transimpedance Gain Matching of an Amplifier Pair	P-channel versus corresponding N-channel	-0.2		0.2	%
204	fhc()	Upper Cut-off Frequency (-3 dB)	without LED current control	120	300	500	kHz
205	VR()	Ratio of Reference Voltage Digital Tracks (Vcomp) to Sum of Digital Track 1	$VR() = \frac{Vcomp}{VA1VP + VA1VN + VA1NP + VA1NN}$		0.25		
206	Hys()	Hysteresis Digital Tracks		5	15	25	mV
207	GR()	Coarse Gain Range Analog Track	GR = 0x00 GR = 0x01 GR = 0x02 GR = 0x03	0.9 1.2 1.45 1.8	1 1.33 1.6 2	1.1 1.45 1.75 2.2	
208	Vref	Reference Voltage of Photocurrent Amplifiers		0.6	0.8	1	V
209	ΔVd()sc	Analog Track Dark Signal Voltage versus Vref	ΔVd()sc = V() - Vref	-20		20	mV
210	ΔVd()dig	Digital Tracks Dark Signal Voltage versus Vref	ΔVd()dig = V() - Vref	-35		35	mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Signal Conditioning Sin/Cos							
301	Gmin	Adjustable Minimum Gain	GS, GC = 0x00		1		
302	Gmax	Adjustable Maximum Gain	GS, GC = 0x3F		2		
303	ΔGdiff	Differential Gain Calibration Accuracy	calibration range 6 bit	-0.5		0.5	LSB
304	Omin	Offset Calibration Min	OSP, OSN, OCP, OCN = 0x00	45	47.5	50	%VDDA
305	Omax	Offset Calibration Max	OSP, OSN, OCP, OCN = 0x7F	50	52.5	55	%VDDA
306	ΔOdiff	Differential Offset Calibration Accuracy	calibration range 7 bit	0.01	0.04	0.06	%VDDA
Output Voltage PSIN, NSIN, PCOS, NCOS							
401	Vdc()	DC-Voltage at all Outputs	Offset adjusted to VDDA/2	47	50	53	%VDDA
402	Vpk()	Permissible Signal Amplitude	DC level = VDDA/2		0.5	0.6	V
403	I()mx	Permissible Output Current		-1		1	mA
404	Ri()	Output Resistor	I() = -1 . . . 1 mA		75	200	Ω
LED Power Control LED, Error Message ERR							
501	Imx()	Permissible LED Current at LED		-100		0	mA
502	Iop()	LED Current Control Range	ERRS (internal) = 0, V(LED) > Vs(LED)	-50		-1	mA
503	Vs()	Saturation Voltage at LED	Vs() = VDDA - V(LED); I() = -50 mA			1	V
504	tr()	Rise Time LED Current	I(LED): 0 % → 90 %		0.8	1.5	ms
505	tset()	Settling Time of LED Control Loop	amplitude at PSIN, NSIN, PCOS and NCOS from 50 % to 100 % of setpoint		300		µs
506	Vs()hi	Saturation Voltage hi at ERR	Vs()hi = VDD - V(ERR); VDD = 3 . . . 4 V, I() = 1.5 mA VDD = 4 . . . 5.5 V, I() = 2.5 mA			400	mV
507	Isc()hi	Short-Circuit Current hi at ERR		-100		-1.5	mA
508	Vs()lo	Saturation Voltage lo at ERR	VDD = 3 . . . 4 V, I() = 1.5 mA VDD = 4 . . . 5.5 V, I() = 2.5 mA			400	mV
509	Isc()lo	Short-Circuit Current lo at ERR		1.5		100	mA
Interpolator							
701	AAabs	Absolute Angular Position Accuracy	referenced to Sin/Cos signal period, HYS = 0x00 RESIPO = 11 (5 bit interpolation) RESIPO = 10 (6 bit interpolation) RESIPO = 01 (7 bit interpolation) RESIPO = 00 (8 bit interpolation)		 ± 7.0 ± 4.2 ± 2.8 ± 1.4		 DEG DEG DEG DEG
702	AArel	Relative Angular Error	referenced to output period T, see Figure 1 RESIPO = 11 (5 bit interpolation) RESIPO = 10 (6 bit interpolation) RESIPO = 01 (7 bit interpolation) RESIPO = 00 (8 bit interpolation)		 1 2 4 8		 % % % %
703	AAhys	Angular Hysteresis	referenced to output period T, see Figure 1 and Table 25, HYS = 0x00 RESIPO = 11 (5 bit interpolation) RESIPO = 10 (6 bit interpolation) RESIPO = 01 (7 bit interpolation) RESIPO = 00 (8 bit interpolation)		 ± 1.4 ± 1.4 ± 1.4 ± 0.7		 DEG DEG DEG DEG
704	tw()hi	Duty Cycle	referenced to output period T, see Figure 1		50		%
705	t_{AB}	Phase Shift A versus B	referenced to output period T, see Figure 1		25		%
706	f_{max}	Maximum Permissible Sin/Cos Frequency	OSZC = 10 RESIPO = 11 (5 bit interpolation) RESIPO = 10 (6 bit interpolation) RESIPO = 01 (7 bit interpolation) RESIPO = 00 (8 bit interpolation)			 250 226 113 56.5	 kHz kHz kHz kHz
707	tp_{IPO}	Propagation Delay Interpolator				$1/f_{oipo}$	

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
708	tst_{IPO}	Startup Time Interpolator	OSZC = 10, SELABS = 1, no illumination error, until POSOK = 1				
			RESIPO = 11 (5 bit interpolation):				
			startup at 14500 rpm			5	µs
			startup at standstill			2	µs
			RESIPO = 10 (6 bit interpolation):				
			startup at 13200 rpm			600	µs
			startup at 12000 rpm			30	µs
			startup at standstill			4	µs
			RESIPO = 01 (7 bit interpolation):				
			startup at 6600 rpm			1100	µs
			startup at 6000 rpm			55	µs
			startup at standstill			6	µs
			RESIPO = 00 (8 bit interpolation):				
			startup at 3300 rpm			2000	µs
			startup at 3000 rpm			100	µs
			startup at standstill			10	µs
FlexCount							
801	$AArel_{Flex}$	Additional Relative Angular Error of FlexCount	referenced to output period T, see Figure 1				
			all resolutions	0		25	%
			all binary resolutions			0	%
			maximum resolution - 4			25	%
			for RESIPO = 00 (8 bit interpolation):				
			RESSUB = 0x01387 (resolution 5 000)			0.48	%
			RESSUB = 0x04E1F (resolution 20 000)			1.92	%
			RESSUB = 0x09C3F (resolution 40 000)			3.85	%
			RESSUB = 0x3FFFB (resolution 2^{18} - 4)			25	%
802	tp_{Flex}	Propagation Delay FlexCount	additional on top of $tp_{Ipo}()$			$4/f_{oflex}$	
803	f_{max}	Maximum Permissible Sin/Cos Frequency	OSZC = 10				
			RESIPO = 11 (5 bit interpolation)			250	kHz
			RESIPO = 10 (6 bit interpolation)			226	kHz
			RESIPO = 01 (7 bit interpolation)			113	kHz
			RESIPO = 00 (8 bit interpolation)			56.5	kHz
804	tst_{Flex}	Startup Time FlexCount	OSZC = 10, SELABS = 0, no illumination error, until POSOK = 1, incl. tst_{Ipo}				
			RESIPO = 11 (5 bit interpolation):				
			startup at 14500 rpm			2.5	ms
			startup at standstill			1.5	ms
			RESIPO = 10 (6 bit interpolation):				
			startup at 13200 rpm			35	ms
			startup at 12000 rpm			15	ms
			startup at standstill			2.5	ms
			RESIPO = 01 (7 bit interpolation):				
			startup at 6600 rpm			70	ms
			startup at 6000 rpm			30	ms
			startup at standstill			5	ms
			RESIPO = 00 (8 bit interpolation):				
			startup at 3300 rpm			140	ms
			startup at 3000 rpm			60	ms
			startup at standstill			10	ms
Incremental Outputs INCA, INCB, INCZ							
901	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); VDD = 3 . . . 4 V, I() = 1.5 mA			400	mV
			VDD = 4 . . . 5.5 V, I() = 2.5 mA				
902	Isc()hi	Short-Circuit Current hi		-100		-1.5	mA
903	Vs()lo	Saturation Voltage lo	VDD = 3 . . . 4 V, I() = 1.5 mA			400	mV
			VDD = 4 . . . 5.5 V, I() = 2.5 mA				
904	Isc()lo	Short-Circuit Current lo		1.5		100	mA
905	tr()	Rise Time	CL = 30 pF, V(): 10% → 90% VDD			50	ns
906	tf()	Fall Time	CL = 30 pF, V(): 90% → 10% VDD			50	ns

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Interface SCK, CS, MISO, MOSI							
A01	Vs()hi	Saturation Voltage hi at MISO	Vs()hi = VDD - V(); VDD = 3 . . . 4 V, I() = 1.5 mA VDD = 4 . . . 5.5 V, I() = 2.5 mA			400	mV
A02	Isc()hi	Short-Circuit Current hi at MISO		-100		-1.5	mA
A03	Vs()lo	Saturation Voltage lo at MISO	VDD = 3 . . . 4 V, I() = 1.5 mA VDD = 4 . . . 5.5 V, I() = 2.5 mA			400	mV
A04	Isc()lo	Short-Circuit Current lo at MISO		1.5		100	mA
A05	fin()	Permissible Clock Frequency at SCK				10	MHz
A06	Vt()hi	Threshold Voltage hi at SCK, CS, MOSI				2	V
A07	Vt()lo	Threshold Voltage lo at SCK, CS, MOSI		0.8			V
A08	Vt()hys	Hysteresis at SCK, CS, MOSI	Vt()hys = Vt()hi - Vt()lo	40	100		mV
A09	Ipu()	Pull-Up Current at SCK, MOSI	V() = 0 . . . VDD - 1 V; VDD = 3 . . . 4 V VDD = 4 . . . 5.5 V	 -65 -120	 -25 -60	 -5 -10	 µA µA
A10	Vpu()	Pull-Up Voltage at SCK, MOSI	Vpu() = VDD - V(); VDD = 3 . . . 4 V, I() = -3 µA VDD = 4 . . . 5.5 V, I() = -5 µA			400	mV
A11	Ipd()	Pull-Down Current at CS	V() = 1 V . . . VDD; VDD = 3 . . . 4 V VDD = 4 . . . 5.5 V	 5 8	 25 60	 80 150	 µA µA
A12	Vpd()	Pull-Down Voltage at CS	VDD = 3 . . . 4 V, I() = 3 µA VDD = 4 . . . 5.5 V, I() = 5 µA			400	mV
A13	t_{P2}	Propagation Delay: MISO tristate after Falling Edge CS	CL = 10 pF, see Figure 2		30	50	ns
A14	t_{P4}	Propagation Delay: MISO Stable after Clock Edge SCK	CL = 10 pF, see Figure 2		30	60	ns
Shift Register CLK, NSL, DOUT, DIN							
B01	Vs()hi	Saturation Voltage hi at DOUT	Vs()hi = VDD - V(); VDD = 3 . . . 4 V, I() = 1.5 mA VDD = 4 . . . 5.5 V, I() = 2.5 mA			400	mV
B02	Isc()hi	Short-Circuit Current hi at DOUT		-100		-1.5	mA
B03	Vs()lo	Saturation Voltage lo at DOUT	VDD = 3 . . . 4 V, I() = 1.5 mA VDD = 4 . . . 5.5 V, I() = 2.5 mA			400	mV
B04	Isc()lo	Short-Circuit Current lo at DOUT		1.5		100	mA
B05	fin()	Permissible Clock Frequency at CLK				16	MHz
B06	Vt()hi	Threshold Voltage hi at CLK, NSL, DIN				2	V
B07	Vt()lo	Threshold Voltage lo at CLK, NSL, DIN		0.8			V
B08	Vt()hys	Hysteresis at CLK, NSL, DIN	Vt()hys = Vt()hi - Vt()lo	40	100		mV
B09	Ipu()	Pull-Up Current at CLK, NSL	V() = 0 . . . VDD - 1 V; VDD = 3 . . . 4 V VDD = 4 . . . 5.5 V	 -65 -120	 -25 -60	 -5 -10	 µA µA
B10	Vpu()	Pull-Up Voltage at CLK, NSL	Vpu() = VDD - V(); VDD = 3 . . . 4 V, I() = -3 µA VDD = 4 . . . 5.5 V, I() = -5 µA			400	mV
B11	Ipd()	Pull-Down Current at DIN	V() = 1 V . . . VDD; VDD = 3 . . . 4 V VDD = 4 . . . 5.5 V	 5 8	 25 60	 80 150	 µA µA
B12	Vpd()	Pull-Down Voltage at DIN	VDD = 3 . . . 4 V, I() = 3 µA VDD = 4 . . . 5.5 V, I() = 5 µA			400	mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B13	tp3()	Propagation Delay: DOUT Idle State after rising Edge NSL	CL = 10 pF, see Figure 3		30	50	ns
B14	tp4()	Propagation Delay: DOUT stable after Clock Edge CLK	CL = 10 pF, see Figure 3		30	60	ns
Parallel Outputs Bit 0 . . . 15 (parameter EPG = 0x1) Pins: TNC, TNS, DIR, NSL, DIN, DOUT, CLK, GA, GB, XJD, POK, INCZ, INCB, INCA, TPS, TPC							
C01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); VDD = 3 . . . 4 V, I() = 1.5 mA, VDD = 4 . . . 5.5 V, I() = 2.5 mA			400	mV
C02	Isc()hi	Short-Circuit Current hi		-100		-1.5	mA
C03	Vs()lo	Saturation Voltage lo	VDD = 3 . . . 4 V, I() = 1.5 mA, VDD = 4 . . . 5.5 V, I() = 2.5 mA			400	mV
C04	Isc()lo	Short-Circuit Current lo		1.5		100	mA
C05	tr()	Rise Time	CL = 30 pF, V(): 10% → 90% VDD			50	ns
C06	tf()	Fall Time	CL = 30 pF, V(): 90% → 10% VDD			50	ns
Power-On-Reset POK							
D01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); VDD = 3 . . . 4 V, I() = 1.5 mA, VDD = 4 . . . 5.5 V, I() = 2.5 mA			400	mV
D02	Isc()hi	Short-Circuit Current hi		-100		-1.5	mA
D03	Vs()lo	Saturation Voltage lo	VDD = 3 . . . 4 V, I() = 1.5 mA, VDD = 4 . . . 5.5 V, I() = 2.5 mA			400	mV
D04	Isc()lo	Short-Circuit Current lo		1.5		100	mA
D05	VDDAon	Turn-on Threshold VDDA, Power-on-release	increasing voltage at VDDA; POK: lo → hi	3.6	3.8	4.0	V
D06	VDDAoff	Turn-off Threshold VDDA, Power-down-reset	decreasing voltage at VDDA; EPG = 0, POK: hi → lo	3.3	3.5	3.7	V
D07	VDDAhys	Hysteresis	VDDAhys = VDDAon - VDDAoff	0.2	0.3		V
Code Inversion Input DIR							
E01	Vt()hi	Threshold Voltage hi				2	V
E02	Vt()lo	Threshold Voltage lo		0.8			V
E03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	40	100		mV
E04	Ipd()	Pull-Down Current	V() = 1 V . . . VDD; VDD = 3 . . . 4 V VDD = 4 . . . 5.5 V	 5 8	 25 60	 80 150	 µA µA
E05	Vpd()	Pull-Down Voltage	VDD = 3 . . . 4 V, I() = 3 µA VDD = 4 . . . 5.5 V, I() = 5 µA			400	mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Oscillator							
F01	f_{oipo}	Oscillator Frequency Interpolator	OSZC = 00	13.0	16.5	20.0	MHz
			OSZC = 01	13.5	17.5	21.5	MHz
			OSZC = 10	14.5	19.0	23.0	MHz
			OSZC = 11	15.0	20.0	24.0	MHz
F02	f_{oflex}	Oscillator Frequency FlexCount	OSZC = 00	14.0	17.0	20.0	MHz
			OSZC = 01	14.5	18.0	21.5	MHz
			OSZC = 10	15.5	19.5	23.0	MHz
			OSZC = 11	16.0	20.5	24.0	MHz

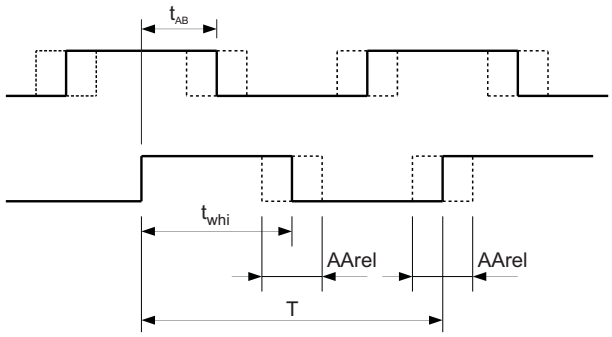

Figure 1: Definition of relative angle error

OPERATING REQUIREMENTS: SPI Interface

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	t_{C1}	Permissible Clock Period	see Elec. Char. No.: A05	1/fin()		
I002	t_{W1}	Wait Time: between CS hi → lo and CS lo → hi		500		ns
I003	t_{S1}	Setup Time: CS hi before SCK lo → hi		50		ns
I004	t_{P1}	Propagation Delay: MISO stable after CS lo → hi	CL = 10 pF		50	ns
I005	t_{P2}	Propagation Delay: MISO tristate after CS hi → lo	CL = 10 pF	Elec. Char. No.: A13		
I006	t_{H1}	Hold Time: CS hi after SCK lo → hi	valid for SPI mode 3	50		ns
I007	t_{S2}	Setup Time: MOSI stable before SCK lo → hi		50		ns
I008	t_{H2}	Hold Time: MOSI stable after SCK lo → hi		50		ns
I009	t_{P3}	Propagation Delay: MISO stable after MOSI change	mode: repeating MOSI on MISO, CL = 10 pF		50	ns
I010	t_{P4}	Propagation Delay: MISO stable after clock edge SCK	mode: sending data MISO, CL = 10 pF	Elec. Char. No.: A14		
I011	t_{W2}	Wait Time: SCK stable after CS hi → lo		500		ns
I012	t_{H3}	Hold Time: CS hi after SCK hi → lo	valid for SPI mode 0	50		ns
I013	t_{L1}	Clock Signal lo Level Duration		50		ns
I014	t_{L2}	Clock Signal hi Level Duration		50		ns

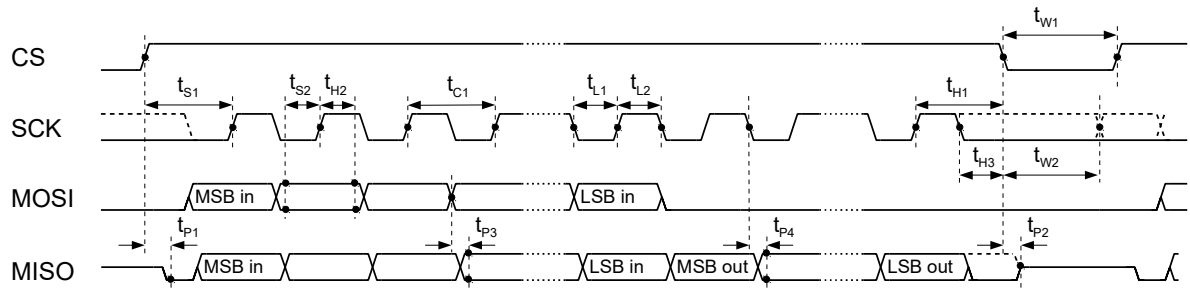

Figure 2: SPI interface timing

OPERATING REQUIREMENTS: Shift Register

Operating conditions: VDDA = 4 V to 5.5 V, VDD = 3 V to 5.5 V, GNDA = GND, Tj = -40 °C to 125 °C, unless otherwise specified.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	t_{C1}	Permissible Clock Period	see Elec. Char. No.: B05	1/fin()		
I102	t_{W1}	Wait Time Load Signal: NSL low after CLK lo → hi		30		ns
I103	t_{P1}	Propagation Delay: DOUT (idle state) after NSL lo → hi	CL = 10 pF	Elec. Char. No.: B13		
I104	t_{P2}	Propagation Delay: DOUT stable after CLK lo → hi	CL = 10 pF	Elec. Char. No.: B14		
I105	t_{S1}	Setup Time: DIN stable before CLK lo → hi		30		ns
I106	t_{H1}	Hold Time: DIN stable after CLK lo → hi		30		ns
I107	t_{W2}	Wait Time: NSL high before request of position data (CLK hi → lo)		100		ns
I108	t_{L1}	Clock Signal lo Level Duration		30		ns
I109	t_{L2}	Clock Signal hi Level Duration		30		ns

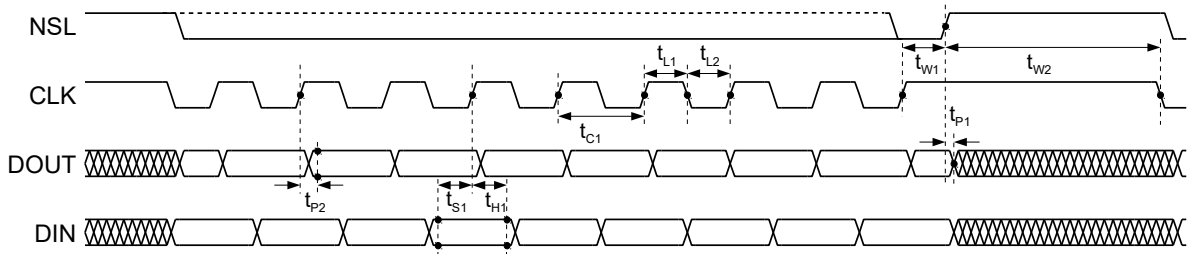

Figure 3: Shift register timing

CONFIGURATION PARAMETERS

Operating Mode ..... Page 32
EPG: Operating mode

Signal Conditioning ..... Page 26
GR: Gain range
GS: Sine gain
OSP: PSIN offset
OSN: NSIN offset
GC: Cosine gain
OCP: PCOS offset
OCN: NCOS offset

LED Power Control ..... Page 39
LCMOD: LED power control mode
LCTYP: LED power control type
LCSET(5:0): LED power control setpoint

Interpolator ..... Page 28
RESIPO: Interpolator resolution
HYS: Interpolator hysteresis
ENIPO: Interpolator enable
NENF: Interpolator filter disable

Incremental Output ..... Page 33
INC: Incremental output resolution
TRIABZ: Incremental output tristate (hi-z)

FlexCount® ..... Page 29
NENFLEX: FlexCount enable/disable
SELABS: Select maximum or FlexCount resolution for absolute outputs
RESSUB: FlexCount resolution – 1
STOPFLEX: Stop/reset FlexCount
POSOK: FlexCount position valid
NOUTLO: Set FlexCount outputs low
INVA: Invert INCA output
INVB: Invert INCB output
INVZ: Invert INCZ output
ZPOS: INCZ output position
Z90: INCZ output pulse width

Shift Register Output ..... Page 35
NENSHIFT: Shift register enable
NGRAY: Shift register output data format
RNF: Shift register idle output
SRC: Output data length
DIR: Shift register code inversion

Parallel Output Mode ..... Page 37
EPG: Operating mode

Alarm Output ..... Page 39
ERRS: LED illumination error (internal)
ERRP: Parity error (internal)

Oscillator ..... Page 40
OSZC: Oscillator adjustment

Test Functions ..... Page 41
TA: Test modes
TMUX: Test signal multiplexer

CONFIGURING THE iC-LNB

REGISTER MAP (RAM)								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Signal calibration								
0x00	P00	NENSHIFT	GS(5:0)					
0x01	P01	LCMOD	GC(5:0)					
0x02	P02	OSP(6:0)						
0x03	P03	OSN(6:0)						
0x04	P04	OCP(6:0)						
0x05	P05	OCN(6:0)						
LED Power Control								
0x06	P06	LCTYP	LCSET(5:0)					
Output Configuration								
0x07	P07	NGRAY	DIR	EPG	OSZC(1:0)		GR(1:0)	
0x08	P08	INC(2:0)			RNF	SRC(2:0)		
Test Functions								
0x09	P09	NENF	TA(1:0)		TMUX(3:0)			
FlexCount								
0x0A	P0A	0	0	0	0	HYS(2:0)		
0x0B	P0B	INVA	INVB	INVZ	TRIABZ	SELABS	NENFLEX	0
0x0C	P0C	ZPOS(6:0)						
0x0D	P0D	ZPOS(13:7)						
0x0E	P0E	RESIPO(1:0)		Z90	ZPOS(17:14)			
0x0F	P0F	RESSUB(6:0)						
0x10	P10	RESSUB(13:7)						
0x11	P11	NOUTLO	STOPFLEX	ENIPO	RESSUB(17:14)			
Status (read only)								
0x12	CHIPVERSION(3:0)				0	ERRP	ERRS	POSOK

Table 6: Register layout

Address Range

The addresses available through the SPI interface range from 0x00 to 0x12. As only the lower five bits of the address byte are evaluated, addresses greater than 0x1F are mapped back to address range 0x00 – 0x12. It is recommended not to use addresses greater than 0x12 with the iC-LNB.

RAM Monitoring (parity check)

The configuration registers in the internal RAM are constantly monitored by a parity check. Bit 7 of each address is the parity bit (P00 – P11) which must be programmed to give an even number of ones in the byte. An odd number of ones in a byte indicates a parity error (ERRP) which sets the ERRP bit in the status register (0x12 bit 2) and activates the ERR output. See ALARM OUTPUT on page 39 for more information.

Chip Version

Chip Version Addr. 0x12; bit 7:4	
Value	Description
0	V
1	U2
2...15	Reserved

Table 7: Chip Version

Reset Values

After power-on, the registers are initialized as follows:

Address	Reset Value	Description
0x00-0x01	0xA0	Gain (GS, GC) = 1.408 Shift register (NENSHIFT) = enabled LED control behavior (LCMOD) = 0
0x02-0x05	0xC0	Offset (OSP, OSN, OCP, OCN) = 0.5004*VDDA
0x06	0x60	LED control mode (LCTYP) = sum control, Set point (LCSET) = 0.23 V
0x07	0x09	Serial output format (NGRAY) = GRAY, Direction (DIR) = CW, EPG = interface mode, Oscillator (OSZC) = 16MHz, Gain range (GR) = 1.33
0x08	0x18	Interpolator factor (INC) = x2, Idle state DOUT (RNF) = '1', Shift register (SRC) = 18 bits
0x09-0x0A	0x00	Test functions = 0, Hysteresis Interpolator (HYS) = 1.4°
0x0B	0x8E	ABZ outputs (INVA/B/Z) = not inverted, ABZ outputs (TRIABZ) = tri-state, Shift register (SELABS) = max. resolution, FlexCount (NENFLEX) = disabled
0x0C-0x10	0x00	FlexCount parameters = 0
0x11	0xA0	FlexCount: Outputs (NOUTLO) = low, Reset (STOPFLEX) = stopped, Interpolator (ENIPO) = disabled

Table 8: Register Reset Values (RAM)

Programming Sequence

After the iC-LNB has powered up (pin POK high), it must be configured through the SPI interface. A microcontroller with an integrated EEPROM and SPI master is usually used for this purpose. Depending on the required application functionality, the parameters must be written in a specific order (see Figure 4 on page 20).

If the iC-LNB is to be used without FlexCount, only the required interpolator resolution (RESIPO) and the incremental output resolution (INC) need to be set and the interpolator enabled (ENIPO = 1). Enable the INCA, INCB, and INCZ output drivers by resetting TRIABZ (0).

If the iC-LNB is to be used with FlexCount, the INCA, INCB, and INCZ outputs can be set low (NOUTLO = 0 and TRIABZ = 0) or to tristate (TRIABZ = 1) during configuration. After configuring all parameters, enable FlexCount (STOPFLEX = 0). After the current position has been found (POSOK = 1), enable the INCA, INCB, and INCZ outputs (NOUTLO = 1 and TRIABZ = 0).

As shown in Figure 4, it is recommended to implement a timeout of 30ms (up to 1000 RPM) when checking for POSOK. This avoids a potential infinite loop that could happen due to glitches or communication errors. If POSOK is still 0 after some number of timeouts (typically 5), a configuration error can be assumed.

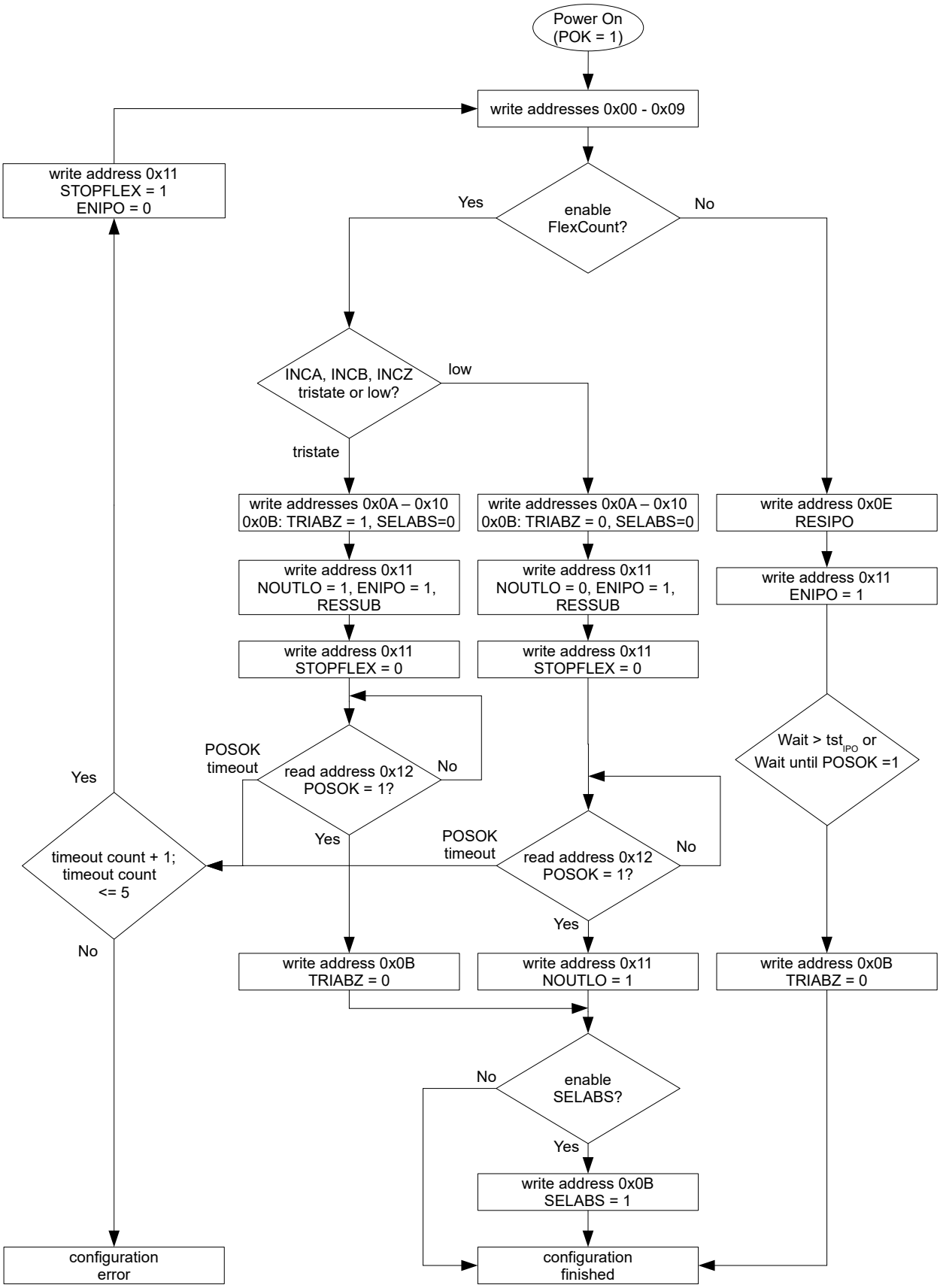

Figure 4: Typical Configuration Sequence

SPI INTERFACE

General Protocol Description

The SPI interface in the iC-LNB is implemented as an SPI slave and supports SPI modes 0 and 3, meaning that the idle state of SCLK can be 0 or 1. Data is always accepted on the rising edge of SCLK and the MISO pin is set to tristate if the iC-LNB is not selected by the master (CS=0). A rising edge on CS initiates an SPI transaction causing the MOSI signal to be fed through to MISO. Data is sent byte by byte with the MSB (most significant bit) first.

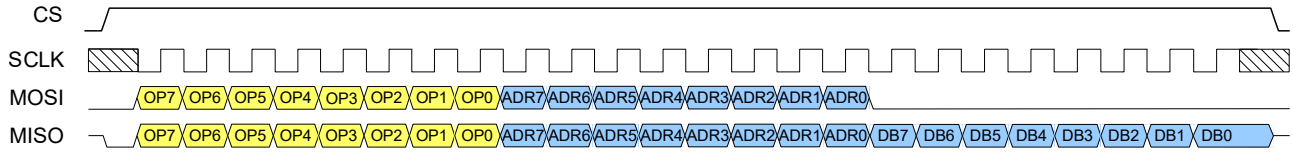

Figure 5: Typical SPI Transaction (Register Read)

Figure 5 shows a single Register Read transaction between the SPI master and a single iC-LNB (SPI slave). SPI data transactions occur as follows:

1. Master initiates a transaction with a rising edge on the chip select input (CS).
2. iC-LNB feeds MOSI through to MISO.
3. Master sends opcode and address bits on MOSI; this data is fed through to MISO.
4. iC-LNB transmits the data from the specified address to the master on MISO.
5. Master ends the transaction with a falling edge on CS.
6. iC-LNB switches its MISO output to tristate.

See Bussing and Chaining Multiple iC-LNBs on page 25 for more information on multiple-device applications.

Opcodes

Each SPI transaction begins with a 1-byte opcode (operation code or command) sent by the SPI master. As shown in Table 9, the opcode determines whether configuration (register) or sensor data (position) is accessed.

SPI Opcodes	
Code	Opcode
0xB0	Activate
0xA6	Position Read
0xF5	Position Data (SDAD) Status
0x8A	Register Read (continuous)
0xCF	Register Write (continuous)
0xAD	Register Status

Table 9: SPI Opcodes

These opcodes are explained following.

Activate

The Activate opcode (0xB0) turns the register and sensor data channels in the iC-LNB on and off individually. This command causes the iC-LNB to reset its RA (register data channel) and PA (Sensor data channel) bits, turning both channels off, and resets the Fail, Valid, Busy, and Dismiss bits in the SPI Status byte (see Table 15). The RA and PA bits in the data byte following the opcode then activate one or both channels for subsequent transactions.

With only one iC-LNB slave (one register and one sensor data channel), the RA and PA bits are bits 1 and 0 respectively in the data byte following the Activate command as shown in Figure 6.

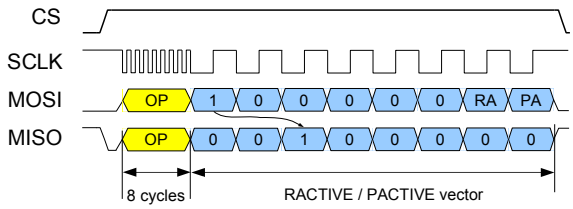

Figure 6: RA and PA (one slave)

If RA = 1, the register data channel is activated and communication with iC-LNB registers is possible. If PA = 1, the sensor data channel is activated and position (angle) information can be read. Both channels can be active at the same time. After power-on (POK = 1), the register data channel is enabled (RA = 1) and the sensor data channel is disabled (PA = 0).

Note that it is not possible for the SPI master to read back the state of the RA or PA bits to determine which data channels are active in the iC-LNB. It is only possible for it to turn both channels off and then activate each or both as required using the Activate command.

If RA = 1, opcodes Register Read, Register Write, and Register Status operate normally, as explained below. If RA = 0, these commands are not executed and, if attempted, set the Error bit in the SPI Status byte (Table 15).

Likewise, if PA = 1, the Position Read opcode operates normally, as explained below. If PA = 0, this command is not executed and, if attempted, sets the Error bit in the SPI Status byte (Table 15). All of these commands, however, are still passed through to MISO.

Position Read
The Position Read command (0xA6) is used to read the absolute position data from the iC-LNB.

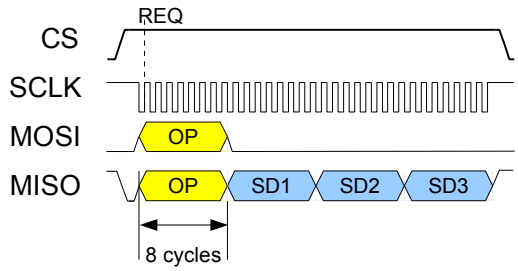

Figure 7: Position Read

As shown in Figure 7, the iC-LNB latches its position data on the first rising edge of SCLK when CS is high (REQ). The position data shift register then clocks out the latched position value on subsequent clock cycles (bytes SD1 - SD3). Position data is available in binary or Gray code.

NGRAY	Address 0x07; bit 6
Value	Data Format
0	Gray Code
1	Binary

Table 10: SPI Position Output Data Format

The sensor data channel must be activated (PA = 1) for proper operation of this command, otherwise the Error bit in the SPI Status byte is set. If invalid data is detected in the shift register, the Error bit in the SPI Status byte (Table 15) is set and SD1 = SD2 = SD3 = 0x00.

The length of the SPI shift register and the number of position bits used is determined by parameter SRC, as shown in Table 11.

SRC	Address 0x08; bits 2:0	
Value	SPI Shift Reg. Length	Number of Bits Used
0	24 bits	18
1	24 bits	17
2	16 bits	16
3	16 bits	15
4	16 bits	14
5	16 bits	13
6	16 bits	13
7	16 bits	12

Table 11: SPI Output Data Length

If SRC $\geq$ 2, only SD1 and SD2 are used. If SRC < 2, SD1, SD2, and SD3 are used.

SPI position is shifted out MSB first and left-justified. If the SPI output data length is greater than the number of bits used (SRC $\neq$ 2), the unused LSBs are zero. For example, if SRC = 1, the shift register outputs the 17-bit position value followed by seven zeros. In this case, SD3 bits [6:0] are zero.

Note that SRC is also used to set the length of the position output shift register (Table 49). However, the position output shift register is not always the same length as the SPI shift register. Also, the position output shift register outputs right-justified position data whereas the SPI position data is left-justified.

If FlexCount is selected (SELABS = 0), the number of valid position bits is determined by the FlexCount resolution, specified by parameter RESSUB. Also, if FlexCount is enabled and a non-binary resolution is used (RESSUB + 1 is not an integer power of 2), the absolute position is a value between two non-zero numbers. See FLEXCOUNT® on page 29 for more information on the absolute position numeric formats.

If FlexCount is not selected (SELABS = 1), the number of valid position bits is determined by the interpolator resolution (RESIPO), as shown in Table 12.

RESIPO	Address 0x0E; bits 6:5	
Value	Interpolator resolution	Valid Position Bits
0	8 bit	18
1	7 bit	17
2	6 bit	16
3	5 bit	15

Table 12: Valid Position Bits

Position Data (SDAD) Status
The status of position data can be checked with the SDAD Status command (0xF5). The command causes:

1. All slaves activated via PACTIVE to switch their SVALID and SFAIL registers between MOSI and MISO.

2. The next request for sensor data started with the first rising edge at SCLK of the next SPI communication is ignored by the slave.

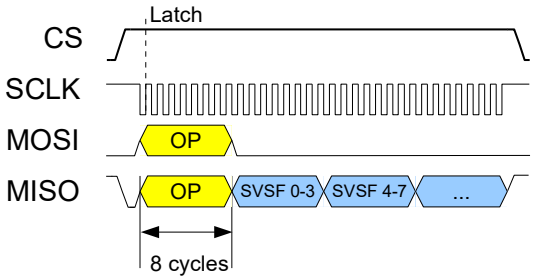

Figure 8: SDAD status

The master can check the validity of the position data and then read out this data with command **SDAD transmission**. In iC-LNB, SVALID (SV) is identical to POSOK and SFAIL (SF) is the logical complement of POSOK.

SVALID	
Value	Description
0	Position data invalid (POSOK = 0)
1	Position data valid (POSOK = 1)

Table 13: SVALID

SFAIL	
Value	Description
0	Position data request okay (POSOK = 1)
1	Position data request failed (POSOK = 0)

Table 14: SFAIL

If only one slave is connected, the corresponding SVALID (SV0) and SFAIL (SF0) bits are placed at bit positions 7 and 6 in the SVALID byte.

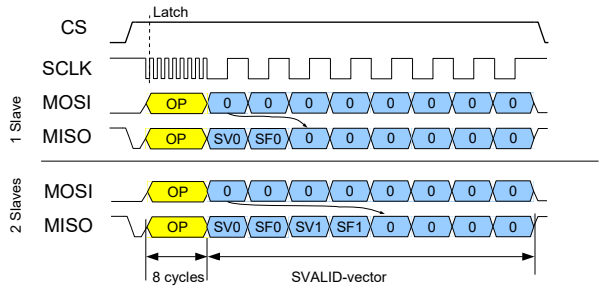

Figure 9: SDAD status (Example with one and two slaves (daisy chain))

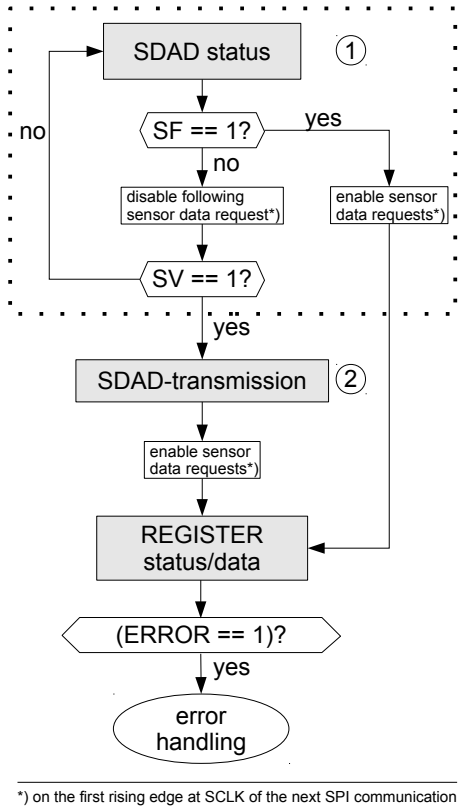

Figure 10: Example sequence of the commands SDAD Status/SDAD-transmission

Figure 10 shows the interaction of the two commands **SDAD Status** and **SDAD transmission**. The position data communication starts with the command **SDAD Status** (1). The first **SDAD Status** requests new data. If SFAIL is not set, subsequent **SDAD Status** commands are used to check for the data to be ready to transmit (no new position data requests are issued).

If SFAIL is set, requesting new position data on the first rising edge of SCLK of the next SPI communication is enabled. If the position data is ready as indicated by SVALID, the **SDAD-transmission** (2) command can be executed to read out the position data. Following this, the command **REGISTER status/data** should be executed to detect an unsuccessful SPI communication.

Register Read
The Register Read command (0x8A) reads data from a contiguous block of one or more RAM addresses starting at a specified address.

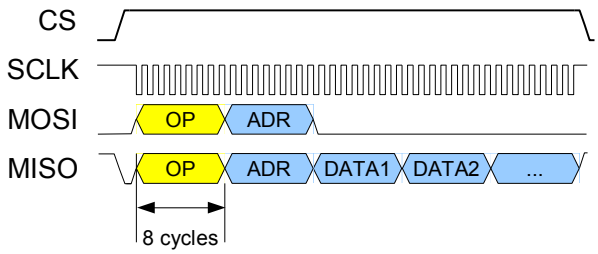

Figure 11: Register Read

The master transmits the read register opcode (0x8A) followed by the starting address of the block of addresses to read (ADR) on MOSI. The iC-LNB immediately outputs the opcode and address on MISO followed by the data from the register at address ADR (DATA1). As long as CS stays active (high), data from the the next register (address ADR + 1) is then output (DATA2). Data from subsequent registers continues to be output as long as CS remains high.

The register data channel must be activated (RA = 1) for proper operation of this command, otherwise the Error bit in the SPI Status byte is set. If an error occurs during a register read (invalid address, invalid data, etc.), the Fail bit in the SPI Status byte is set, the address counter is no longer incremented, and the data returned is invalid. See Table 15 on page 24 for more information.

Register Write
The Register Write command (0xCF) writes data to a contiguous block of one or more RAM addresses starting at a specified address.

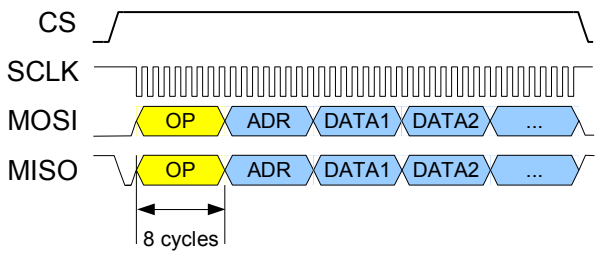

Figure 12: Write to REGISTER (cont.)

The master transmits the write register opcode (0xCF) followed by the starting address of the block of addresses to write (ADR), followed by the data to write to the register at address ADR (DATA1), the data to write to the address at ADR + 1 (DATA2), etc. on MOSI. The iC-LNB immediately outputs the MOSI bits on MISO. Data continues to be written to subsequent registers as long as CS stays active (high).

The register data channel must be activated (RA = 1) for proper operation of this command, otherwise the Error bit in the SPI Status byte is set. If an error occurs during a register write (invalid address, invalid data, etc.), the Fail bit in the SPI Status byte is set, the address counter is no longer incremented, and the data is not written. See Table 15 on page 24 for more information.

Register Status
The Register Status command (0xAD) returns the SPI Status byte which indicates the status of the last register transaction or data transmission.

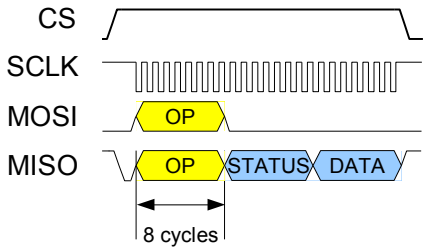

Figure 13: Register Status

As shown in Figure 13, the SPI Status byte is returned immediately following the Register Status opcode (STATUS) and is followed by an undefined data byte (DATA).

Table 15 shows the SPI Status byte bits.

STATUS		
Bit	Name	Description
7	Error	Invalid opcode
6:4	–	Reserved
3	Dismiss	Illegal Address
2	Fail	Data request failed
1	Busy	Slave busy
0	Valid	Position data valid

Table 15: SPI Status Byte

Status bits are updated with every register access, except Error, which indicates the status of the *last* command (opcode).

Bussing and Chaining Multiple iC-LNBs

Multiple iC-LNBs can be bussed or chained to a single SPI master. Figure 14 shows two iC-LNBs in a bussed configuration.

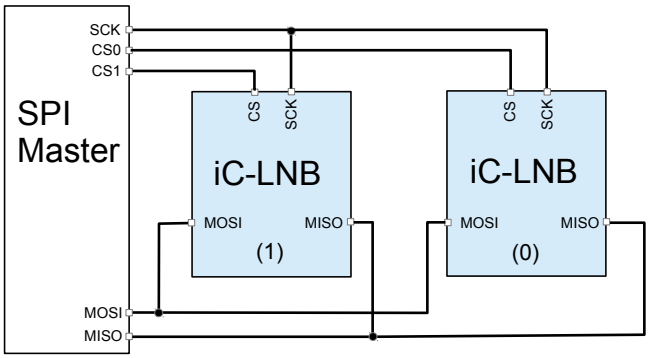

Figure 14: Bussing Multiple iC-LNBs

In this configuration, the SPI master communicates with each iC-LNB individually by activating the appropriate chip select (CS) output.

Figure 15 shows two iC-LNBs in a chained configuration.

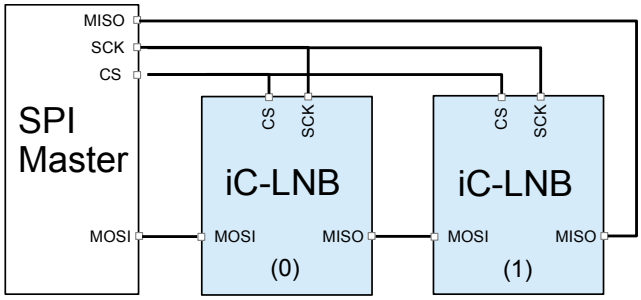

Figure 15: Chaining Multiple iC-LNBs

In this configuration, the MISO output of each iC-LNB is chained to the MOSI input of the next device in the chain. The SPI master must activate the desired channel(s) in a specific slave device to communicate with it.

The required RA and PA bits for each slave are packed into the bytes following the Activate opcode, as shown in Figure 16.

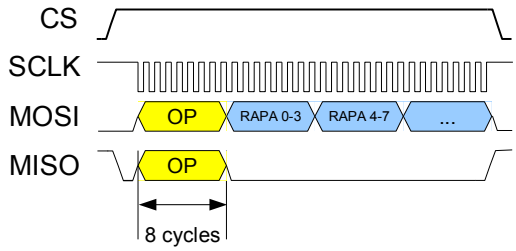

Figure 16: Activate Command For Multiple Slaves

For example, Figure 17 shows MOSI and MISO for an Activate command for one and two chained slaves.

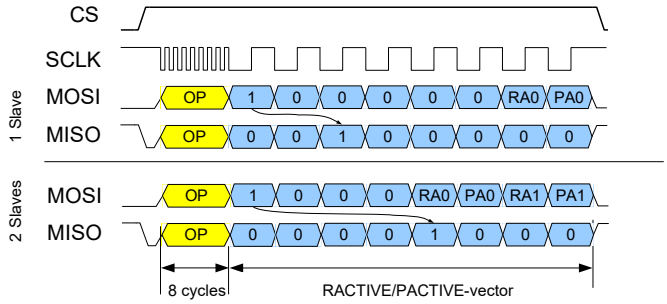

Figure 17: Activate Command For Two Slaves

Each slave outputs two zeros on MISO followed by the six most significant bits of MOSI and reads its RA and PA bits from bits 1 and 0 respectively of the RA/PA vector on MOSI. In this way, the RA/PA bits for the next slave in the chain are moved into bits 1 and 0 for the next slave.

The SPI master can determine the number of data channels in the chain by sending a 1 as bit 7 after the opcode in the Activate command. It then counts the number of zeros it receives on MISO before receiving the 1 back. The number of zeroes preceding the returned 1 is the number of data channels in the chain.

SIGNAL CONDITIONING

The iC-LNB provides seven parameters for conditioning and calibrating the signals from the sine and cosine photodiodes. These allow the elimination of offsets and the calibration and equalization of gain between the two channels. The sin/cos signal path and the adjustment parameters are shown in Figure 18.

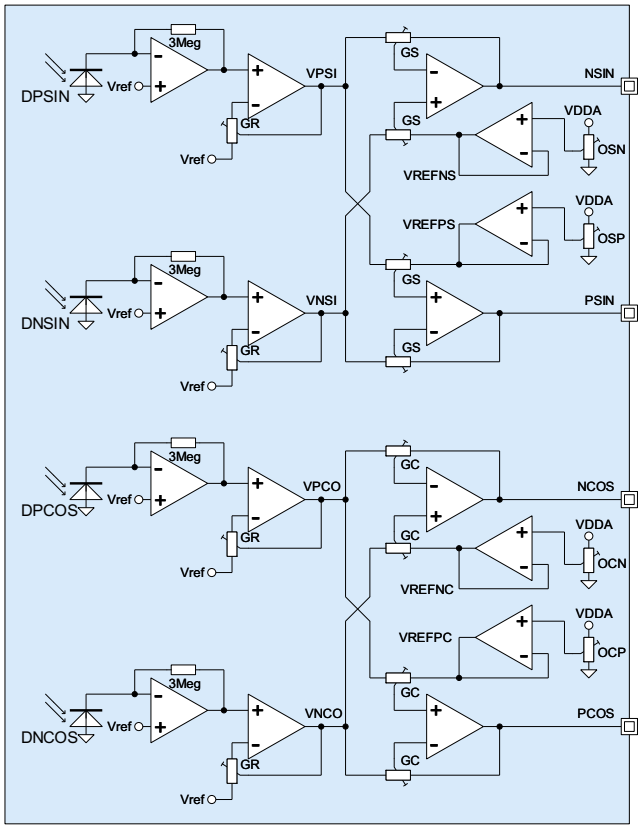

Figure 18: Sin/Cos Signal Path

Test modes (see TEST FUNCTIONS on page 41) allow observing many of the internal signals of the sin/cos signal path on the NSIN, PSIN, NCOS, and PCOS outputs to assist in calibration.

Gain Range (GR)

The gain range for the analog sin/cos signal path is set using parameter GR (0x07 bits 1:0).

GR	Address 0x07; bits 1:0
Value	Gain Factor
0	1.0
1	1.33
2	1.6
3	2.0

Table 16: Gain Range for Sin/Cos Signal Path

A gain range of 1.33 (GR = 1) is recommended for most applications.

Sine Gain (GS) and Offsets (OSP and OSN)

To calibrate the sine channel gain and offsets, the LED power control must be set to sum control (LCTYP = 1). In addition, the internal sine channel calibration signals must be made available on the analog outputs as shown in Figure 19 by setting TA = 0x1 and TMUX = 0x0D.

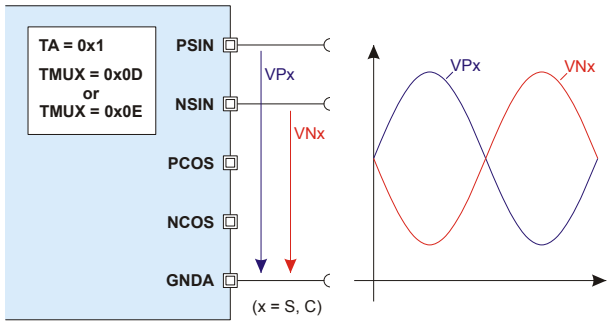

Figure 19: Gain and Offset Calibration

To start, set the sine and cosine amplitude (GS and GC) and offset parameters (OSP, OSN, OCP, and OSN) to their nominal values of 0xA0 and 0xC0 respectively (see Table 8). Adjust the optical power of the LED using parameter LCSET (0x06 bits 5:0) to set the sine channel amplitudes (VPS and VNS) as close to 500 mV as possible. Trim the sine channel amplitudes to 500 mV using parameter GS (0x00 bits 5:0).

GS	Address 0x00; bits 5:0
Value	Gain
0x00	1.0
0x01	1.01
...	$\frac{1+GS\cdot 0.0053}{1-GS\cdot 0.0053}$
0x3F	2.0

Table 17: Sine Channel Gain

Next, calibrate the offset of VPS and VNS such that the zero level (average) of VPS is equal to VNS, using parameters OSP (0x02 bits 6:0) and OSN (0x03 bits 6:0), respectively. When properly adjusted, the difference between the average DC voltage of VPS and VNS should be zero.

OSP	Address 0x02; bits 6:0
Value	Offset Value
0x00	0.475 · *VDDA*
0x01	0.4754 · *VDDA*
...	$(0.475 + \frac{OSP \cdot 0.05}{127}) \cdot VDDA$
0x7F	0.525 · *VDDA*

Table 18: Positive Sine (PSIN) Offset

OSN	Address 0x03; bits 6:0
Value	Offset Value
0x00	0.475 · *VDDA*
0x01	0.4754 · *VDDA*
...	$(0.475 + \frac{OSP \cdot 0.05}{127}) \cdot VDDA$
0x7F	0.525 · *VDDA*

Table 19: Negative Sine (NSIN) Offset

Cosine Gain (GC) and Offsets (OCP and OCN)
Calibration of the cosine channel gain and offsets is the same as for the sine channel, except that parameter TMUX must be set to 0x0E instead of 0x0D. This makes the internal cosine channel calibration signals available on the analog outputs as shown in Figure 19.

First, trim the cosine channel amplitudes (VPC and VNC) to 500 mV using parameter GC (0x01 bits 5:0).

GC	Address 0x01; bits 5:0
Value	Gain
0x00	1.0
0x01	1.01
...	$\frac{1+GC \cdot 0.0053}{1-GC \cdot 0.0053}$
0x3F	2.0

Table 20: Cosine Channel Gain

Next, calibrate the offset of VPC and VNC such that the zero level (average) of VPC is equal to VNC using parameters OCP (0x04 bits 6:0) and/or OCN (0x05 bits 6:0), respectively. When properly adjusted, the difference between the average DC voltage of VPC and VNC should be zero.

OCP	Address 0x04; bits 6:0
Value	Offset Value
0x00	0.475 · *VDDA*
0x01	0.4754 · *VDDA*
...	$(0.475 + \frac{OSP \cdot 0.05}{127}) \cdot VDDA$
0x7F	0.525 · *VDDA*

Table 21: Positive Cosine (PCOS) Offset

OCN	Address 0x05; bits 6:0
Value	Offset Value
0x00	0.475 · *VDDA*
0x01	0.4754 · *VDDA*
...	$(0.475 + \frac{OSP \cdot 0.05}{127}) \cdot VDDA$
0x7F	0.525 · *VDDA*

Table 22: Negative Cosine (NCOS) Offset

After all seven parameters (three gain and four offset) have been calibrated, return the iC-LNB to normal operation by turning off test mode (TA = 0x0).

LED Power Control
After calibration, it is recommended to enable the square control function of the LED power control by setting LCTYP = 0. This keeps the optical power received by the sine/cosine sensors constant regardless of changes in temperature and LED aging effects. After changing to square control, disable the deadband control by setting LCMOD = 0 and then use parameter LCSET (0x06 bits 5:0) to adjust the sine/cosine amplitudes to 500mV. After adjustment, it is recommended to enable the deadband control by setting LCMOD = 1. See LED POWER CONTROL on page 39 for more information.

INTERPOLATOR

Interpolator Resolution

The resolution of the internal interpolator determines the resolution of the iC-LNB; it is set using parameter RESIPO (0x0E bits 6:5). The interpolator resolution also determines the maximum speed (sin/cos input frequency) as shown in Table 23.

RESIPO	Address 0x0E; bits 6:5		
Value	Interpolator Resolution	iC-LNB Resolution	Max. Speed
00	8 bit	18 bit	3300 rpm
01	7 bit	17 bit	6600 rpm
10	6 bit	16 bit	13200 rpm
11	5 bit	15 bit	14500 rpm

Table 23: Interpolator Resolution

The maximum speeds shown in Table 23 are for a nominal interpolator oscillator frequency of 19.0 MHz (OSCZ = 10).

The interpolator must be enabled (ENIPO = 1) for normal operation of the iC-LNB, but must be disabled (ENIPO = 0) when setting or changing its resolution. After setting ENIPO = 1, the interpolator needs the startup time tst_{IPO} to reach the current position. The startup time depends on the interpolator resolution and the speed at enabling, see spec. item 708.

ENIPO	Address 0x11; bit 4
Value	Description
0	Interpolator Disabled
1	Interpolator Enabled

Table 24: Interpolator Enable

When disabled, the interpolator output is zero.

Interpolator Hysteresis

The hysteresis window of the interpolator is set using parameter HYS.

HYS	Address 0x0A; bits 2:0			
Value	Hysteresis with RESIPO =			
	00 (8 bit)	01 (7 bit)	10 (6 bit)	11 (5 bit)
0x00	+/- 0.7°	+/- 1.4°	+/- 1.4°	+/- 1.4°
0x01	+/- 2.1°	+/- 1.4°	+/- 1.4°	+/- 1.4°
0x02	+/- 3.5°	+/- 2.8°	+/- 1.4°	+/- 1.4°
0x03	+/- 4.9°	+/- 4.1°	+/- 2.8°	+/- 1.4°
0x04	+/- 6.3°	+/- 5.6°	+/- 4.1°	+/- 1.4°
0x05	+/- 7.7°	+/- 7.0°	+/- 5.6°	+/- 2.8°
0x06	+/- 9.1°	+/- 8.4°	+/- 7.0°	+/- 4.1°
0x07	+/- 10.5°	+/- 9.8°	+/- 8.4°	+/- 5.6°
Note	The recommended values are printed in black			

Table 25: Hysteresis Depending On Interpolator Resolution

Interpolator Filter

A low-pass filter is available to reduce noise on the interpolator inputs. This filter is enabled by parameter NENF.

NENF	Address 0x07; bit 6
Value	Description
0	Filter Enabled (recommended)
1	Filter Disabled

Table 26: Interpolator Filter

It is recommended to always use the input filter; it has been designed so that it can be used across the entire speed range.

FLEXCOUNT®

FlexCount® allows the resolution of the incremental, serial, and parallel outputs, as well as the SPI position to be programmed to any value less than the maximum resolution. FlexCount operates in real time and does not introduce any significant latency into the signal path.

Enable/Disable

FlexCount is enabled or disabled using parameter NENFLEX.

NENFLEX	Address 0x0B; bit 1
Value	Description
0	FlexCount Enabled
1	FlexCount Disabled

Table 27: FlexCount Disable

Incremental FlexCount Output

To use FlexCount for the incremental (ABZ) outputs, parameter INC must be set to INC = 0x07. See INCREMENTAL (ABZ) OUTPUTS on page 33 for more information.

Absolute FlexCount Output

FlexCount can also be used for the absolute serial (shift register), parallel, and SPI outputs of the iC-LNB as determined by parameter SELABS.

SELABS	Address 0x0B; bit 2
Value	Absolute Output Resolution
0	FlexCount Resolution
1	Maximum Resolution

Table 28: Absolute Output Resolution

FlexCount provides Gray code absolute outputs for all resolutions, however the position data output also allows binary absolute output.

If FlexCount is *not* used for the absolute outputs (SELABS = 1), the resolution of the absolute outputs is the maximum iC-LNB resolution, as determined by the selected interpolator resolution (RESIPO), as shown in Table 29.

Note that with SELABS = 1 the status POSOK is set to 1 if the interpolator position is valid and with SELABS = 0 the status POSOK is set to 1 if the FlexCount position is valid.

RESIPO	Address 0x0E; bits 6:5
Value	Maximum Resolution (Counts per Revolution)
3	15 bits (32 768)
2	16 bits (65 536)
1	17 bits (131 072)
0	18 bits (262 144)

Table 29: Maximum Absolute Output Resolution

Resolution

Parameter RESSUB determines the FlexCount resolution in incremental edges (ABZ outputs) or absolute counts (serial, parallel, and SPI outputs) per revolution.

RESSUB	Addresses 0x0F, 0x10, and 0x11 bits 3:0	
Value	Resolution (edges or counts per revolution)	
0x3	4	
0x7	8	
...	...	
0x07FFF	32 768	
0x08003	32 772	
...	...	(only with 6, 7 or 8 bit interpolation)
0x0FFFF	65 536	
0x10003	65 540	
...	...	(only with 7 or 8 bit interpolation)
0x1FFFF	131 072	
0x20003	131 076	
...	...	(only with 8 bit interpolation)
0x3FFFF	262 144	

Table 30: FlexCount Resolution

As shown in Table 30, RESSUB is equal to the desired resolution minus 1. For example, if an output resolution of 10 000 edges per revolution for the ABZ outputs is desired, set RESSUB = 0x0270F (10 000 – 1 = 9999 = 0x0270F).

FlexCount resolution must be evenly divisible by four. In addition, maximum FlexCount resolution is limited by the selected interpolator resolution (RESIPO) as shown in Table 31.

RESIPO	Address 0x0E; bits 6:5
Value	Maximum RESSUB Value
3	0x07FFF
2	0x0FFFF
1	0x1FFFF
0	0x3FFFF

Table 31: Maximum FlexCount Resolution

RESSUB is an 18-bit value spread across three registers in the iC-LNB register map, as shown in Table 32.

RESSUB	Registers
Bits	Address
17:14	0x11 bits 3:0
13:7	0x10 bits 6:0
6:0	0x0F bits 6:0

Table 32: RESSUB Addresses

Position offset
iC-LNB's FlexCount allows a programmable position offset to be specified. This offset can be set as a binary value of the maximum internal resolution (which is dependent on interpolator resolution RESIPO) using parameter ZPOS (not in the selected FlexCount resolution). All values from 0 to 262,143 can be selected when using 8 bit interpolator resolution; with 7 bit resolution, the LSB must be 0; with 6 bit resolution, the last two LSBs must be 0, and with 5 bit resolution, the last three LSBs must be 0.

ZPOS	Addresses 0x0C, 0x0D, 0x0E bits 3:0
Value	Position offset (binary)
0x00000	0 (any interpolation)
0x00001	1 (only with 8 bit interpolation)
0x00002	2 (only with 7 or 8 bit interpolation)
0x00003	3 (only with 8 bit interpolation)
0x00004	4 (only with 6, 7 or 8 bit interpolation)
...	...
0x00008	8 (any interpolation)
...	...
0x3FFFF	262 143 (only with 8 bit interpolation)

Table 33: FlexCount Position Offset

Absolute Position Numeric Formats
With binary FlexCount resolutions (those where RESSUB + 1 is an integer power of two), the Gray code absolute position is a number between 0 and RESSUB. Contiguous Gray code values differ by only one bit. Gray code 0 is coincident with the zero position of the encoder disc (falling edge of GA with DIR = 0).

With non-binary resolutions (those where RESSUB + 1 is not an integer power of 2), however, the full n-bit Gray code cannot be used. In these cases, to preserve the Gray code characteristic of a one bit change between contiguous values, only RESSUB+1 number of bits from the center of the full n-bit Gray code are used. This means that the Gray code absolute position is a value between two non-zero numbers.

For example, with a binary FlexCount resolution of 128 (RESSUB = 0x0007F), the Gray code absolute position is a value between 0 (0g0000) and 127 (0g0100'0000) inclusive. However, for the non-binary resolution of 100 (RESSUB = 0x00063), the Gray code absolute position is a value between 14 (0g0000'1001) and 113 (0g0100'1001) inclusive.

The lowest Gray code value (14 in this case) is called the *excess* and is the value by which the Gray code value exceeds the actual absolute position. To determine the true absolute position (a value between 0 and 99 for a FlexCount resolution of 100 as in the example above), the excess must be subtracted from each converted Gray code value.

For example, if the absolute position returned by the iC-LNB is 0g0010'0111, the true absolute position is calculated as 58 – 14 = 44 because 0g0010'0111 = 0b0011'1010 = 0x3A = 58).

With non-binary resolutions, the excess is calculated as

$$Excess = \frac{2^N - (RESSUB + 1)}{2}$$

In the above equation, N is the number of bits necessary to represent RESSUB. For example, with a FlexCount resolution of 100, N = 7 since 7 bits are required to represent 0x63. For any FlexCount resolution, N is calculated as

$$N = INT(log_2(RESSUB) + 1)$$

With non-binary FlexCount resolutions, a Gray code value equal to the excess is coincident with the zero position of the encoder disc (falling edge of GA with DIR = 0).

Changing FlexCount Resolution, Offset, or Direction
FlexCount must be stopped before the resolution (RESSUB), offset (ZPOS), or direction of rotation are changed (pin DIR or parameter DIR). This is done using parameter STOPFLEX, which stops FlexCount.

STOPFLEX	Address 0x11; bit 5
Value	Description
0	FlexCount active (normal operation)
1	FlexCount Stopped

Table 34: FlexCount Reset

After changing the FlexCount resolution, offset, or direction, activate FlexCount again by setting STOPFLEX = 0. This resets and re-enables FlexCount, causing the incremental (ABZ) and absolute (if SELABS = 0) outputs to count to the current absolute position. During this period, the outputs are not valid and POSOK = 0. POSOK is set to 1 when the position outputs are again valid.

POSOK	Address 0x12; bit 0
Value	Description
0	Position Invalid
1	Position Valid

Table 35: Position Valid

As shown in Figure 4, it is recommended to implement a timeout when checking for POSOK. This timeout must be larger than the startup time tst_{Flex} (see spec. item 804) of the FlexCount. This avoids a potential infinite loop that could happen due to glitches or communication errors. If POSOK is still 0 after some number of timeouts (typically 5), a configuration error can be assumed.

Additionally, the incremental (ABZ) outputs can be set low (NOUTLO = 0 and TRIABZ = 0) or the incremental outputs can be set to tristate (TRIABZ = 1) to avoid invalid outputs when changing the FlexCount resolution, offset or direction. After the outputs are at the current absolute position (POSOK = 1), enable the FlexCount outputs (NOUTLO = 1 and TRIABZ = 0).

NOUTLO	Address 0x11; bit 6
Value	FlexCount Outputs
0	Low
1	Normal Operation

Table 36: FlexCount Outputs

See INCREMENTAL OUTPUTS on page 33 for more information on TRIABZ.

OPERATING MODE

The iC-LNB has two operating modes which are selected using configuration bit EPG.

EPG	Address 0x07, bit 4
Value	Description
0	Interface Mode
1	Parallel Mode

Table 37: Operating Mode

Interface Mode

In interface mode, the shift register is used for absolute position output and the quadrature outputs (INCA and INCB) are used for incremental position output. If FlexCount is enabled (NENFLEX = 0), the incremental resolution is programmable and an index signal (INCZ) is also available. Also with FlexCount active, the absolute resolution can be the same as the incremental resolution or the maximum as determined by RESSUB. See FLEXCOUNT® on page 29 for more information.

Regardless of the FlexCount resolution, two Gray code outputs GA and GB are available. These represent the MSB and MSB – 1 (respectively) of the iC-LNB absolute position and are provided for use by an external turns (revolution) counter. See GRAY CODE OUTPUTS on page 36 for more information.

Also in interface mode, an output (XJD) is provided to aid in minimizing the mechanical tilt angle of the iC-LNB relative to the code disc. See ADJUSTMENT on page 38 for more information.

A power-on output at pin POK indicates whether or not the iC-LNB is ready.

Parallel Mode

In parallel mode, the absolute position output is a 16-bit parallel data word in Gray code. In this mode, all I/O pins are configured as outputs and the shift register output, incremental outputs, Gray code outputs, XJD, and POK outputs cannot be used. See PARALLEL MODE on page 37 for more information.

The SPI interface can also be used for position data readout and is available in both operating modes. Table 38 shows the pin functions for each operating mode. Pins not shown in Table 38 are not affected by the choice of operating mode.

Pad	**Interface Mode**	**Parallel Mode**
TNC	Test Input NCOS	Parallel Output Bit 15
TNS	Test Input NSIN	Parallel Output Bit 14
DIR	Code Inversion Input	Parallel Output Bit 13
NSL	Shift Register Load Input	Parallel Output Bit 12
DIN	Shift Register Data Input	Parallel Output Bit 11
DOUT	Shift Register Data Output	Parallel Output Bit 10
CLK	Shift Register Clock Input	Parallel Output Bit 9
GA	Gray-code Output A (MSB)	Parallel Output Bit 8
GB	Gray-code Output B (MSB-1)	Parallel Output Bit 7
XJD	Adjustment Signal	Parallel Output Bit 6
POK	Power OK Indication	Parallel Output Bit 5
INCZ	Incremental Output Z	Parallel Output Bit 4
INCB	Incremental Output B	Parallel Output Bit 3
INCA	Incremental Output A	Parallel Output Bit 2
TPS	Test Input PSIN	Parallel Output Bit 1
TPC	Test Input PCOS	Parallel Output Bit 0

Table 38: Pin Functions According to Operating Mode

INCREMENTAL (ABZ) OUTPUTS

ABZ Resolution

In interface mode (EPG = 0), the incremental outputs INCA and INCB can be set to use various interpolation factors or the FlexCount resolution. Selection is made using parameter INC.

INC	Address 0x08; bits 6:4
Value	Resolution
0x00	Interpolation Factor X1
0x01	Interpolation Factor X2
0x02	Interpolation Factor X4
0x03	Interpolation Factor X8
0x04	Interpolation Factor X16
0x05	iC-Haus digital test
0x06	iC-Haus test
0x07	FlexCount Resolution

Table 39: Incremental Output Resolution

If INC = 0x00 – 0x04, the resolution of the ABZ outputs is the selected interpolation factor times the resolution of the incremental track on the code disc. INC = 0x05 and 0x06 are used for special test modes as explained in TEST FUNCTIONS on page 41. If INC = 0x07, the ABZ resolution is the selected FlexCount resolution. See FLEXCOUNT® on page 29 for more information.

Note that a valid Z pulse on output INCZ is only available when FlexCount resolution is used (INC = 0x07).

Direction Reversal

If FlexCount is enabled (NENFLEX = 0 and SELABS = 0), the rotation direction of the incremental outputs can be reversed using parameter DIR or the DIR input.

DIR	Address 0x07; bit 5
Value	Description
0	CW (Normal Rotation)
1	CCW (Reversed Rotation)

Table 40: Direction Reversal

The DIR input and the DIR bit are XOR (exclusive OR) gated. This means that no direction reversal occurs if the DIR input is high and parameter DIR = 1.

FlexCount must be reset after changing the direction of rotation. See FLEXCOUNT® on page 29 for more information.

Incremental Output Inversion

If FlexCount is used (INC = 0x07), the incremental (ABZ) outputs can be inverted as required using register bits INVA, INVB, and INVZ. If FlexCount is not used (INC ≠ 0x07), these bits have no effect.

INVA	Address 0x0B; bit 6
Value	Incremental Output INCA
0	Normal
1	Inverted

Table 41: INCA Output Inversion

INVB	Address 0x0B, bit 5
Value	Incremental Output INCB
0	Normal
1	Inverted

Table 42: INCB Output Inversion

INVZ	Address 0x0B; bit 4
Value	Incremental Output INCZ
0	Normal
1	Inverted

Table 43: INCZ Output Inversion

Note that inverting INCA or INCB reverses the counting direction of the AB outputs. Inverting both INCA and INCB does not affect the AB counting direction.

INCZ Position

If FlexCount resolution is used (INC = 0x07), the position of the INCZ output (relative to zero absolute position) is programmable. The Z position is determined by parameter ZPOS, as shown in Table 44.

ZPOS	Addresses 0x0C, 0x0D, 0x0E bits 3:0
Value	Z Position (Edges Relative to Absolute Zero)
0x00000	0 (any interpolation)
0x00001	1 (only with 8 bit interpolation)
0x00002	2 (only with 7 or 8 bit interpolation)
0x00003	3 (only with 8 bit interpolation)
0x00004	4 (only with 6,7 or 8 bit interpolation)
...	...
0x00008	8 (any interpolation)
...	...
0x3FFFF	262 143 (only with 8 bit interpolation)

Table 44: INCZ Position

If ZPOS = 0x0000, the zero position is coincident with the falling edge of GA (iC-LNB MSB) as shown in Figure 20).

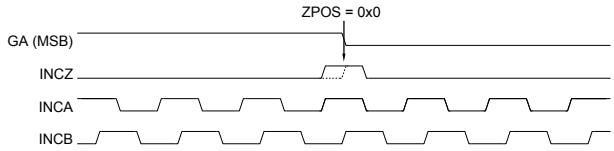

Figure 20: Zero position for ZPOS = 0x0

Acceptable ZPOS values are also affected by the interpolator resolution RESIPO, as shown in Table 45.

RESIPO	Address 0x0E; bits 6:5
Value	ZPOS Value
3	Evenly divisible by 8
2	Evenly divisible by 4
1	Evenly divisible by 2
0	any value

Table 45: Allowed ZPOS Value

ZPOS is an 18-bit value spread across three registers in the iC-LNB register map, as shown in Table 46.

ZPOS	Registers
Bits	Address
17:14	0x0E bits 3:0
13:7	0x0D bits 6:0
6:0	0x0C bits 6:0

Table 46: ZPOS Addresses

INCZ Width

If FlexCount resolution is used (INC = 0x07), the width of the INCZ output is also programmable. The Z width is determined by parameter Z90, as shown in Table 47.

Z90	Address 0x0E; bit 4	
Value	Index Width (AB Cycle)	Coincident With
0	180°	A high
1	90°	A and B high

Table 47: Z Pulse Width

The INCZ output coincidence shown in Table 47 is true if ZPOS = 0x00000 and INVA = INVB = INVZ = 0. Other ZPOS values cause the INCZ output to be coincident with other AB states. Depending on the value of ZPOS, it may be necessary to invert INCA, INCB, or both to achieve the desired coincidence.

Tristate

The incremental outputs INCA, INCB, and INCZ can be put into a high-impedance state (tristate) using register bit TRIABZ.

TRIABZ	Address 0x0B; bit 3
Value	INCA, INCB, INCZ
0	Normal Operation
1	Tristate

Table 48: Incremental Outputs Tristate

This can be used to eliminate invalid transitions on the ABZ outputs when changing the FlexCount resolution or direction. After power-on TRIABZ = 1.

SHIFT REGISTER OUTPUT

In interface mode (EPG = 0), a shift register is used for absolute position output.

As shown in Figure 21, the current absolute position is latched into the shift register on the first falling edge on the shift register clock input (CLK) while the shift register load input (NSL) is high. Following this, the absolute position is clocked out on the shift register output (DOUT) on each rising edge of CLK, regardless of the level of NSL. Position is output in Gray code or binary, depending on parameter NGRAY, MSB first.

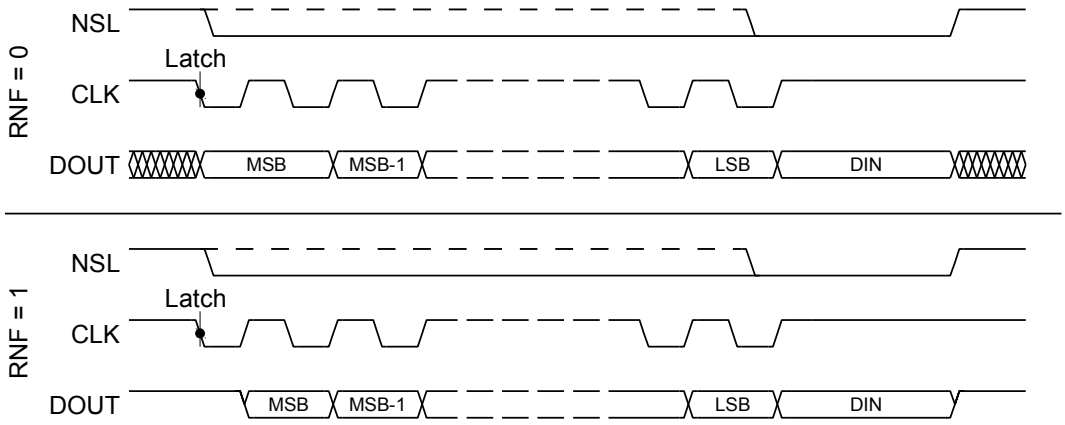

Figure 21: Shift register output

External data can be read into the iC-LNB through the shift register input (DIN). This data is clocked out following the position data, as shown in Figure 21.

The shift register output (DOUT) returns to its idle state (as specified by parameter RNF) on the rising edge of NSL. This means that the falling edge of NSL can occur any time during position transmission and is not critical.

Output Data Length

The length of the shift register and the number of position bits used are selected using parameter SRC, as shown in Table 49.

SRC	Address 0x08; bits 2:0	
Value	Shift Register Length	Number of Bits Used
0	18 bits	18
1	17 bits	17
2	16 bits	16
3	16 bits	15
4	16 bits	14
5	16 bits	13
6	14 bits	13
7	14 bits	12

Table 49: Shift Register Output Data Length

Position is always shifted out MSB first and left-justified. If the output data length is greater than the number of bits used (SRC $\geq$ 3), the unused LSBs are zero. For example, if SRC = 4, the shift register outputs the 14-bit position value followed by two zeros.

Output Data Format

Parameter NGRAY is used to select whether the shift register absolute position output is in Gray code or binary as shown in Table 50.

NGRAY	Address 0x07; bit 6
Value	Data Format
0	Gray Code
1	Binary

Table 50: Shift Register Output Data Format

If FlexCount is enabled (NENFLEX = 0 and SELABS = 0) and a non-binary resolution is used (RESSUB + 1 is not an integer power of 2), the absolute position is a value between two non-zero numbers regardless of the setting of NGRAY. See FLEXCOUNT® on page 29 for more information on the absolute position numeric formats.

Idle Output

Parameter RNF is used to select the idle output of the shift register output (DOUT) as shown in Table 51.

RNF	Address 0x08; bit 3
Value	Shift Register Output (DOUT)
0	Absolute Position MSB
1	High

Table 51: Shift Register Idle Output

If the position data is invalid (POSOK = 0), the output DOUT is set to low in idle state.

Direction Reversal

If FlexCount is enabled (NENFLEX = 0 and SELABS = 0), the absolute position direction can be reversed using parameter DIR or the DIR input. Both of these accomplish direction reversal by inverting the MSB of the Gray code absolute position.

DIR	Address 0x07; bit 5
Value	Description
0	CW (Normal Rotation)
1	CCW (Reversed Rotation)

Table 52: Direction Reversal

The DIR input and the DIR bit are XOR (exclusive OR) gated. This means that no direction reversal occurs if the DIR input is high and parameter DIR = 1. Direction reversal also works when binary output is selected (NGRAY = 1) as the conversion from Gray code to binary occurs after the MSB inversion.

FlexCount must be reset after changing the direction of rotation. See FLEXCOUNT® on page 29 for more information.

Shift Register Disable

The output shift register can be disabled using NENSHIFT.

NEN-SHIFT	Address 0x00; bit 6
Value	Description
0	Output shift register enabled
1	Output shift register disabled

Table 53: Shift Register Disable

GRAY CODE OUTPUTS

In interface mode (EPG = 0), outputs GA and GB provide two 90° shifted digital signals with 1 PPR each as shown in Figure 22. These signals can be used by an external revolution counter to implement multiturn capability.

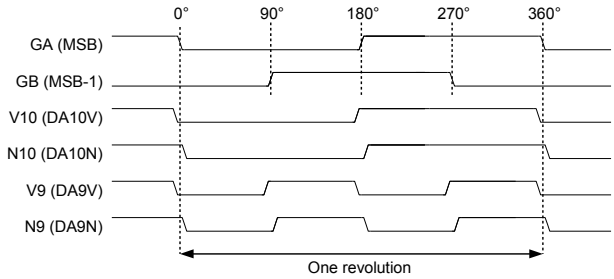

Figure 22: Outputs GA and GB

GA and GB are independent of the FlexCount resolution (RESSUB) or the zero position (ZPOS), and always occur at the positions shown in Figure 22 relative to the code disc.

The DIR input or parameter DIR (0x07 bit 5) can be used to invert the GA signal to reverse the rotation direction of the GA and GB outputs.

DIR	Address 0x07; bit 5
Value	Description
0	CW (Normal Rotation)
1	CCW (Reversed Rotation)

Table 54: Direction Reversal

The DIR input and the DIR bit are XOR (exclusive OR) gated. This means that no direction reversal occurs if the DIR input is high and parameter DIR = 1.

If FlexCount is enabled (NENFLEX = 0 and SELABS = 0), it must be reset after changing the direction of rotation. See FLEXCOUNT® on page 29 for more information.

PARALLEL OUTPUT MODE

Parallel output mode is provided as an alternative to the serial shift register output, incremental outputs, and the Gray code outputs. Parallel output mode is selected by setting EPG = 1.

EPG	Address 0x07, bit 4
Value	Description
0	Interface Mode
1	Parallel Output Mode

Table 55: Operating Mode

In parallel output mode, the absolute position output is a 16-bit parallel data word in Gray code. In this mode, all I/O pins are configured as outputs and the shift register output, incremental outputs, Gray code outputs, XJD, and POK outputs cannot be used.

The 16-bit parallel output can be the 10 bits from the digital tracks and 6 bits from the interpolator or the top 16 FlexCount bits depending on parameter SELABS. See FLEXCOUNT® on page 29 for more information on parameter SELABS and configuring FlexCount.

If FlexCount is enabled (NENFLEX = 0 and SELABS = 0) and a non-binary resolution is used (RESSUB + 1 is not an integer power of 2), the absolute position is a value between two non-zero numbers. See FLEXCOUNT® on page 29 for more information on the absolute position numeric formats.

It is recommended to set the interpolator resolution to 6 bits (RESIPO = 0x2) when using parallel output mode to allow the maximum input frequency, unless additional resolution is required by the SPI interface. See INTERPOLATOR on page 28 for more information on RESIPO and input frequency.

The DIR input or parameter DIR (0x07 bit 5) can be used to invert the MSB to reverse the rotation direction of the parallel output.

DIR	Address 0x07; bit 5
Value	Description
0	CW (Normal Rotation)
1	CCW (Reversed Rotation)

Table 56: Direction Reversal

The DIR input and the DIR bit are XOR (exclusive OR) gated. This means that no direction reversal occurs if the DIR input is high and parameter DIR = 1.

If FlexCount is enabled (NENFLEX = 0 and SELABS = 0), it must be reset after changing the direction of rotation. See FLEXCOUNT® on page 29 for more information.

ADJUSTMENTS

Tilt Angle

In interface mode (EPG = 0), a special output (XJD) is available to aid in adjusting the iC-LNB to minimize its tilt angle relative to the code disc for maximum accuracy.

XJD is the XORed signal from tracks DA4V and DA10V (the differential signal of the leading track 4 and track 10 diodes). As shown in Figure 23, adjust the tilt angle of the iC-LNB relative to the code disc to minimize the spike width, t, at 0° and 180°, as indicated by the edges of the GA output.

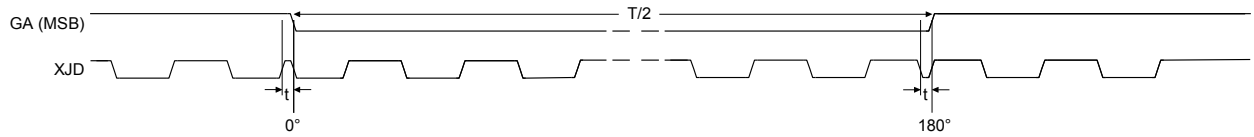

Figure 23: Using XJD to Minimize Tilt Angle

The maximum tilt angle that can be tolerated by the system is determined by the the diameter of the code disc and the chosen interpolator hysteresis (HYS), as shown in Table 57.

HYS(2:0)	LNB1S	LNB4S
0x00	1.8°	1.0°
0x01	1.75°	1.0°
0x02	1.7°	0.95°
0x03	1.7°	0.95°
0x04	1.65°	0.95°
...	...	...
0x07	1.6°	0.9°

Table 57: Maximum Tilt Angle (relative to chip center)

The scan ratio for the adjustment signal at XJD can be derived from the maximum tilt angle. For example, with the LNB1S 42-1024 at a tilt angle of 1.8°, photodiode DA4V is approximately 74 µm from its ideal position. With an average radius of 19.89 mm for track DA4, this results in an edge shift of 0.06%. The edge shift for photodiode DA10V is approximately the same size, but in the opposite direction. Therefore, the scan ratio is t/T = 0.12% for the maximum tilt angle of 1.8°. Minimizing this value minimizes the tilt angle and maximizes system accuracy.

The actual spike width, t, depends on the rotation speed of the code disc. Under optimum conditions, the maximum spike Width is

$$t\,[\mu s] = \frac{36\,000}{Speed\,[RPM]}$$

The min. spike width is 0 µs and can be regarded as an ideal value, but is difficult to achieve in practice. Due to imperfect light levels, code disc tolerances, etc. adjustment to a spike width between 0 µs and half of this maximum value is recommended. Ideally, both spikes should be the same width. For example, at 300 RPM, the spike width, t, should be less than 60 µs ($\frac{36000}{300} \cdot 0.5$).

Radial Position

The radial position of the iC-LNB relative to the code disc must be adjusted to center the tracks of the disc on the photodiodes of the iC-LNB. The error from ideal radial position must be less than 100 µm to avoid crosstalk between the absolute tracks, which can cause absolute position errors.

Radial position error also causes a phase error between the sine and cosine signals from the incremental track. This phase error can be measured and used to adjust the radial position of the iC-LNB relative to the code disc.

The phase error for a radial position error of 100 µm is shown in Table 58.

Code Disc	Phase Error
LNB1S 42-1024	0.65°
LNB4S 26-1024	1.6°

Table 58: Phase Error with 100 µm Radial Position Error

Adjust the radial position of the iC-LNB relative to the code disc to minimize the phase error between the sine and cosine signals.

LED POWER CONTROL

The optical power received by the sine/cosine sensors is kept constant by the integrated LED power control, regardless of changes in temperature and LED aging effects. The control mode is determined by parameter LCTYP, the options being sum control or square control. It is recommended to use square control during normal operation and sum control only for calibration.

LCTYP	Address 0x06; bit 6
Value	Control Type
0	Square Control ($\sin^2+\cos^2$)
1	Sum Control (DC sum)

Table 59: LED Power Control Type

The control setpoint is determined by parameter LCSET.

LCSET	Address 0x06; bits 5:0	
Value	Square Control LCTYP = 0	Sum Control LCTYP = 1
0x00	0.240 Vp	0.140 V
0x01	0.243 Vp	0.142 V
...	$\frac{0.24\ Vp}{1-LCSET \cdot 0.0125}$	$\frac{0.14\ V}{1-LCSET \cdot 0.0125}$
0x3F	1.1 Vp	0.640 V

Table 60: LED Power Control Setpoint

LCMOD determines whether or not deadband is used in the LED power control loop.

LCMOD	Address 0x01; bit 6
Value	Control Mode (LCTYP = 0 or 1)
0	Continuous Control
1	Deadband Control (approximately ± 5% of setpoint)

Table 61: LED Power Control Mode

In operation, if LCMOD = 0, the LED power control decreases the LED power whenever the LED voltage exceeds the setpoint (LCSET) and increases it whenever the LED voltage is less than the setpoint. If LCMOD = 1, the LED power is only changed when the LED voltage deviates from the setpoint by more than ≈ ± 5%.

The iC-LNB monitors the operation of the LED power control. If LED current exceeds the control range, ERRS in the status register (0x12 bit 1) is set to 1 and the ERR output is activated. See ALARM OUTPUT on page 39 for more information.

ALARM OUTPUT

The iC-LNB has an alarm or error output (ERR) to indicate errors. Under normal operation, ERR is low indicating that no errors are present.

ERR is driven high when the LED power control range is exceeded (ERRS = 1) or a parity error is detected in the RAM (ERRP = 1). ERRS and ERRP can also be read from the SPI status register, address 0x12 bits 1 and 2, respectively.

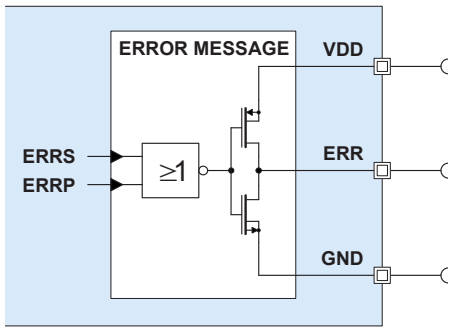

Figure 24: Alarm Output

OSCILLATOR

The iC-LNB has two internal oscillators, one each for the interpolator and FlexCount. The frequency of these oscillators can be trimmed using parameter OSZC.

The oscillator frequency also affects the maximum speed (sin/cos input frequency). See INTERPOLATOR on page 28 and spec. item 706 for more information.

OSZC	Address 0x07; bits 3:2	
Value	Typical Interpolator Oscillator Frequency	Typical FlexCount Oscillator Frequency
0	16.5 MHz	17.0 MHz
1	17.5 MHz	18.0 MHz
2	19.0 MHz	19.5 MHz
3	20.0 MHz	20.5 MHz

Table 62: Oscillator Adjustment

It is recommended to use OSZC = 2, the startup value, unless application conditions require otherwise.

TEST FUNCTIONS

Test functions are provided in the iC-LNB to allow observation of internal analog signals for calibration and adjustment. These internal signals replace the analog sine and cosine outputs when TA = 1.

TA	Address 0x09; bits 5:4
Value	Output at PSIN, NSIN, PCOS, NCOS
0	Normal operation
1	Test Mode
2	iC-Haus Test
3	iC-Haus Test

Table 63: Test Modes

In test mode (TA = 1), parameter TMUX determines which four internal signals are available on the analog sine and cosine outputs, as shown in Table 64.

TMUX	Address 0x09; bits 3:0			
Value	Pin PSIN	Pin NSIN	Pin PCOS	Pin NCOS
0x00	VPSI	VNSI	VPCI	VNCI
0x01	AVP1	Vref	AVN1	Vcomp
0x02	ANP1	Vref	ANN1	Vcomp
0x03	AN2	Vref	AV2	Vcomp
0x04	AN3	Vref	AV3	Vcomp
0x05	AN4	Vref	AV4	Vcomp
0x06	AN5	Vref	AV5	Vcomp
0x07	AN6	Vref	AV6	Vcomp
0x08	AN7	Vref	AV7	Vcomp
0x09	AN8	Vref	AV8	Vcomp
0x0A	AN9	Vref	AV9	Vcomp
0x0B	AN10	Vref	AV10	Vcomp
0x0C	VREFPS	VREFNS	VREFPC	VREFNC
0x0D	PSIN	NSIN	PCOS	SVDC
0x0E	PCOS	NCOS	PSIN	CVDC
0x0F, NENF = 1	IPQT	IPO	VREFO	BIASPO
0x0F, NENF = 0	PSF	NSF	PCF	NCF

Table 64: Test Signal Multiplexer for Analog Signals

See SIGNAL CONDITIONING on page 26 for information on using the test signals for device calibration.

A digital test mode is provided to allow observation of internal digital signals for test and diagnosis. These internal signals replace the incremental outputs when INC = 0x05, as shown in Table 65.

TMUX	Address 0x09; bits 3:0		
Code	Pin INCA	Pin INCB	Pin INCZ
0x00	NENOS	NLOCK	$f_{ipo}/4$
0x01	V1	N1	I7
0x02	V1	N1	I7
0x03	V2	N2	I7
0x04	V3	N3	I7
0x05	V4	N4	I7
0x06	V5	N5	I7
0x07	V6	N6	I7
0x08	V7	N7	I7
0x09	V8	N8	I7
0x0A	V9	N9	I7
0x0B	V10	N10	I7
0x0C	I6	I5	I7
0x0D	I4	I3	I7
0x0E	IPO_A	IPO_B	IPO_Z
0x0F	I2	I1	I7

Table 65: Test Signal Multiplexer for Digital Signals

DESIGN REVIEW: Notes On Chip Functions

iC-LNB V		
No.	Function, Parameter/Code	Description and Application Notes
		Refer to datasheet iC-LNB release B2, 2016.

Table 66: Notes on chip functions regarding iC-LNB chip release V

iC-LNB U2		
No.	Function, Parameter/Code	Description and Application Notes
		None at time of release.

Table 67: Notes on chip functions regarding iC-LNB chip release U2

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	13-06-21	Initial Release		

Rel.	Rel. Date*	Chapter	Modification	Page
B1	15-02-02	Electrical Characteristics	Item 102: changed name in "Max. Spectral Sensitivity" Added new item 103: spectral sensitivity of 850nm Item 703: angular hysteresis corrected Item F01, F02: corrected typ. and add. min/max valid for iC-LNB V	9, 10
		OPERATING REQUIREMENTS: SPI Interface	Updated Figure 2 SPI interface timing: definition of tcs Item I002: changed SCK hi → lo to SCK lo → hi	14
		SPI Interface	Notice box on MISO regarding idle state of pin MISO Description revised: Position data output format is always Gray code	21, 22
		Design Review	Added chip revision iC-LNB V Chip revision X and X1 removed	35
		Programming iC-LNB	Figure 4 enhanced with information regarding defensive programming	19

Rel.	Rel. Date*	Chapter	Modification	Page
B2	2016-06-17	ELECTRICAL CHARACTERISTICS	Item 707 added: propagation delay interpolator	10
		FLEXCOUNT®	Improved description and notes of table 30	29
		DESIGN REVIEW: Notes On Chip Functions	Removed notes of pre-series revision W1 Added note on chip revision V	42

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2018-03-27	all	Complete rework for chip revision iC-LNB U2 (For chip revision iC-LNB V please refer to datasheet release B2, 2016)	all

Rel.	Rel. Date*	Chapter	Modification	Page
D1	2020-10-08	DESCRIPTION	Note added	2
		PACKAGING INFORMATION	Added information of IC top marking for LNB2C package	4
		ABSOLUTE MAXIMUM RATINGS	Items G005, G010 changed	8
		ELECTRICAL CHARACTERISTICS	Items 702, 703, 706, 707, 802, 803, A13, A14, B13, B14 changed Items 708, 804 added	10 ff.
		OPERATING REQUIREMENTS	Symbol names changed	15 f.
		CONFIGURATION PARAMETERS	Parameter SRC changed	17
		CONFIGURING THE iC-LNB	Figure 4 changed	20
		SPI INTERFACE	Figure 17 changed	25
		SIGNAL CONDITIONING	Information on square control adjustment added	27
		INTERPOLATOR	Table 23 and Table 25 changed Startup time added	28
		FLEXCOUNT®	Note on POSOK added POSOK timeout changed	29 ff.
		SHIFT REGISTER OUTPUT	Note on idle output added	36
		ADJUSTMENTS	Note on ideal spike width added	38
		OSCILLATOR	Table 62 values corrected	40
		TEST FUNCTIONS	Table 64 changed: VTH→ Vref, VREF → Vcomp	41

* Release Date format: *YYYY-MM-DD*

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ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-LNB	30-pin optoBGA	standard reticle LNB1R standard reticle LNB4R customer specific reticle	iC-LNB oBGA LNB2C-1R iC-LNB oBGA LNB2C-4R iC-LNB oBGA LNB2C-xR
	38-pin optoQFN	standard reticle LNB1R standard reticle LNB4R customer specific reticle	iC-LNB oQFN38-7x5-1R iC-LNB oQFN38-7x5-4R iC-LNB oQFN38-7x5-xR
Standard Code Discs		Sin/Cos 1024 PPR, 10 bit digital OD/ID ∅42/18 mm, glass	LNB1S 42-1024
		Sin/Cos 1024 PPR, 10 bit digital OD/ID ∅26/9.6 mm, glass	LNB4S 26-1024

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