iC-HF

6-CH. ENCODER LINK, RS-422 DRIVER/RECEIVER

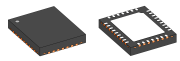
FEATURES

- Versatile 3+3 channel RS-422 line driver/receiver
- Pin configured as 6-ch. driver, or 3+3/4+2 ch. driver/receiver
- Pin configured as driver (6x) or driver/receiver (3x/3x or 4x/2x)
- Supports *BiSS bus structure* and *BiSS bus loopback*
- Unique *Encoder Link* mode: analog switches to bridge 9 lines
- Differential short-circuit-proof push-pull outputs
- Source/sink driving capability of 30 mA typ. at 3 V
- Reduced EMI due to output current limitation
- Output shutdown with undervoltage and overtemperature
- Suits various line impedances, allows 120 Ω termination
- TTL-compatible hysteresis inputs
- Up to 10 MHz input/output frequency
- Open-drain error message output (NERR)
- Reverse polarity protection
- Reverse pol. protection of periphery by supply switch (60 mA)
- Operation from 3.0 V to 5.5 V
- Operating temperature range of -40 °C to +125 °C
- Space-saving 32-pin QFN package

APPLICATIONS

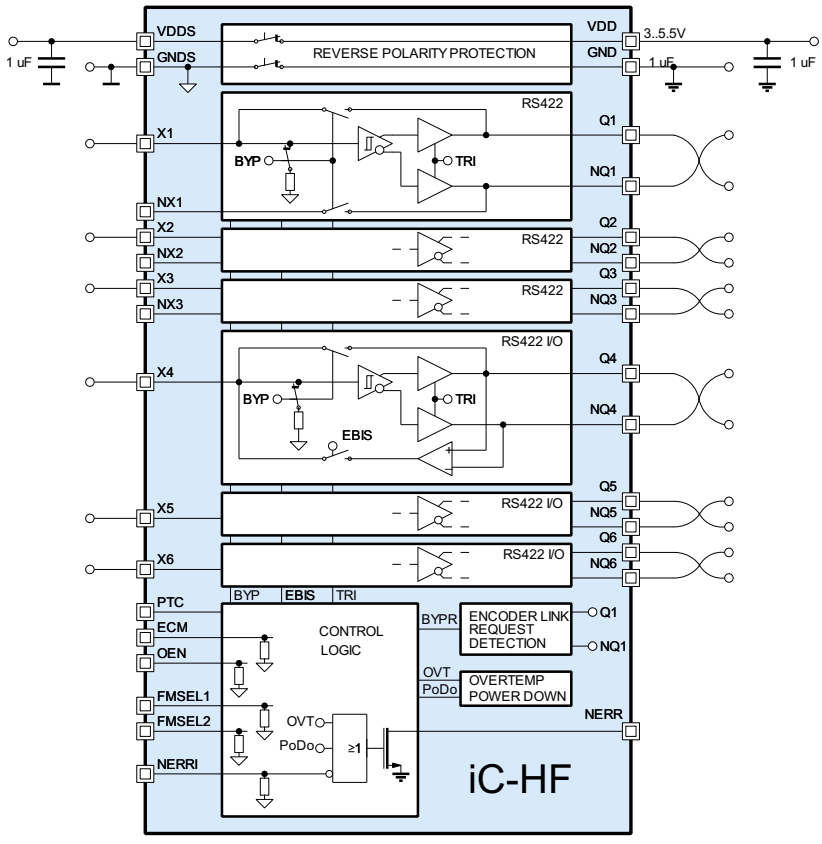
- Differential cable driver
- Motion control encoders
- Control engineering
- Microcontroller peripheries
- BiSS Interface bus structures

PACKAGES



32-pin QFN
5 mm x 5 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-HF is a robust line driver for industrial 5 V control applications featuring six differential output channels.

Single-ended, TTL-compatible input signals are transmitted as differential, 5 V RS-422 output signals at a rate up to 10 MHz. The push-pull driver stages typically provide 40 mA, present low saturation voltage, are current limited for reduced EMI emissions, and short-circuit-proof.

iC-HF is protected against reverse polarity connection, disabling internal supply voltage and setting output channels to high impedance when reverse polarity connection is detected. It offers a power-good switch, delivering up to 60 mA, that allows extended reverse polarity protection for connected sensors.

iC-HF supports *Encoder Link*. In this configuration input signals are directly linked to output pins. Analog signals from sensors can be accessed directly at output pins from iC-HF, allowing sensor calibration and alignment. Up to 9 channels can be configured as *Encoder Link*. Entering and exiting Encoder Link configuration requires no additional line.

BiSS/SSI communication is supported through RS-422 standard physical layer. iC-HF can also be included in a *BiSS bus structure*, and it can be configured as a bus termination node (*BiSS bus loopback*).

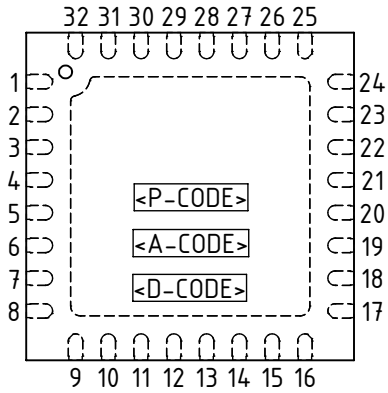
iC-HF protects against undervoltage and overtemperature events. Output channels are left in high impedance upon any of these events, and an error is signaled through the open drain output NERR. NERR is short-circuit protected.

Error signaling from sensor can be transferred via NERRI/NERR pins.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION QFN32-5x5 (topview)



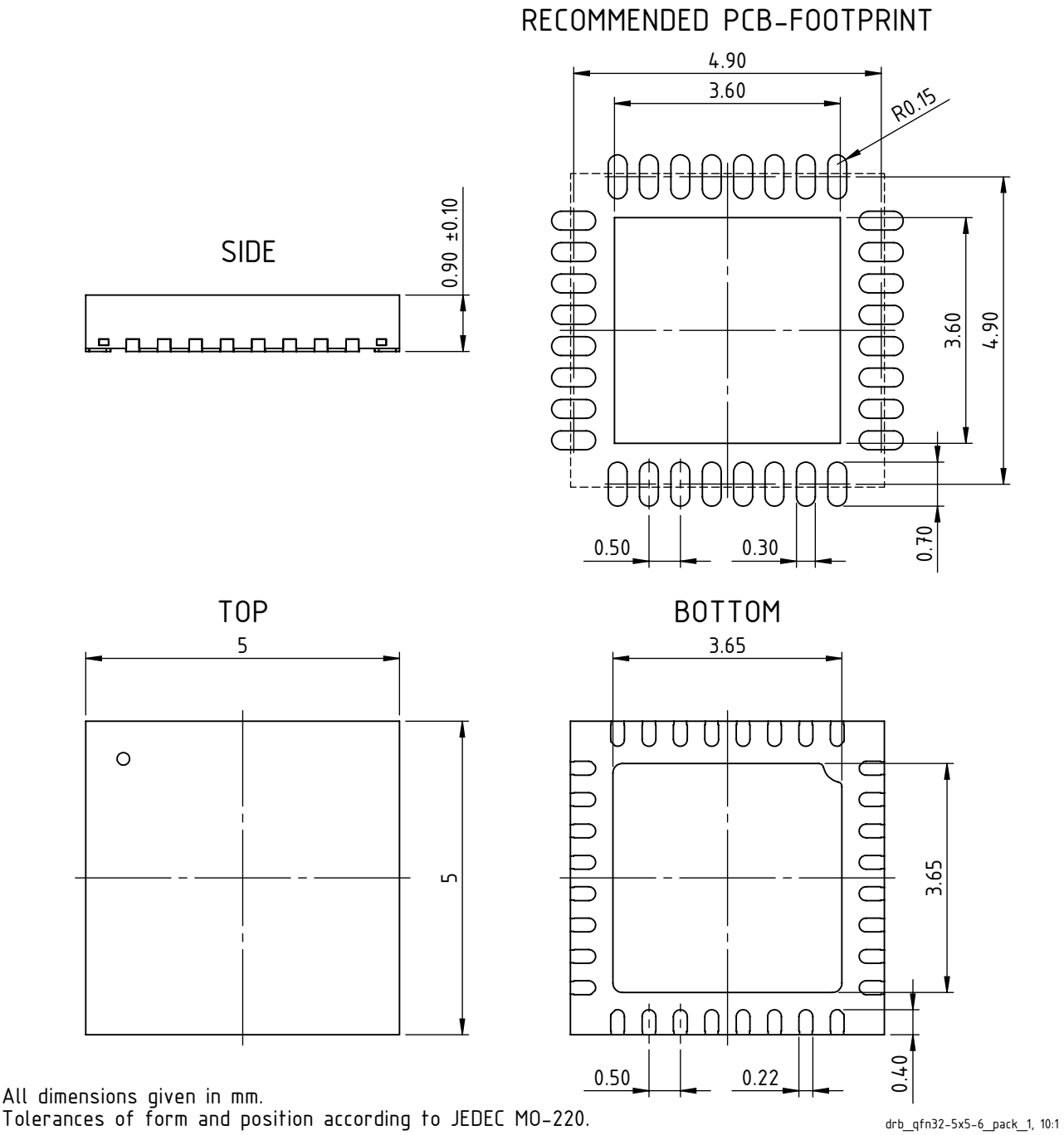
PIN FUNCTIONS

No.	Name	Function
1	X5	Channel 5 positive input
2	X4	Channel 4 positive input
3	X3	Channel 3 positive input
4	NX3	Channel 3 negative input
5	OEN	Output Enable input
6	X2	Channel 2 positive input
7	NX2	Channel 2 negative input
8	X1	Channel 1 positive input
9	NX1	Channel 1 negative input
10	Q1	Channel 1 positive output
11	NQ1	Channel 1 negative output
12	Q2	Channel 2 positive output
13	NQ2	Channel 2 negative output
14	Q3	Channel 3 positive output
15	NQ3	Channel 3 negative output
16	NERRI	Error Input (low active)
17	ECM	Enable *Encoder Link State* input
18	VDD	Power Supply Voltage
19	VDDS	Switched Power Supply output
20	GND	Ground
21	GNDS	Switched Ground output
22	FMSEL2	Function Mode Select 2 input
23	FMSEL1	Function Mode Select 1 input
24	PTC	PT configuration output
25	NERR	Error Output (low active)
26	NQ6	Channel 6 negative output
27	Q6	Channel 6 positive output
28	NQ5	Channel 5 negative output
29	Q5	Channel 5 positive output
30	NQ4	Channel 4 negative output
31	Q4	Channel 4 positive output
32	X6	Channel 6 positive input
BP		Backside Paddle (GNDS)

The pin directions input and output are related to default operation, not to Encoder Link State or operational mode.

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);
The *Backside Paddle* must be connected to GNDS.

PACKAGE DIMENSIONS



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

drb_qfn32-5x5-6_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V(VDD)	Voltage at VDD		-6	6	V
G002	I(VDD)	Current in VDD		-20	600	mA
G003	Vin	Voltage at NERR, X1 . . . X6, NX1 . . . NX6, PTC, ECM, NERRI, FMSEL1, FMSEL2, OEN, Q1...Q6, NQ1...NQ6, VDDS, GNDS		-0.3	VDD+0.3	V
G004	I(GND)	Current in GND		-600	20	mA
G005	I()	Current in VDDS, GNDS		-70	70	mA
G006	I()	Current in X1 . . . X6, NX1 . . . NX3, PTC, ECM, NERRI, FMSEL1, FMSEL2, OEN		-4	4	mA
G007	I()	Current in Q1 . . . Q6, NQ1 . . . NQ6		-60	60	mA
G008	I()	Current in NERR		0	30	mA
G009	Vd()	ESD Susceptibility at All Pins, Reference GNDS	HBM 100 pF discharged through 1.5kΩ		4	kV
G010	Tj	Junction Temperature		-40	150	°C
G011	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VDD = 3 . . . 5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C

All voltages are referenced to pin GND unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: Tj=-40 °C ... 125 °C, VDD = 3 ... 5.5 V, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	V(VDD)	Permissible Supply Voltage		3		5.5	V
002	I(VDD)	Supply Current	no load, VDD = 5.5 V no load, VDD = 3 V		1.6 1	2.5 1.8	mA mA
003	I(VDDS)	Permissible Load Current VDDS		-60		0	mA
004	I(GNDS)	Permissible Load Current GNDS		0		60	mA
005	Toff	Overtemperature Shutdown	Increasing temperature Tj	135		185	°C
006	V(VDD)on	Turn-On Threshold	Increasing VDD	2.1		2.9	V
007	V(VDD)off	Turn-off Threshold	Decreasing VDD	2.1		2.9	V
008	V(VDD)hys	Power-on Hysteresis			3		mV
009	Vcz()hi	Clamp Voltage hi at X1 ... X3, NX1 ... NX3, Q1 ... Q6, NQ1 ... NQ6, VDDS		7			V
010	Vc()hi	Clamp-Voltage hi at ECM, OEN, FMSEL1, FMSEL2, NERRI	Vc()hi = V() - V(VDD), I() = 0.2 mA	0.3		1.5	V
011	Vc()hi	Clamp-Voltage hi at Inputs X4 ... X6, PTC	Vc()hi = V() - V(VDD), I() = 1 mA	0.3		1.5	V
012	Vc()lo	Clamp Voltage lo at X1 ... X6, NX1 ... NX3, PTC, ECM, OEN, FMSEL1, FMSEL2, NERRI, NERR, Q1 ... Q6, NQ1 ... NQ6, VDDS	Vc()lo = V() - V(GNDS), I() = -1 mA,	-1.5		-0.3	V
Digital Inputs X1 ... X6, ECM, NERRI, OEN, FMSEL1, FMSEL2							
101	Vt()hi	Input Threshold Voltage hi	Channel as output driver			2	V
102	Vt()lo	Input Threshold Voltage lo	Channel as output driver	0.8			V
103	Vt()hys	Input Hysteresis	Channel as output driver	110	280		mV
104	Ipd()	Input Pull-Down Current	Channel as output driver V() = 0.4 V ... VDDS	4	60	220	µA
105	tdmax()	Maximum delay from Single-Ended Input to RS-422 output			30		ns
Digital Outputs X4, X5, X6							
201	Isc()lo	Output Short Circuit lo	Channel as RS-422 receiver V() = VDDS OEN = 1	8		100	mA
202	Isc()hi	Output Short Circuit hi	Channel as RS-422 receiver V() = GNDS OEN = 1	-100		-8	mA
203	Vs()lo	Output Saturation Voltage lo	Channel as RS-422 receiver I() = 3 mA Vs()= V() - V(GNDS) OEN = 1			400	mV
204	Vs()hi	Output Saturation Voltage hi	Channel as RS-422 receiver I() = -3 mA Vs()= VDDS - V() OEN = 1			400	mV
205	tr()	Rise Time	Channel as RS-422 receiver Cext = 50 pF OEN = 1			20	ns
206	tf()	Fall Time	Channel as RS-422 receiver Cext = 50 pF OEN = 1			20	ns

ELECTRICAL CHARACTERISTICS

Operating Conditions: Tj=-40 °C ... 125 °C, VDD = 3 ... 5.5 V, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Analog Inputs/Outputs							
301	Ron	ON Resistance at X1 ... X6, NX1 ... NX3	Channel in *Encoder Link State*		110	400	Ω
302	I(max)	Maximum Direct Current	Channel in *Encoder Link State*			1	mA
303	Ilk()	Leakage Current at X1 ... X6, NX1 ... NX3, Q1 ... Q6, NQ1 ... NQ6	Channel in *Encoder Link State*	-35	0	35	µA
304	f(COMM)	Communication Frequency at X1 ... X6, NX1 ... NX3	Channel in *Encoder Link State*			10	MHz
NERR Output							
401	INERR()	Current in NERR	V(NERR) < 0.5 V, error	4		25	mA
402	Vs()lo	Saturation Voltage lo	I(NERR) = 4mA			0.5	V
RS-422 Inputs Q4/NQ4 ... Q6/NQ6							
501	Ri	Input Resistance	Channel configuration as RS-422 Receiver Vi(Qx)= 0 ... 5.5 V Vi(NQx)= 0 V $Ri = \frac{5.5}{\Delta I Qx}$ OEN = 1	1			kΩ
502	Vi(Qx), Vi(NQx)	Input Voltage	Channel configuration as RS-422 Receiver OEN = 1	0		VDD	V
503	|Vid()|	Differential Input Voltage	Channel configuration as RS-422 Receiver $\|Vid()\| = \|Vip() - Vin()\|$ OEN = 1	0.05		VDD/2	V
504	Vic()	Common-Mode Input Voltage	Channel configuration as RS-422 Receiver $Vic() = \frac{Vip() - Vin()}{2}$ OEN = 1	0.8		VDD	V
505	Vid()hys	Differential Input Voltage Hysteresis	Channel configuration as RS-422 Receiver OEN = 1	0.5		8	mV
506	f(max)	Maximum Communication Frequency	Channel configuration as RS-422 Receiver OEN = 1, R Termination = 120 Ω, 50% Duty Cycle	10			MHz
507	tdmax()	Maximum delay from RS-422 input to Single-Ended Output			40		ns
Line Driver Outputs Q1/NQ1 ... Q6/NQ6							
601	Icex	Output Leakage Current	OEN = 0	-35	0	35	µA
602	Vs()hi	Saturation Voltage hi	Vs() = VDD - V(); I() = -20 mA OEN = 1			800	mV
603	Vs()lo	Saturation Voltage lo	Vs() = V(); I() = 30 mA OEN = 1			800	mV
604	Isc()lo	Short-Circuit Current lo at output driver	V() = V(VDD) OEN = 1	30		65	mA
605	Isc()hi	Short-Circuit Current Hi at output driver	V() = V(GND) OEN = 1	-45		-20	mA
606	f(max)	Maximum Output Frequency	Load = 120 Ω	10			MHz
607	tr()	Rise Time	RL = 120 Ω in-between Qx and NQx; VDD = 5.5 V VDD = 3 V			 15 20	 ns ns
608	tf()	Fall Time	RL = 120 Ω in-between Qx and NQx; VDD = 5.5 V VDD = 3 V			 15 20	 ns ns

ELECTRICAL CHARACTERISTICS

Operating Conditions: Tj=-40 °C ... 125 °C, VDD = 3 ... 5.5 V, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reverse Polarity Protection and Supply Switches VDDS, GNDS							
701	Vs()	Saturation Voltage VDD, Vs(VDDS) = VDD − V(VDDS)	I(VDDS) = -20 ... 0 mA I(VDDS) = -60 ... -20 mA			150 250	mV mV
702	Vs()	Saturation Voltage GND, Vs(GNDS) = V(GNDS) − GND	I(GNDS) = 0 ... 20 mA I(GNDS) = 20 ... 60 mA			150 250	mV mV
703	Irev(VDD)	Reverse-Polarity Current	V(VDD) = -5.5V ... -3 V	-1		0	mA
Encoder Link Sequence							
801	Vt()hi	Input Voltage Level hi at Q1, NQ1				80	%VDD
802	Vt()lo	Input Voltage Level lo at Q1, NQ1		20			%VDD
803	ts	Valid State Duration Time		49	50	52	µs
804	Δ ts	Max State Time Variation	ts = 50 µs	-500		200	ns
805	Ilk()	Leakage Current	voltage reversal	-1		1	µA
Configuration Output, pin PTC							
901	Vptc()	Configuration Output Voltage	*Encoder Link State* C_{PTC} = 10 nF optional	45	50	55	%VDDS
902	Ilk()	Leakage Current	no *Encoder Link State*	-10		10	µA

CHANNEL DESCRIPTION

iC-HF is a 6-channel RS-422 line driver.
There are two types of channels:

- unidirectional channel
- bidirectional channel

Unidirectional channel

Channels 1, 2 and 3 are unidirectional channels. These channels can work under unidirectional RS-422 driver configuration or under *Encoder Link State*.

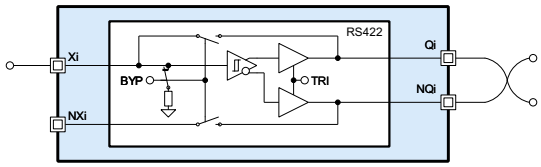


Figure 1: Unidirectional channel

When the channel works as unidirectional RS-422 driver, single ended input signals at Xi pins are converted into differential output signals at Qi/NQi outputs. Output signals follow RS-422 protocol. Differential output drivers are tristate drivers. OEN pin must be set hi to enable differential output signals, otherwise they will remain in high impedance state. More information on the internal signal TRI and the output drivers in high impedance can be found on page 17.

A pull-down resistor is present at the inputs, and incoming signals at Xi pins must be TTL-compatible. In unidirectional driver configuration, signals at NXi pins are disabled. The equivalent circuit can be found in Figure 2.

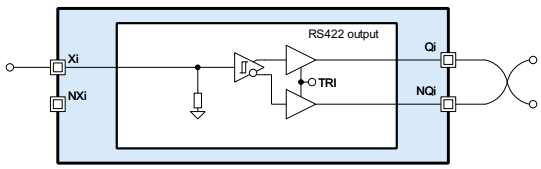


Figure 2: Equivalent circuit of unidirectional RS-422 driver channel

When the channel is in *Encoder Link State*, signals present at input pins Xi are bypassed and directly connected to output pins Qi. Signals at NXi are bypassed too to output pins NQi. Unidirectional channels in *Encoder Link State* present two bypassed lines.

The input stage and the input pull-down resistor and the output stage are disabled in *Encoder Link State*.

This configuration is useful for calibrating sensors. Analog signals from the sensor can be directly accessed from pins Qi/NQi. More information on the *Encoder Link State* on page 21.

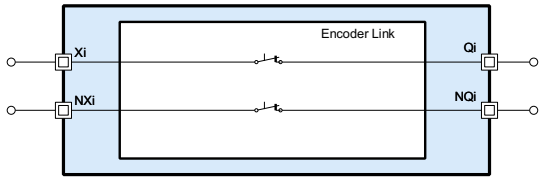


Figure 3: Equivalent circuit of 1 channel (2 lines) in *Encoder Link State*

Bidirectional channel

Channels 4, 5 and 6 are bidirectional channels. These channels can work under bidirectional RS-422 driver configuration or under *Encoder Link State*.

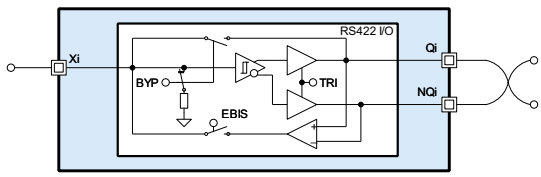


Figure 4: Bidirectional channel

When the channel is a bidirectional RS-422 driver, it can work as a transmitter or as a receiver. It cannot work simultaneously in both modes, each working mode corresponds to a specific configuration of the channel.

If the channel is a transmitter, single ended signals at input pins Xi are converted into differential output signals at Qi/NQi outputs. Outputs signals follow RS-422 protocol. A pull-down resistor is present at the inputs, and incoming signals at Xi pins must be TTL compatible. The equivalent circuit can be found in Figure 5. Similarly to unidirectional channels, OEN pin must be set hi to enable differential output signals, otherwise they will remain in high impedance state. More information on output drivers in high impedance can be found on page 17.

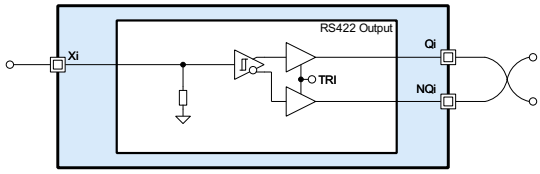


Figure 5: Equivalent circuit of RS-422 transmitter

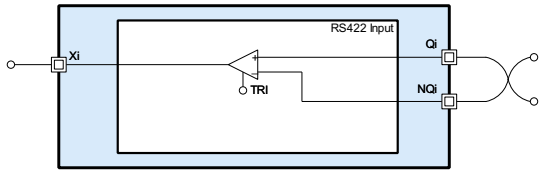


Figure 6: Equivalent circuit of RS-422 receiver

If the channel is a receiver, differential input signals at pins Qi/NQi are converted into single ended signals at Xi outputs. Incoming differential signals should follow RS-422 protocol. External resistors may be required to adapt signal voltage levels to iC-HF internal voltages. More information on the RS-422 receiver on page 23.

Output Enable bit OEN must be set hi in order enable the single ended output driver. With OEN = 0, the driver is left in high impedance.

In RS-422 receiver configuration the pull-down resistor is disabled and the differential output driver is left in high impedance.

If the channel is in *Encoder Link State*, signals present at input pins Xi are bypassed and directly connected to output pins Qi. Bidirectional channels in *Encoder Link State* present one bypassed line. Pull-up resistors and the output drivers are disabled. No signal is connected to NQi pins.

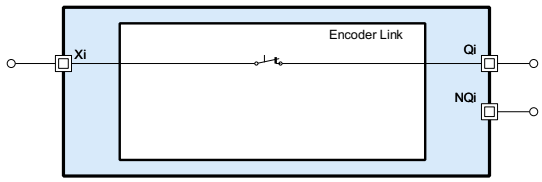


Figure 7: Equivalent circuit of one line in *Encoder Link State*

FUNCTION DESCRIPTION

iC-HF has 4 function modes. Each function mode combines the unidirectional and bidirectional channels with a specific configuration. iC-HF can be operated as a six channel line driver, as a 6 lines transceiver with BiSS/SSI connectivity or as a bus capable BiSS slave transceiver inserted in a *BiSS bus structure*. The 4 function modes are the following:

- *A/B/Z and U/V/W*
- *A/B/Z and BiSS/SSI*
- *BiSS bus structure*
- *BiSS bus loopback*

Selection of iC-HF's function mode is set by the pins FMSEL2 and FMSEL1:

FMSEL2	FMSEL1	MODE
0	0	*A/B/Z and U/V/W*
0	1	*A/B/Z and BiSS/SSI*
1	1	*BiSS bus structure*
1	0	*BiSS bus loopback*

Table 1: Mode Configurations

FMSELx pins include pull-down resistors. When there is no external connection to FMSELx pins, *A/B/Z and U/V/W* is the default selected mode.

A/B/Z and U/V/W Mode

If FMSEL2 = 0 and FMSEL1 = 0, iC-HF is configured in *A/B/Z and U/V/W* mode. *A/B/Z and U/V/W* mode is the default mode. In this mode all 6 channels work as line drivers. Single ended input signals at pins X1 to X6 are converted into differential output signals at pins Q1/NQ1 to Q6/NQ6. Output signals follow RS-422 standard.

Output Enable pin "OEN" must be set hi to enable differential output signals. When working as 6-channel line driver, pins NX1 to NX3 are disabled. An example of iC-HF working as a 6-channel line driver is presented in Figure 8.

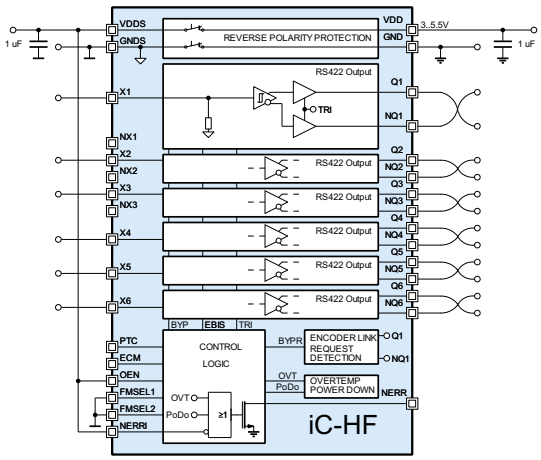


Figure 8: *A/B/Z and U/V/W* mode, 6 channel line driver

In *A/B/Z and U/V/W* mode it is possible to enter *Encoder Link State*. If *Encoder Link State* in this mode is entered, signals at pins X1 to X6 are directly linked to output pins Q1 to Q6. Input signals at pins NX1 to NX3 are also linked to output pins NQ1 to NQ3. Altogether, 9 lines are available in *A/B/Z and U/V/W* mode in *Encoder Link State*.

To enter *Encoder Link State*, ECM pin must be set hi and two signals must be input at pins Q1 and NQ1 following a specific timing sequence. This timing sequence is called *Encoder Link Sequence*. More information about entering *Encoder Link State* on page 21.

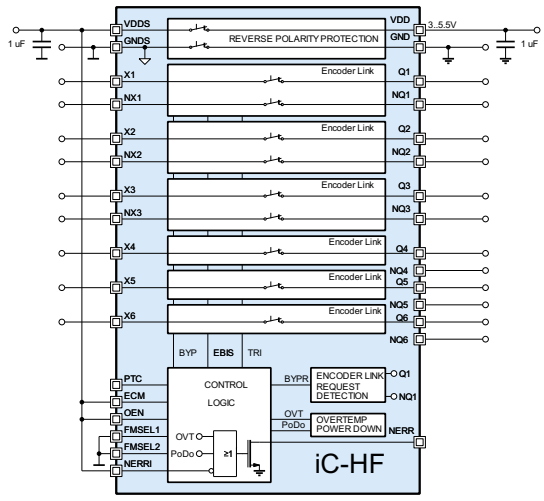


Figure 9: *A/B/Z and U/V/W* mode, 9 lines in *Encoder Link State*

A/B/Z and BiSS/SSI mode

If FMSEL2 = 0 and FMSEL1 = 1, iC-HF is configured in *A/B/Z and BiSS/SSI* mode. In *A/B/Z and BiSS/SSI* Mode channels 1, 2 and 3 work as line drivers, similar to *A/B/Z and U/V/W* mode.

Channels 4, 5 and 6 are used for implementing BiSS/SSI communication in RS-422. This allows com-

municating with a sensor using BiSS protocol and RS-422 physical layer, suitable for industrial environments. The sensor's BiSS lines should be connected to pins X4, X5 and X6 of iC-HF. The BiSS/SSI master must use pin pairs Q4/NQ4, Q5/NQ5 and Q6/NQ6 for BiSS communication.

Channel 4 is configured as an RS-422 output driver and carries SLO signal. SLO from the sensor in single ended form must be connected to input pin X4. The signal SLO will be delivered by pins Q4/NQ4 to the master following the RS-422 standard.

Channels 5 and 6 are configured as RS-422 input drivers. Channel 5 carries MA signal and delivers it to the sensor through pin X5 in a single ended signal. Channel 6 does the same with SLI signal.

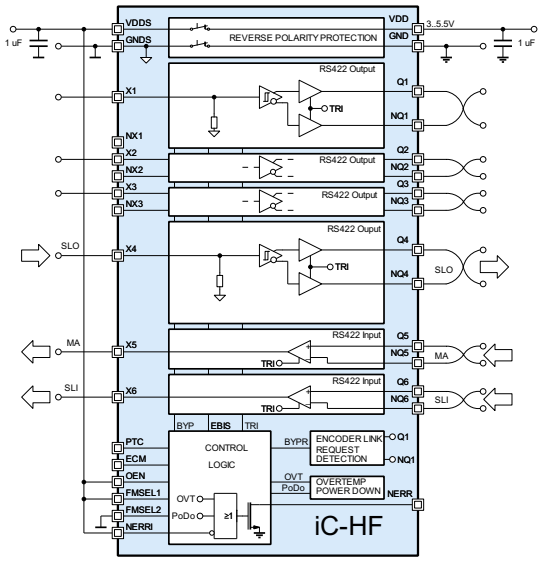


Figure 10: *A/B/Z and BiSS/SSI* mode, 3 channels line driver

In *A/B/Z and BiSS/SSI* mode it is possible to enter *Encoder Link State*. Only channels 1, 2 and 3 can enter Encoder Link state in this mode. Signals at pins X1 to X3 are directly linked to output pins Q1 to Q3 and signals at pins NX1 to NX3 to output pins NQ1 to NQ3. Altogether, 6 lines are available in *A/B/Z and BiSS/SSI* mode under *Encoder Link State*.

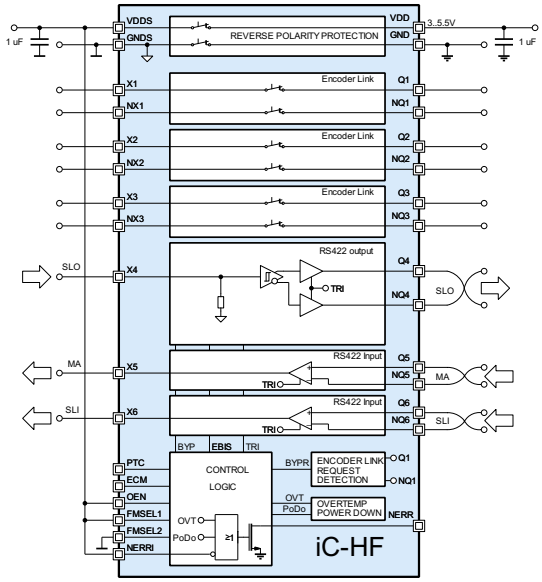


Figure 11: *A/B/Z and BiSS/SSI* mode, 6 lines in *Encoder Link State*

To enter *Encoder Link State*, ECM pin must be set hi and two signals must be input at pins Q1 and NQ1 following a specific timing sequence. This timing sequence is called the *Encoder Link Sequence*. For more information about entering *Encoder Link State* on page 21.

BiSS bus structure

If FMSEL2 = 1 and FMSEL1 = 1, iC-HF is configured in *BiSS bus structure* mode. This mode allows to communicate with a sensor BiSS and including the sensor in a BiSS bus structure/topology. Signals will follow RS-422 protocol, making it suitable for industrial environments. For using this mode it is necessary that the sensor connected to iC-HF has an BiSS bus compatible interface.

In *BiSS bus structure* mode each differential channel carries a specific line from BiSS bus:

Channel Number	Input/Output	BiSS Signal
1	output	MA output
2	output	SLO
3	output	SL output
4	input	MA input
5	input	SLI
6	input	SL input

Table 2: Differential channel function in *BiSS bus structure* mode

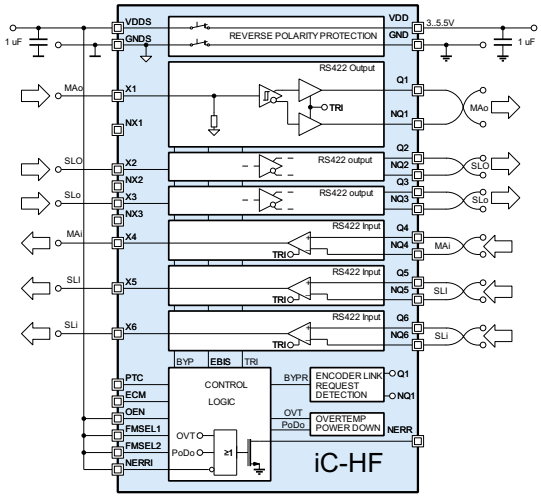


Figure 12: *BiSS bus structure* mode

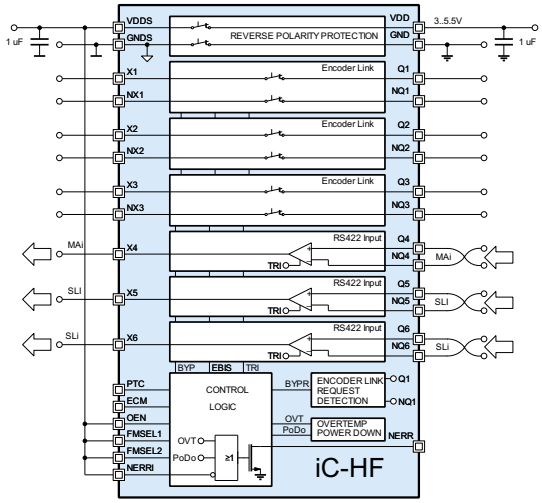


Figure 13: *Encoder Link State* in *BiSS bus structure* mode

In *BiSS bus structure* mode it is possible to enter *Encoder Link State*. Only channels 1, 2 and 3 can enter Encoder Link state in this mode. Signals at pins X1 to X3 are directly linked to output pins Q1 to Q3 and signals at pins NX1 to NX3 to output pins NQ1 to NQ3. Altogether, 6 lines are available in *BiSS bus structure* mode under *Encoder Link State*, as it is shown in Figure 13.

Figure 14 shows an example of connecting several sensor nodes in a *BiSS bus structure* using iC-HF. The location of the channels has been modified in the picture to have a clearer view of the data flow in the bus.

In the example, the slave nodes do not have SLo and SLi pins. Therefore, pins X3 and X6 should be externally connected to allow proper data flow.

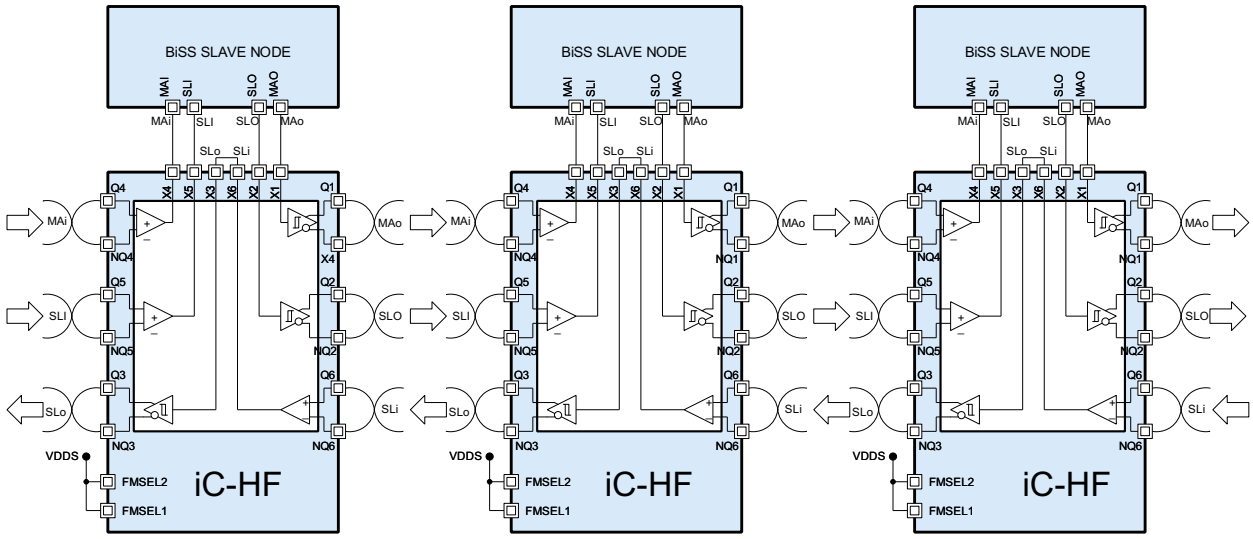


Figure 14: Several slave nodes in *BiSS bus structure*

BiSS bus loopback

If FMSEL2 = 1 and FMSEL1 = 0, iC-HF is configured in *BiSS bus loopback* mode. This mode is a particular case of *BiSS bus structure* mode, where iC-HF is operated as the termination node/loopback of the BiSS bus.

BiSS bus loopback allows addressing the case where the BiSS Bus is damaged. If the bus is somehow damaged, e.g. a broken wire, data will be interrupted and no communication will be possible. The last node previous to the point of damage can be configured as a termination node of the BiSS bus by setting FMSEL = 0, avoiding the need of re-wiring last node's output channels. Therefore communication between nodes before

the damage point will still be possible. iC-HF does not detect a BiSS bus structure damage nor activate automatically the *BiSS bus loopback*.

When the iC-HF is configured as a termination node of the BiSS bus, some channels configurations are changed with respect to *BiSS bus loopback* mode. Channel 1 is disabled and pins Q1/NQ1 will be in high impedance. The clock input signal MA entering channel 4 is no longer transmitted along the bus through channel 1.

Output signals from channel 2 will also be disabled, setting Q2/NQ2 to high impedance. Input signals at X2 will be internally connected to channel 3 and output through pins Q3/NQ3. The data input signal SLI entering channel 5 is no longer transmitted through SLO at channel 2. The data input signal SLI is transmitted through signals SLo at channel 3.

Input signals at X3 are disabled. The data return input signals SLi at channel 6 will no longer be transmitted through channel 3.

Table 3 summarizes each differential channel's function in this mode.

Channel Number	Input/Output	BiSS Signal
1	disabled	-
2	disabled	-
3	output	SL output
4	input	MA input
5	input	SLI
6	input	-

Table 3: Differential channel function in *BiSS bus loopback* mode

In *BiSS bus loopback* mode it is possible to enter *Encoder Link State*. Only channels 1, 2 and 3 can enter Encoder Link state in this mode. Signals at pins X1 to X3 are directly linked to output pins Q1 to Q3 and signals at pins NX1 to NX3 to output pins NQ1 to NQ3. Altogether, 6 lines are available in *BiSS bus loopback* mode under *Encoder Link State*, as it is shown in Figure 16.

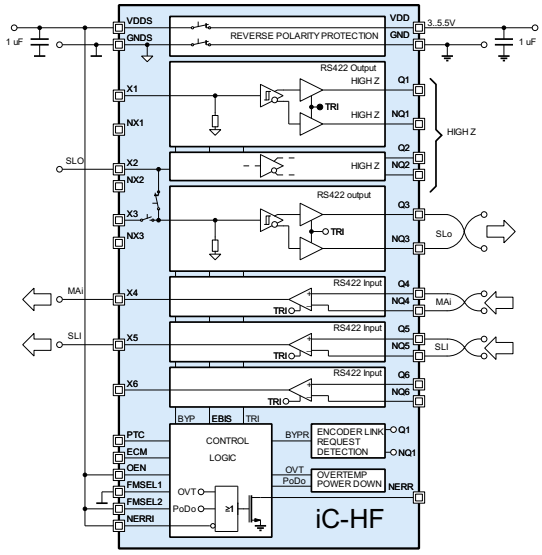


Figure 15: *BiSS bus loopback* mode

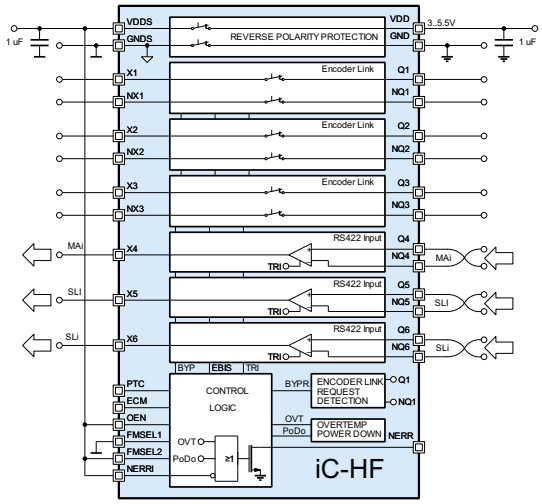


Figure 16: *Encoder Link State* in *BiSS bus loopback* mode

Figure 17 shows an example of several sensor nodes in BiSS bus using each iC-HF for a bus capable transceiver. The location of the channels has been modified in the picture to have a clearer view of the data flow in the bus.

The example shows the case of a broken cable. The node in the middle is configured as the bus terminator. Data flow occurs from left to right. When reaching the middle node, it goes back in the left direction.

The slave nodes typically do not have SLo and SLi pins. Therefore, pins X3 and X6 should be externally connected in order to allow proper data flow.

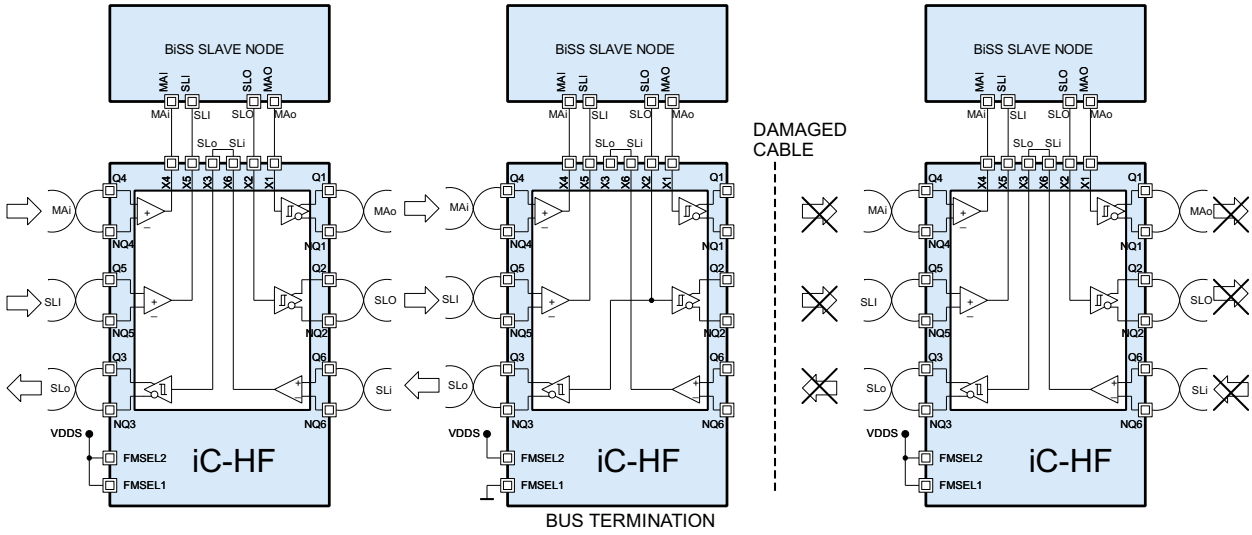


Figure 17: BiSS bus with node in *BiSS bus loopback*

Summary of Function Modes

Channel	FMSEL2 FMSEL1 Mode	0 0 **ABZ / UVW** [1]	E-Link [2]	0 1 **ABZ / BiSS**	E-Link	1 1 **BiSS Bus**	E-Link	1 0 **BiSS Loopback**	E-Link
1 (unidirect.)		Diff. Output	Yes	Diff. Output	Yes	Diff. Outp. MA	Yes	High Z	Yes
N1			Yes		Yes		Yes	High Z	Yes
2 (unidirect.)		Diff. Output	Yes	Diff. Output	Yes	Diff. Outp. SLO	Yes	High Z	Yes
N2			Yes		Yes		Yes	High Z	Yes
3 (unidirect.)		Diff. Output	Yes	Diff. Output	Yes	Diff. Outp. SL	Yes	Diff. Outp. SLO	Yes
N3			Yes		Yes		Yes		Yes
4 (bidirect.)		Diff. Output	Yes	Diff. Outp. SLO	No	Diff. Inp. MA	No	Diff. Input MA	No
5 (bidirect.)		Diff. Output	Yes	Diff. Inp. MA	No	Diff. Inp. SLI	No	Diff. Input SLI	No
6 (bidirect.)		Diff. Output	Yes	Diff. Inp. SLI	No	Diff. Inp. SL	No	Unused (SL)	No

General conditions: [1] OEN = 1, [2] ECM = 1

Table 4: Function Modes

INTERNAL PROTECTION AND ERROR SIGNALING

iC-HF is protected against internal overtemperature. When internal temperature is higher than a safety value (cf. *Electrical Characteristics no. 005*), an overtemperature event (OVT) is triggered and all output stages are set to high impedance though internal signal ”TRI”. Output stages are also left in high impedance if a power-down (PoDo) event is detected.

When the channel outputs are in high impedance, this is signaled through output pin NERR. NERR is an open-drain output and it goes lo when an overtemperature or power-down event is triggered, when OEN is lo, or when NERRI input is set lo.

The logic state of signal at input pin NERRI is directly passed to NERR output. This allows transferring an error signal from the sensor through iC-HF. If not used, NERRI should always be set hi.

Figure 18 shows an example of using NERRI pin for combining the external NERRI input signal from iC-MH16 with the iC-HF internal OVT and PoDo error signals to NERR output. In this example, iC-HF is in A/B/Z and U/V/W mode, operating as a set of 6 line drivers.

The open drain NERR output is protected against external short circuit. An error LED can be driven directly and used for visual warning or the NERR signal can be connected to a microcontroller interrupt pin.

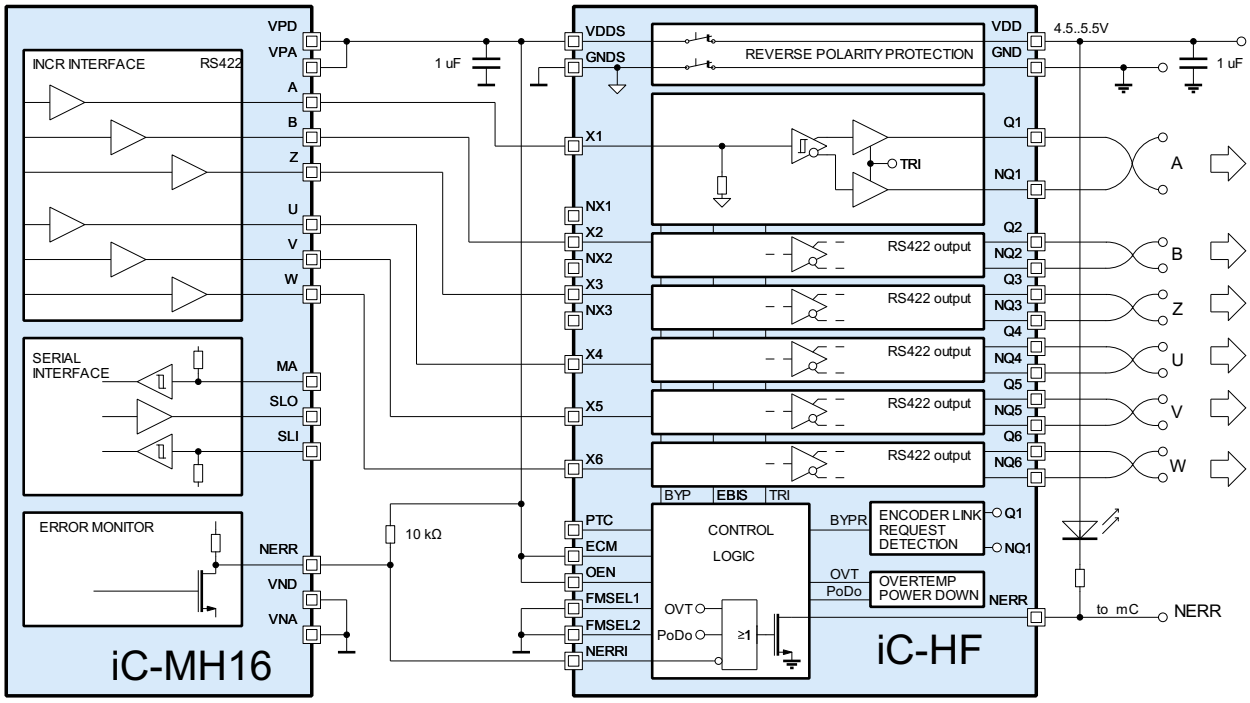


Figure 18: NERR signaling example in A/B/Z and U/V/W mode

REVERSE POLARITY PROTECTION

iC-HF is protected against applying reverse supply voltage at pins VDD and GND. Connecting a power supply with reverse polarity to an unprotected chip would permanently damage it.

iC-HF has a reverse polarity detection block. When a reverse polarity connection is detected, iC-HF provides the following protection actions:

- Power supply for internal blocks is disabled
- The RS-422 output drivers are supplied by VDD.
- The RS-422 output drivers are high impedance when VDD not ok.
- This high impedance when VDD is not includes lines Q1 to Q6, NQ1 to NQ6 and NERR line.

iC-HF also provides extended reverse polarity protection through output power supply lines VDDS (VDD switched) and GNDS (GND switched). These pins are connected to VDD and GND through a protecting switch. When a reverse polarity is detected at VDD/GND, VDDS and GNDS are internally disconnected. If a sensor is supplied by iC-HF through VDDS/GNDS lines, the polarity protection on iC-HF will be extended to the sensor.

VDDS can supply a maximum of 60 mA (cf. *Electrical Characteristics no. 003*). The current consumption of the sensor connected to the protected supply pins should not exceed this value.

Figure 19 shows connection of a sensor through extended reverse polarity protection.

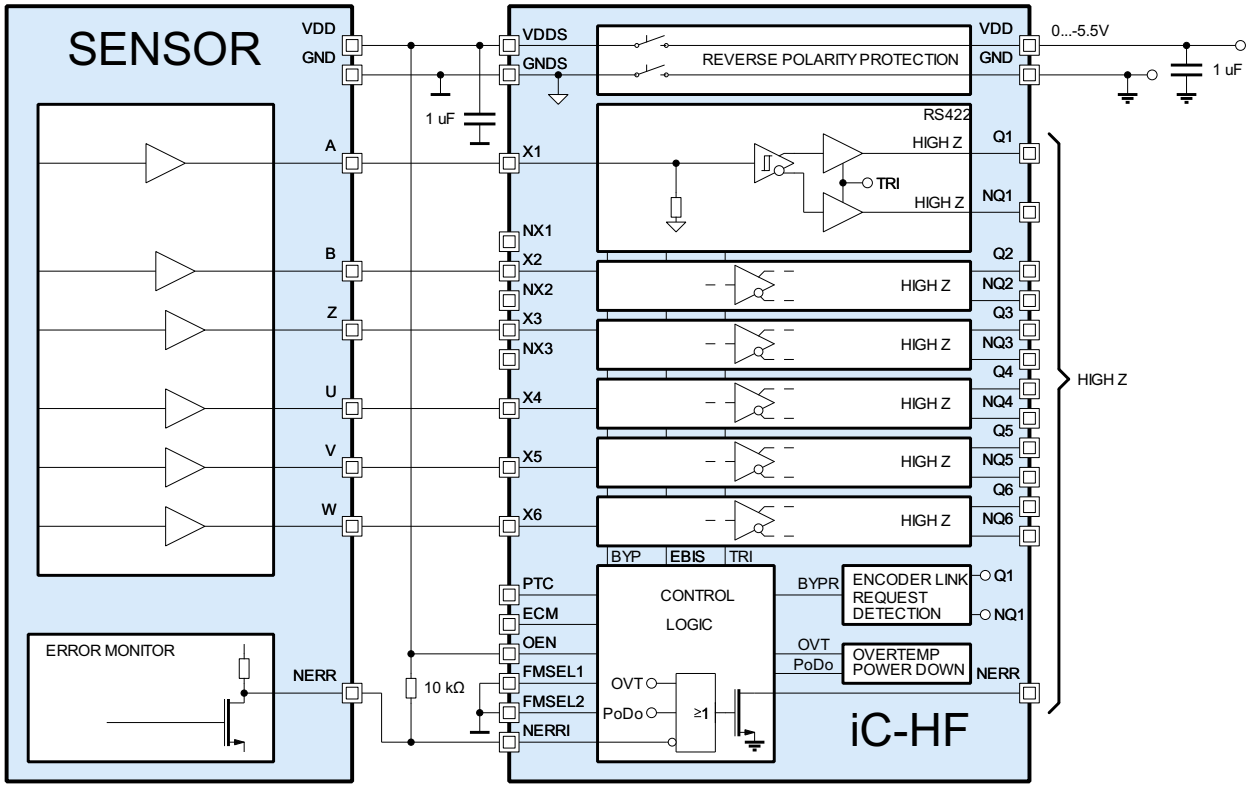


Figure 19: Extended reverse polarity protection

It is possible to connect to iC-HF a sensor that demands more than the maximum permissible load current (cf. *Electrical Characteristics no. 003*). However, connection of the sensor to iC-HF pins VDDS and GNDS should be avoided. A load exceeding this maximum value will prevent iC-HF to comply with electrical characteristic no. 701 and no. 702. Instead, the sensor should be supplied directly through pins VDD and GND. Figure 20 shows an example.

If configuration in Figure 20 is implemented, it must be noticed that iC-HF will still be protected against reverse polarity but this will not be the case of the sensor.

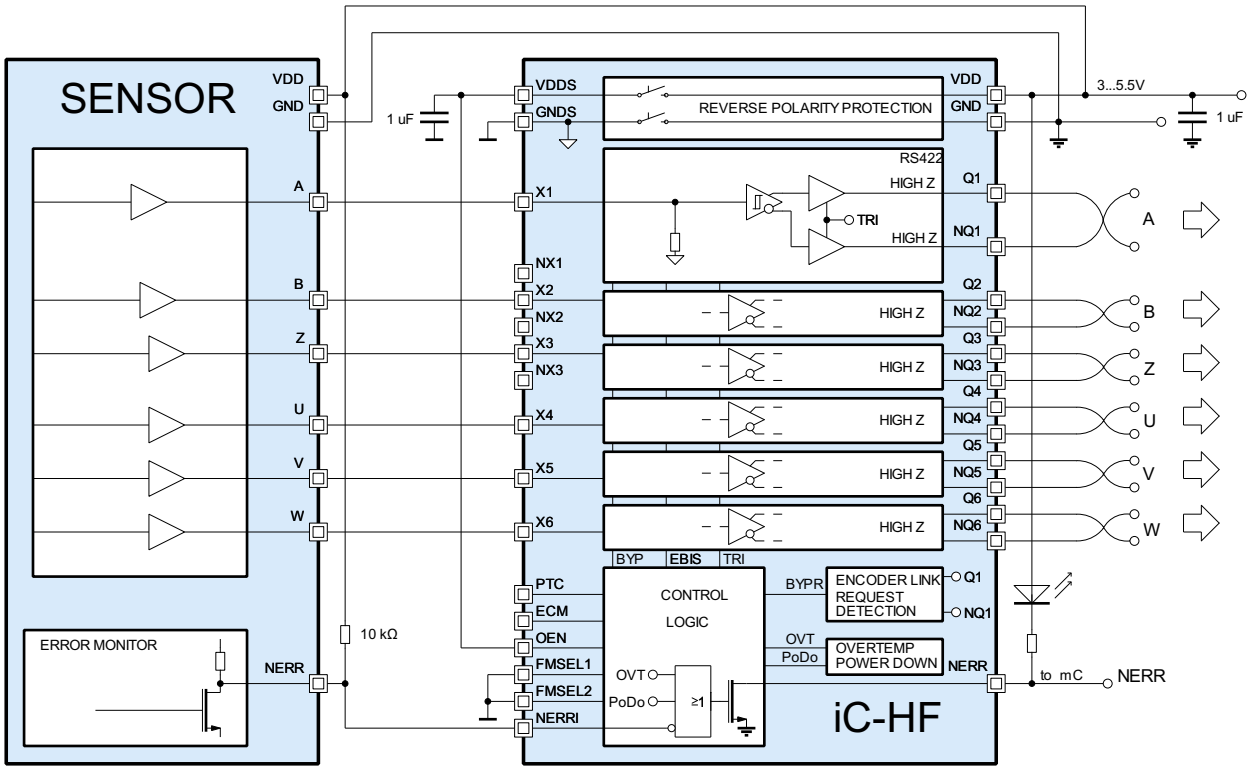


Figure 20: Example connection for a sensor with exceeding the maximum permissible load current

Figure 21 shows an alternative example. In this case, VDD and GND lines are short-circuited with VDDS and GNDS lines. This configuration option is permitted, but it is however not recommended. Connecting VDD and GND to VDDS and GNDS prevents having reverse polarity protection in iC-HF.

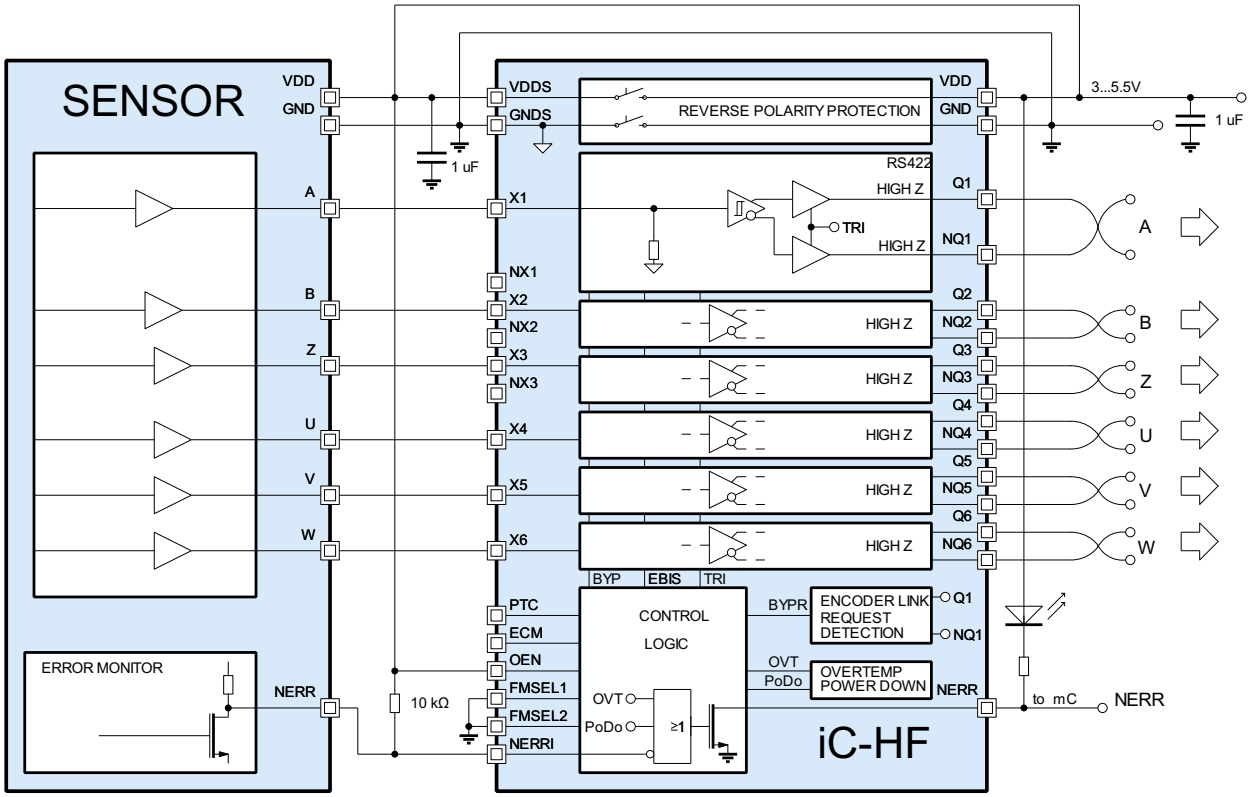


Figure 21: Alternative example connection for a sensor with exceeding the maximum permissible load current

ENCODER LINK SEQUENCE

All modes A/B/Z and U/V/W, and A/B/Z and BiSS/SSI, and BiSS bus structure, and BiSS loop back modes support *Encoder Link State*. FMSEL1 may have any state and is uncritical for reaching the *Encoder Link State*. In this state some input signals at pins Xi and NXi are linked directly to outputs Qi and NQi. The pins that are linked in the *Encoder Link State* depend on the function mode. In A/B/Z U/V/W 9 lines are available, while in the remaining modes there are 6 lines available. This feature allows having direct access to analog signals of the sensor from pins Qi/NQi for calibration purposes.

To enter *Encoder Link State*, ECM pin must be set hi and two signals must be input at pins Q1 and NQ1 following a specific timing sequence. This timing sequence is called the *Encoder Link Sequence*. No additional pin is needed in to enter *Encoder Link State*. ECM can be used to inhibit entering the *Encoder Link State*. If ECM is lo, the *Encoder Link Sequence* will never be acknowledged.

An example of this sequence is presented in Figure 22. The sequence is divided into three time intervals or steps: $t1$, $t2$ and $t3$:

- In the first step both pins Q1 and NQ1 must be driven hi during a specific amount of time. This time is stored by a Finite State Machine and must fulfill the requirements specified by parameter *ts*, which is typically 50 µs (cf. Electrical Characteristics no. 803). Therefore, the following condition must be satisfied:

  $ts(min) < t1 < ts(max)$

- In the second step, both pins Q1/NQ1 must be released. They will go back to complementary state (in *BiSS bus loopback* mode Q1 must be pulled hi and NQ1 lo externally). In the example of Figure 22, input X1 is high and therefore Q1 goes high and NQ1 low when released. Q1/NQ1 must be kept in complementary state during an amount of time as close as possible to $t1$. The maximum allowed time tolerance is specified by parameter Δts, (cf. *Electrical Characteristics no. 804*).

  $(t1 - \Delta ts) < t2 < (t1 + \Delta ts)$

- In the final step both pins Q1 and NQ1 must be driven lo during an amount of time as close as possible to $t1$. The following condition must be fulfilled:

  $(t1 - \Delta ts) < t3 < (t1 + \Delta ts)$

- After $t3$ is elapsed, pins Q1/NQ1 must be released.

- Once released, iC-HF will enter *Encoder Link State*.

If any of the steps explained above is not fulfilled, the *Encoder Link Sequence* will be interrupted. A new attempt to enter *Encoder Link State* will have to start from the beginning of the *Encoder Link Sequence*.

There are 2 possibilities to exit *Encoder Link State*. Driving ECM pin lo will exit the configuration. Normally, ECM will be connected to VDDS. A power-down event also exits *Encoder Link State*, without the need of an extra pin.

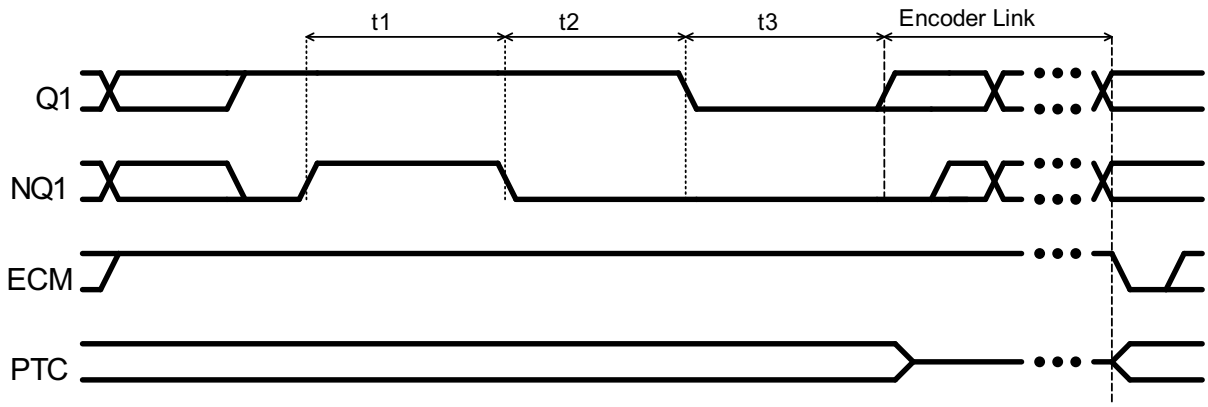


Figure 22: Time diagram of the *Encoder Link Sequence*

iC-PT/ iC-PT H-Series mode control

iC-HF is a general purpose 6-channel line driver. iC-HF is suitable to be operated with iC-PT and iC-PT H-Series opto encoder.

If iC-PT input pin SEL is lo, A/B mode is selected and iC-PT delivers complementary digital A/B/Z signals. If iC-PT input pin SEL is hi, iC-PT is in A/B mode with two fold interpolation. When iC-HF enters *Encoder Link State* output pin PTC provides VDD/2 to iC-PT and therefore iC-PT is forced to enter analog mode. In this analog mode, analog signals from the photosensors are directly output.

In order to improve the noise rejection and stability at pin PTC, an external 10nF capacitor C_{PTC} can be added between PTC and GNDS pins.

External pull-up and pull-down resistors at SEL pin can be used in order to select the iC-PT working mode. iC-HF output PTC pin is used to control the iC-PT to output analog signals. When Encoder Link mode is entered, PTC delivers VDD/2 voltage. If connected to SEL pin from iC-PT, this will enter analog mode and signals from the photosensors will be present at output pins Qi/NQi from iC-HF.

Figure 23 shows how to connect iC-PT and iC-HF in order to force Analog Mode in iC-PT when iC-HF enters Encoder Link. The recommended resistor values are given in table 5. See page 25 for more information on driving an iC-PT with iC-HF.

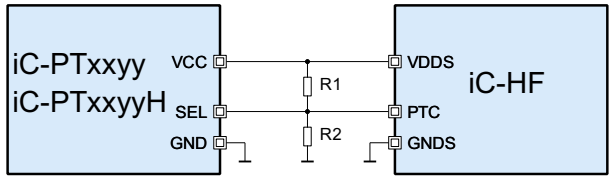


Figure 23: iC-PT and iC-HF connection for Analog Mode selection.

SEL	R1[1)]	R2[1)]	Operation Mode
100 % VCC	10 kΩ	open	ABZ x2 interpolated
50 % VCC	open	open	all analog
0 % VCC	open	10 kΩ	x1 interpolated
1) Exemplary values.			

Table 5: Selection of iC-PT operation mode by pin SEL.

iC-PT H-Series opto encoder include 3 additional working modes. Table 6 gives the recommended resistor values for fixing any working mode and allowing All Analog mode when iC-HF enters Encoder Link.

SEL	R1[1)]	R2[1)]	Operation Mode
100 % VCC	2.7 kΩ	open	x2 interpolated
75 % VCC	12 kΩ	48 kΩ	analog ABZ, dig. UVW
50 % VCC	open	open	all analog
25 % VCC	48 kΩ	12 kΩ	x4 interpolated
0 % VCC	open	2.7 kΩ	x1 interpolated
1) Exemplary values.			

Table 6: Selection of iC-PT H-Series operation mode by pin SEL.

RS-422 RECEIVER CONFIGURATION

In A/B/Z and BiSS/SSI mode, *BiSS bus structure* mode, and *BiSS bus loopback* mode some channels are configured as RS-422 receivers. Table 7 presents the function modes together with the channels that are configured as RS-422 receivers.

Function mode	RS-422 receiving channels
A/B/Z and BiSS/ISS	channel 5 and 6
BiSS bus structure	channel 4, 5 and 6
BiSS bus loopback	channel 4, 5 and 6

Table 7: RS-422 receiving channels

Some parameters are important in characterizing the receiver: the input voltage (VQi and VNQi), the differential voltage (Vid), and the common mode voltage (Vic), where:

$$Vid = VQi - VNQi$$

$$Vic = \frac{VQi+VNQi}{2}$$

Figure 24 shows these voltages.

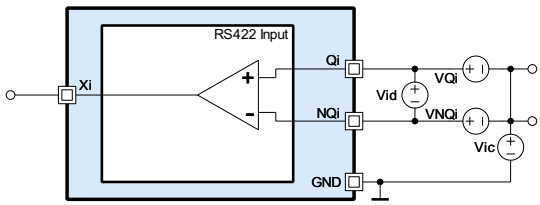


Figure 24: RS-422 input sensitivity

Possible voltage ranges of RS-422
To comply with the possible voltage ranges of RS-422 standard, the RS-422 receiver must fulfill the following requirements:

- Over an entire common mode voltage ranging from -7 V to 7 V the receiver should not require a differential input voltage of more than |200 mV| to correctly assume the intended binary state.
- The receiver has to maintain correct operation for differential input voltages ranging from 200 mV to 10 V in magnitude.
- The maximum input voltage (VQi, VNQi) shall not exceed 10 V in magnitude.
- The receiver must be able to operate with a maximum differential of 12 V without being damaged.

Figure 25 illustrates the minimum and maximum operating voltages of the receiver.

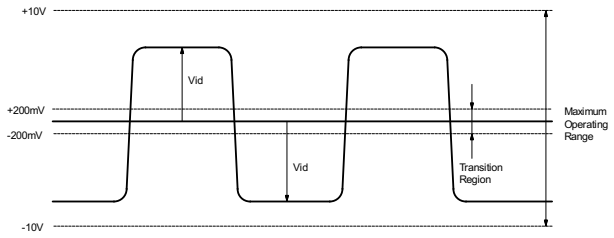


Figure 25: RS-422 input maximum and minimum operating voltages

It is not allowed in iC-HF to apply negative input signals or signals higher than supply voltage. Following these requirements, table 8 shows the sensitivity, the minimum and the maximum values at the receiver.

Parameter	Minimum	Maximum
Vi(Qx)	0 V	5.5 V
Vi(NQx)	0 V	5.5 V
|Vid|	50 mV	5.5 V
Vic	800 mV	5.5 V

Table 8: RS-422 sensitivity and input voltages

To comply with the total voltage ranges of RS-422 external resistors can be placed in line of the input pins each receiver. The resistor value is 16.9 kΩ with a tolerance of 1%. The relative tolerance of both resistors (matching) requires a tolerance of 0.1%.
An elegant solution is an integrated resistor network with a matching better 0.1% e.g. :

- Vishay ACAS 0606 for a point-to-point BiSS interface (MA+/- input) with two resistors each 4 pin package.
- Vishay ACAS 0612 for a BiSS bus structure interface (MA+/-, SLI+/- inputs) with four resistors each 8 pin package.

It is recommended to locate such optional resistors closely and symmetrically to the related RS-422 input pins. If these resistors are used, the sensitivity, the minimum, and the maximum input voltages at the receiver are shown in table 9. With these resistors in use a measurement between iC-HF and the resistors can be sensitive due to possible additional capacitive load of probe(s).

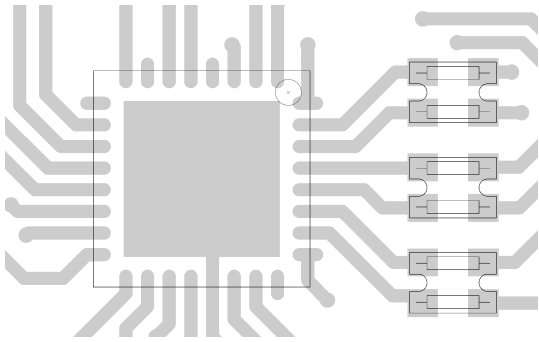


Figure 26: External resistors layout location example for RS-422 receiver

Parameter	Minimum	Maximum
Vi(RTQx)	-10 V	10 V
Vi(RTNQx)	-10 V	10 V
|Vid|	200 mV	12 V
Vic	-7 V	7 V

Table 9: RS-422 sensitivity and input voltages with external resistors

In addition to the external resistors, the bus termination resistor of 120 Ω should be placed between both inputs of the receiver. Figure 27 shows this configuration.

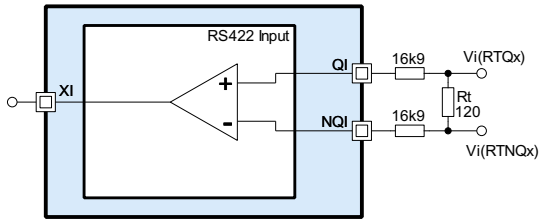


Figure 27: RS-422 receiver with external resistors

iC-HF allows RS-422 communication up to 10 MHz. At high frequencies the performance can be improved by using 1 pF capacitors parallel with each external resistor (excluding the bus termination resistor). Some designs do provide such similar capacity already by layout.

Note: Operating the iC-HF without further external circuitry over the entire RS-422 voltage range will result in permanent damage because iC-HF is designed for 5 V signals on the serial BiSS/SSI interface. For full RS-422 compliance with +12 V / -7 V / ±10 V, the receiver inputs require the resistor network as described. To enable the full RS-422 operating voltage range, the protection diodes and TVS diodes used must then be RS-422 compatible types.

Unused/open RS-422 input pins
To avoid oscillations on open or unused pins a stable state is recommended. Unused or open RS-422 input pins can be to be connected to a stable voltage. The voltage of the positive and negative input pin needs to be bigger than the input hysteresis. In the case of unused input pins the Qi and NQi pins should be connected to field sided, different, stable input voltages like VDD and GND.

Example for stable input voltages on unused/open pins:

- Qi = VDD
- NQi = GND

APPLICATION EXAMPLES

All figures indicate only the basic operation with iC-HF and do not contain all details, connections, configurations and options for a working system.

iC-HF can drive a wide range of applications and combinations of sensors and interpolators and their possible signals and interfaces. In this chapter, a group of examples on interconnecting different devices with iC-HF is presented.

- The blocking capacitor at VDD - GND will help to reduce the spikes due to the RS-422 drivers switching.
- A better blocking against spikes at the iC can be improved by placing the capacitor closer to the iC-HF.

Function Mode	iC-PT H-Series	iC-MU	iC-MH16 iC-MHM	iC-NQ
A/B/Z and U/V/W	X	X	X	
A/B/Z and BiSS/SSI		X	X	X

Table 10: Applications and modes

iC-PT/ iC-PT H-Series

Figure 28 shows an example of using iC-HF for driving iC-PT/ iC-PT H-Series, which are three complementary channel photodiode arrays. iC-PT/iC-PT H-Series are supplied through the reverse polarity protected supply pins, VDDS and GNDS.

FMSEL1 and FMSEL2 are set to lo, therefore iC-HF is in *A/B/Z and U/V/W* mode, a 6 channel RS-422 line driver.

A pull-down resistor (10 kΩ for iC-PT, 2.7 kΩ for iC-PT H-Series) at SEL pin forces iC-PT/ iC-PT H-Series to work in A/B operation x1 interpolated. Outputs PA, PB, and PZ are connected to pins X1 to X3. Therefore, A, B, and Z signals are transmitted under RS-422 protocol through channels 1 to 3. Signals U, V, and W are connected to inputs X4 . . . X6 and outputs through channels 4 to 6. Set the OEN pin hi for channel enabling.

iC-HF enters *Encoder Link State* when ECM pin is set to hi. Pins NA, NB, and NZ from iC-PT/ iC-PT H-Series are connected to NX1, NX2, and NX3 respectively. PTC from iC-HF is connected to SEL from iC-PT/ iC-PT H-Series. After a successful *Encoder Link Sequence*, SEL/PTC node will be driven at VDDS/2. iC-PT H-Series will enter analog mode and all signals will be directly linked to output pins Qi/NQi.

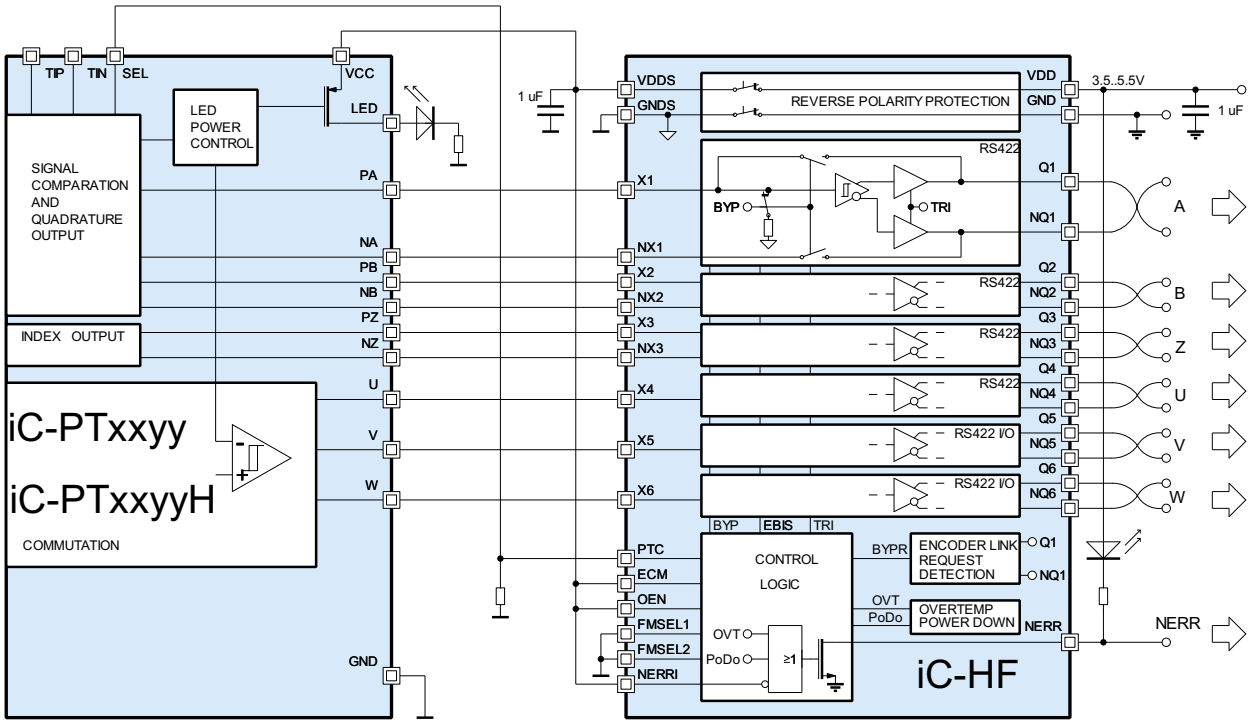


Figure 28: Example application of iC-PT/ iC-PT H-Series in A/B operation x1 interpolated with iC-HF

iC-MH16, iC-MH8, iC-MHM

Figure 29 shows an example driving iC-MH16, a 12 bit angular Hall encoder (iC-MH16, iC-MH8, iC-MHM can also be used). iC-HF provides reverse polarity protection.

In this example, FMSEL1 and FMSEL2 are low and *A/B/Z and U/V/W* mode is selected. All 6 channels work as RS-422 line drivers. OEN is set hi and all channels are enabled. iC-MH16 has no complementary outputs, therefore pins NX1 . . . NX3 from iC-HF are kept disconnected.

After a valid *Encoder Link Sequence* all connected signals at X1 to X6 will be directly linked to outputs Q1 to Q6.

NERR output from iC-MH16 is connected to input pin NERRI of iC-HF. Any error occurring either on iC-MH16 or on iC-HF will be signaled through NERR output pin from iC-HF.

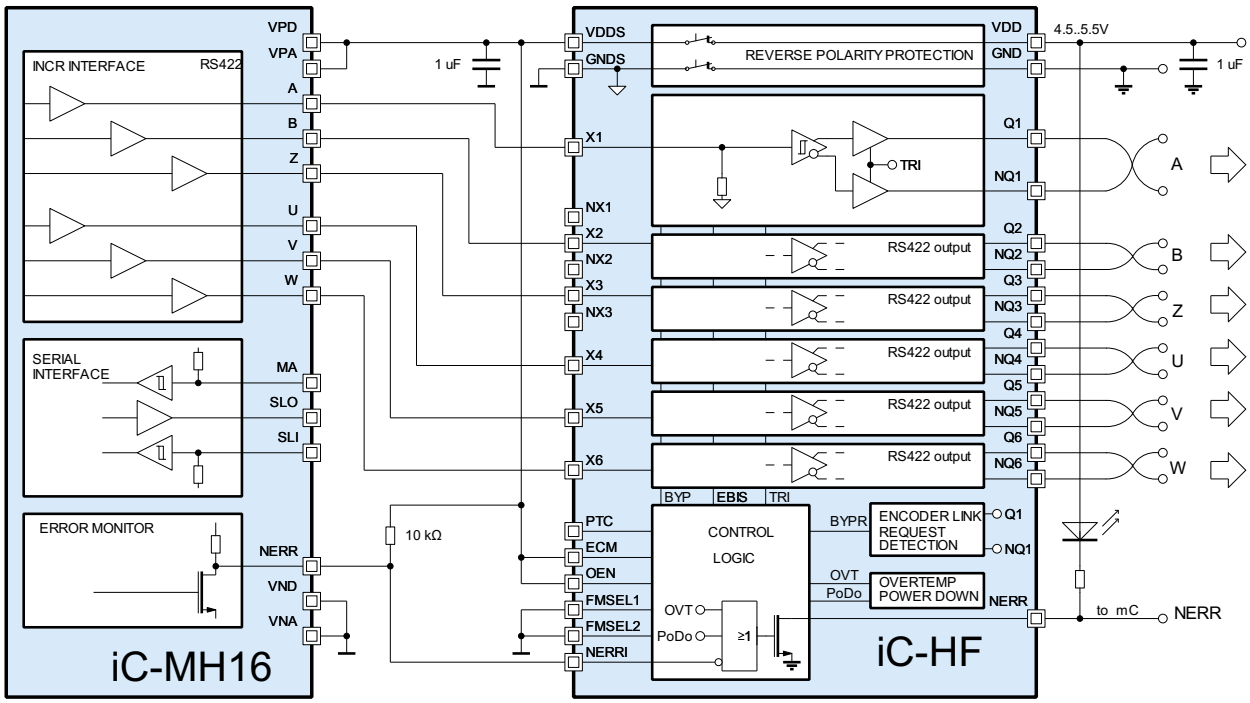


Figure 29: Example application with iC-MH16 in *A/B/Z and U/V/W* mode

Mind voltage and current requirements for programming/zapping OTP devices with iC-HF use.

iC-MH16 is a BiSS slave. If FMSEL1 from iC-HF is set hi, *A/B/Z and BiSS/SSI* mode is selected and iC-HF can be used to communicate through BiSS with iC-MH16. This is shown in figure 30.

Signals U, V, and W are replaced by BiSS signals MA, SLO, and SLI. Input RS-422 signals at channels 5 and 6 in the example include the adaptation resistors, together with the RS-422 bus termination resistor. See page 23 for more information about RS-422 receiver configuration.

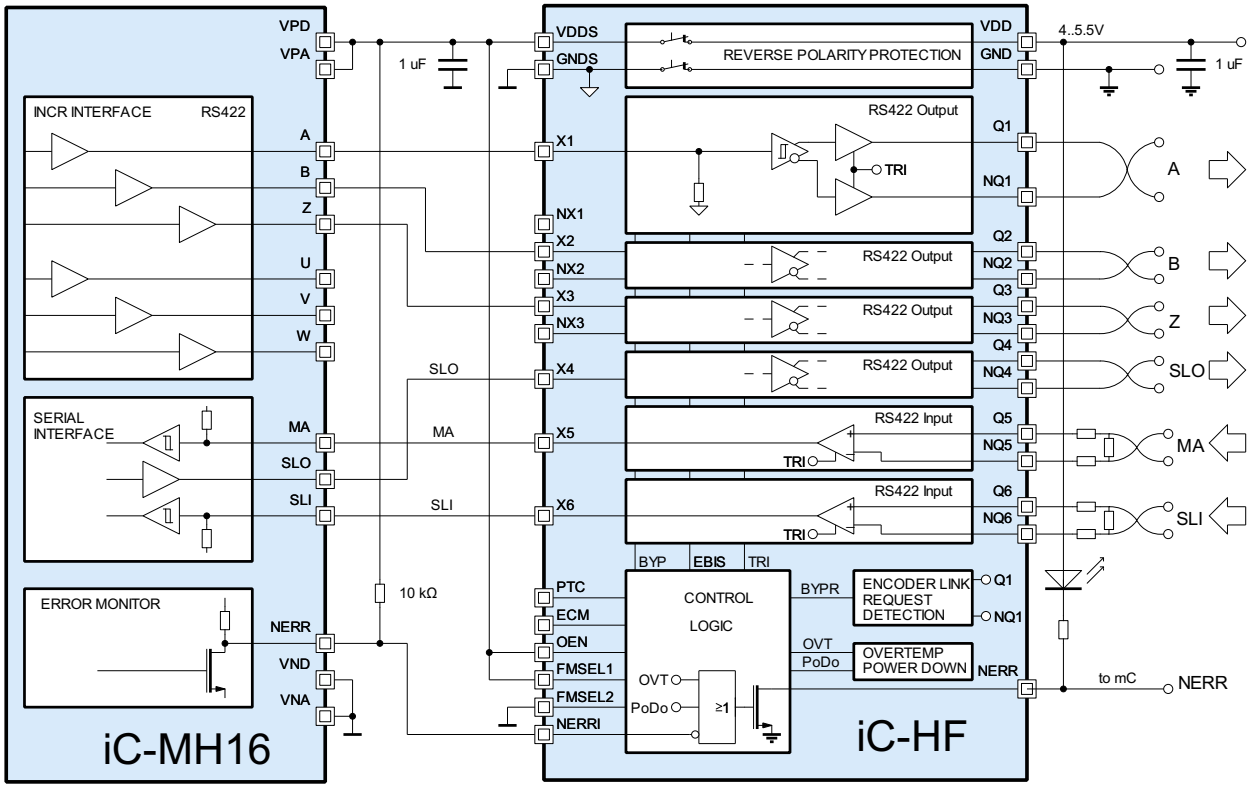


Figure 30: Example application with iC-MH16 in *A/B/Z and BiSS/SSI* mode

iC-MU

iC-MU is an off-axis nonius encoder with integrated Hall sensors. An example of iC-MU with iC-HF is shown in figure 31.

In this example, iC-MU is in ABZ function and iC-HF in *A/B/Z and U/V/W* mode. These signals are delivered through output pins PB0 to PB2, and PB3. iC-HF provides reverse polarity protection.

A microcontroller communicates with iC-MU. It can automatically enable/disable iC-HF output channels by driving OEN pin. NERR from iC-HF is used as external interrupt.

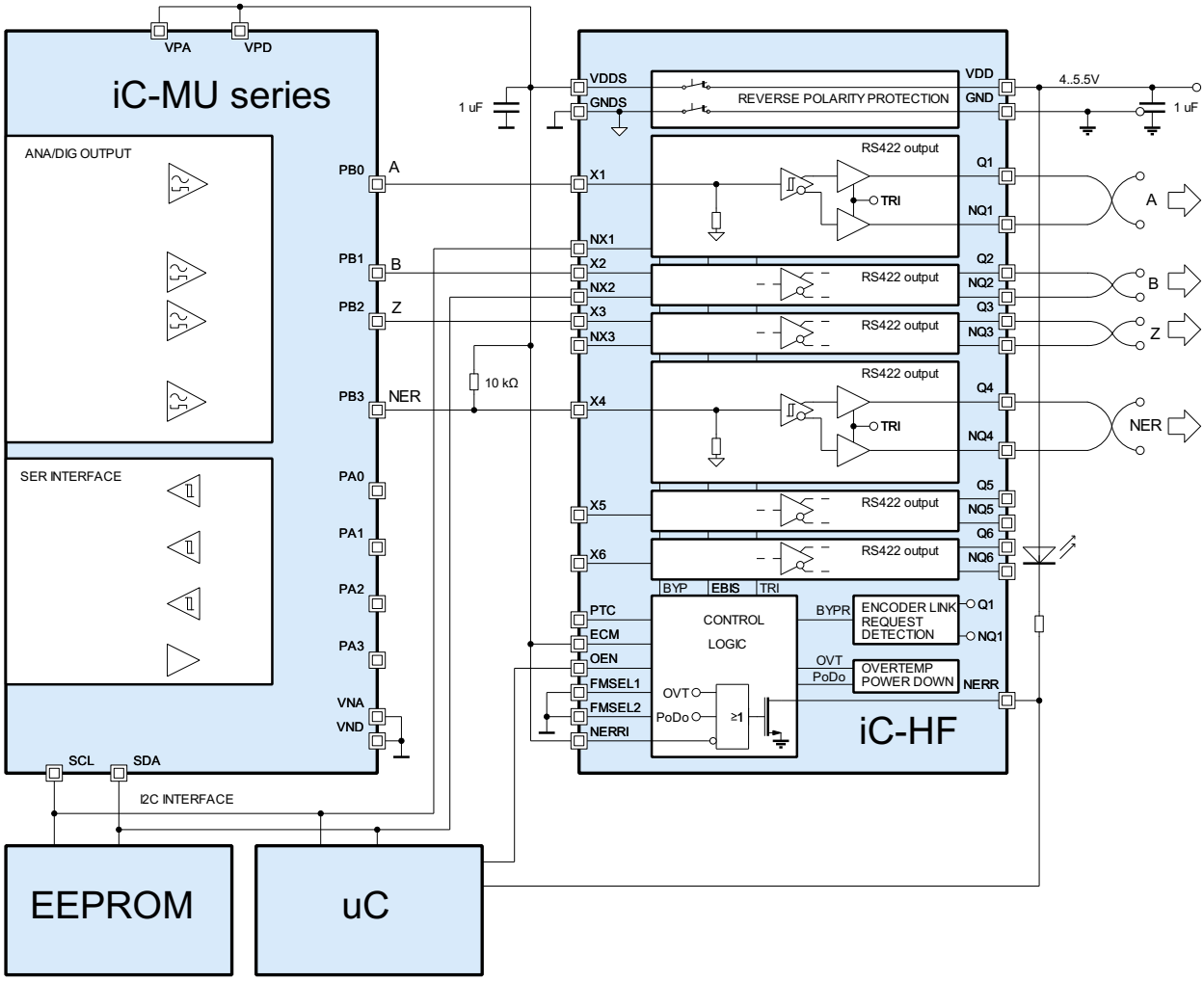


Figure 31: Example application with iC-MU and microcontroller with iC-HF in *A/B/Z and U/V/W* mode

Since ECM pin is held hi, it is possible to enter *Encoder Link State* with the *Encoder Link Sequence* at pins Q1/NQ1. iC-HF is in A/B/Z and U/V/W mode, therefore 9 *Encoder Link* lines are in use.

In *Encoder Link State*, I²C bus lines SCL and SDA are transmitted in the example through pins NQ1 and NQ2.

A command can be sent to the microcontroller through I²C to modify the state of iC-MU and select analog mode. In this mode, positive and negative sine, and positive and negative cosine signals are output via pins PB0 to PB3. These analog signals are directly linked to iC-HF output pins Q1 to Q4.

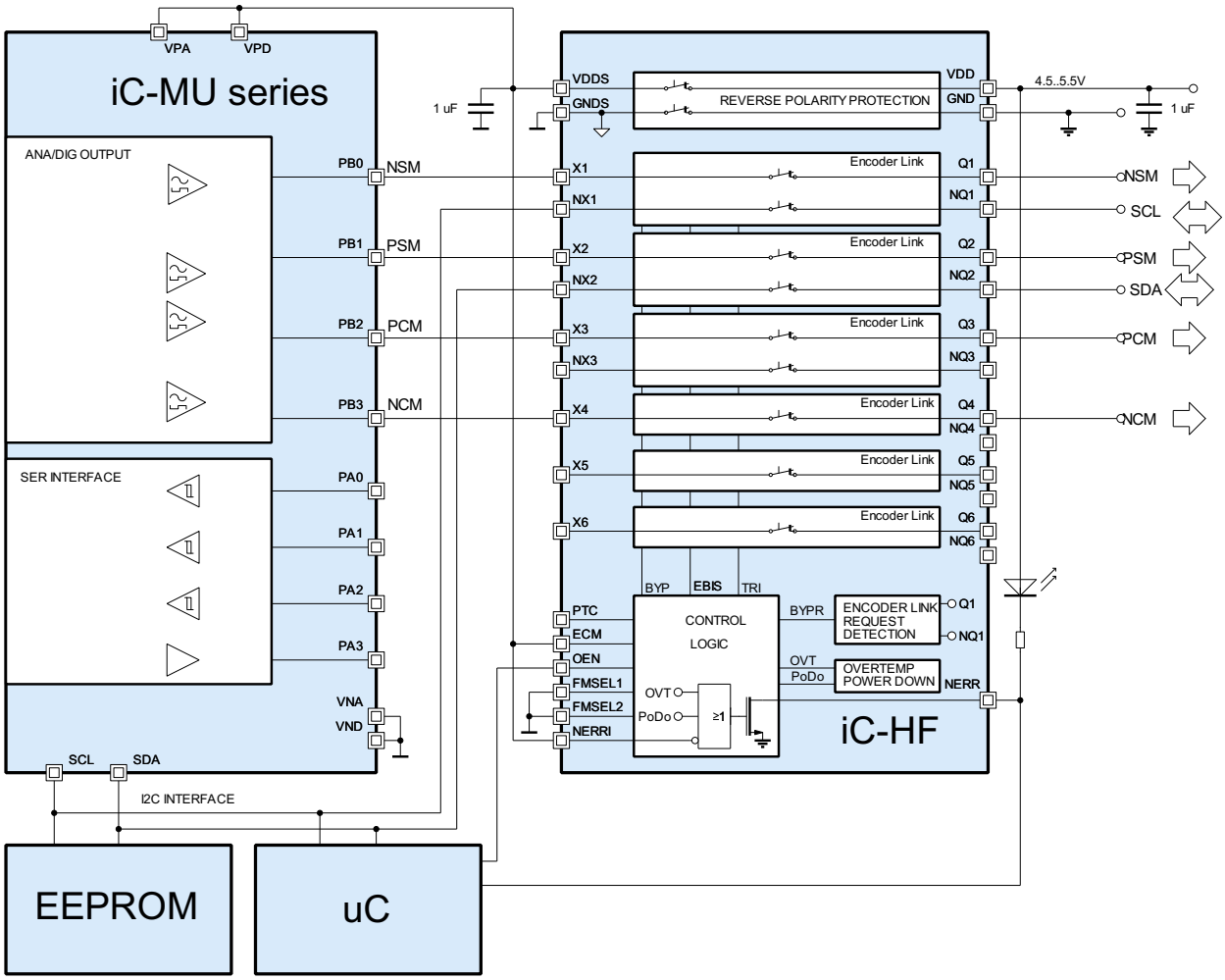


Figure 32: Example application with iC-MU and microcontroller with iC-HF in *Encoder Link State*

As shown in figure 33 iC-MU can also be operated as a BiSS slave. Master clock MA is input through, channel 5, data input SLI though channel 6, and data output SLO is sent through channel 4.

iC-MU is initially in ABZ function, and signals are output in RS-422 protocol by pins Q1, NQ1, Q2, NQ2, and Q3, NQ3. In ABZ function, PB3 provides the error signal from iC-MU. In the example, this signal is connected to NERRI from iC-HF and transferred through NERR.

PB3 is also connected to NX3 from iC-HF. If iC-MU changes to analog function and iC-HF enters *Encoder Link State*, analog signals at PB0 to PB3 will be linked inside iC-HF and output through pins Q1, Q2, Q3, and NQ3.

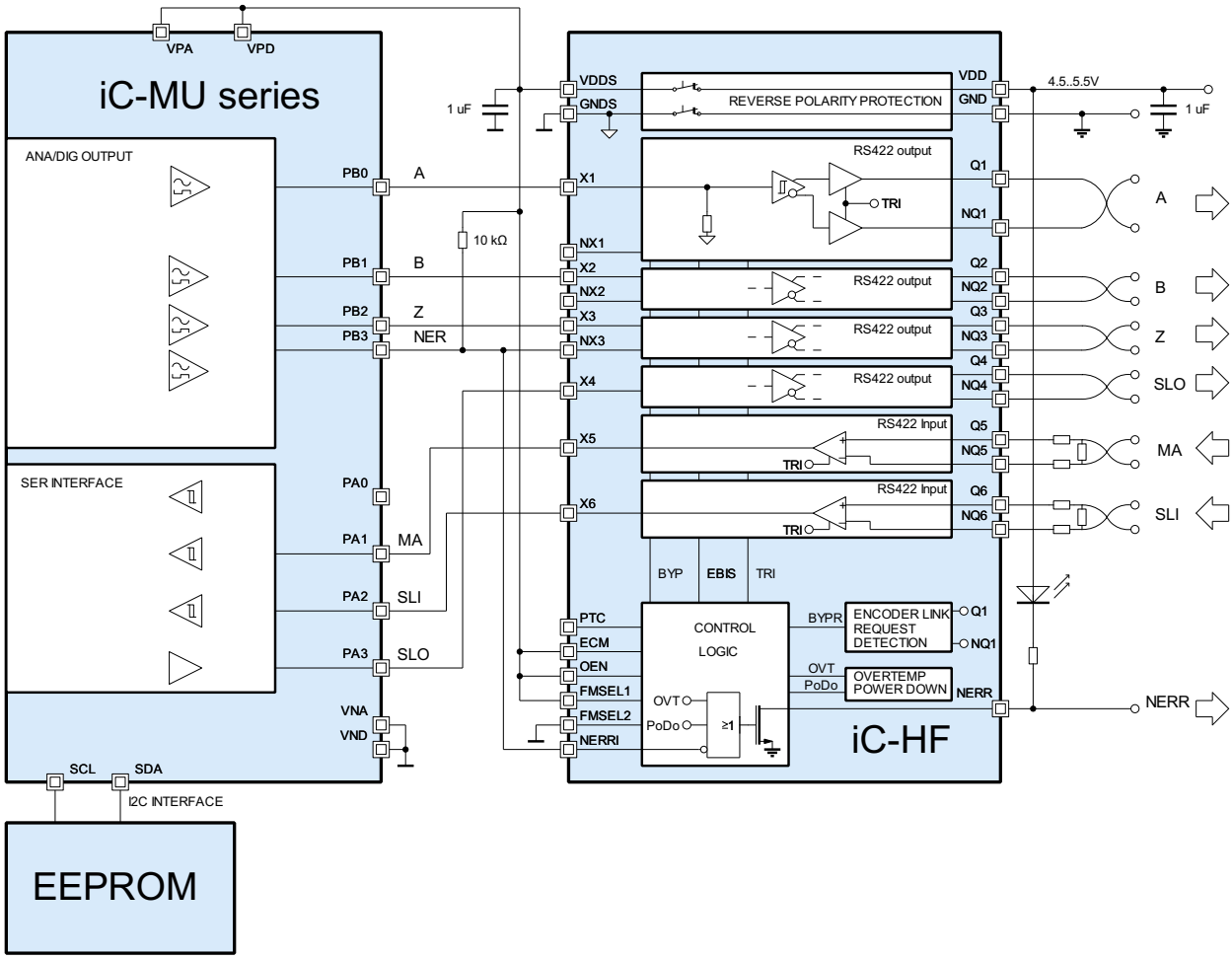


Figure 33: Example application with iC-MU and iC-HF in *A/B/Z and BiSS/SSI* mode

If it is desired to use only three channels of iC-HF (channels 1, 2, and 3), it is possible to implement BiSS communication with no need for extra channels. This can be achieved by using pins NQ1, NQ2, and NQ3. Figure 34 shows this example.

To achieve this, iC-HF must be configured either in *A/B/Z and U/V/W* mode (as in this example) or in *A/B/Z and BiSS/SSI* mode. In default state, iC-HF is a set of line drivers and signals. PB0, PB1, and PB2 from iC-MU are output through channels 1, 2 and 3 as differential signals. With the *Encoder Link Sequence* at pins Q1/NQ1, iC-HF enters *Encoder Link State*. Pins NQ1, NQ2 and NQ3 are directly connected to NX1, NX2 and NX3 respectively. It is possible to access the BiSS interface of iC-MU through these three lines, as shown in figure 34.

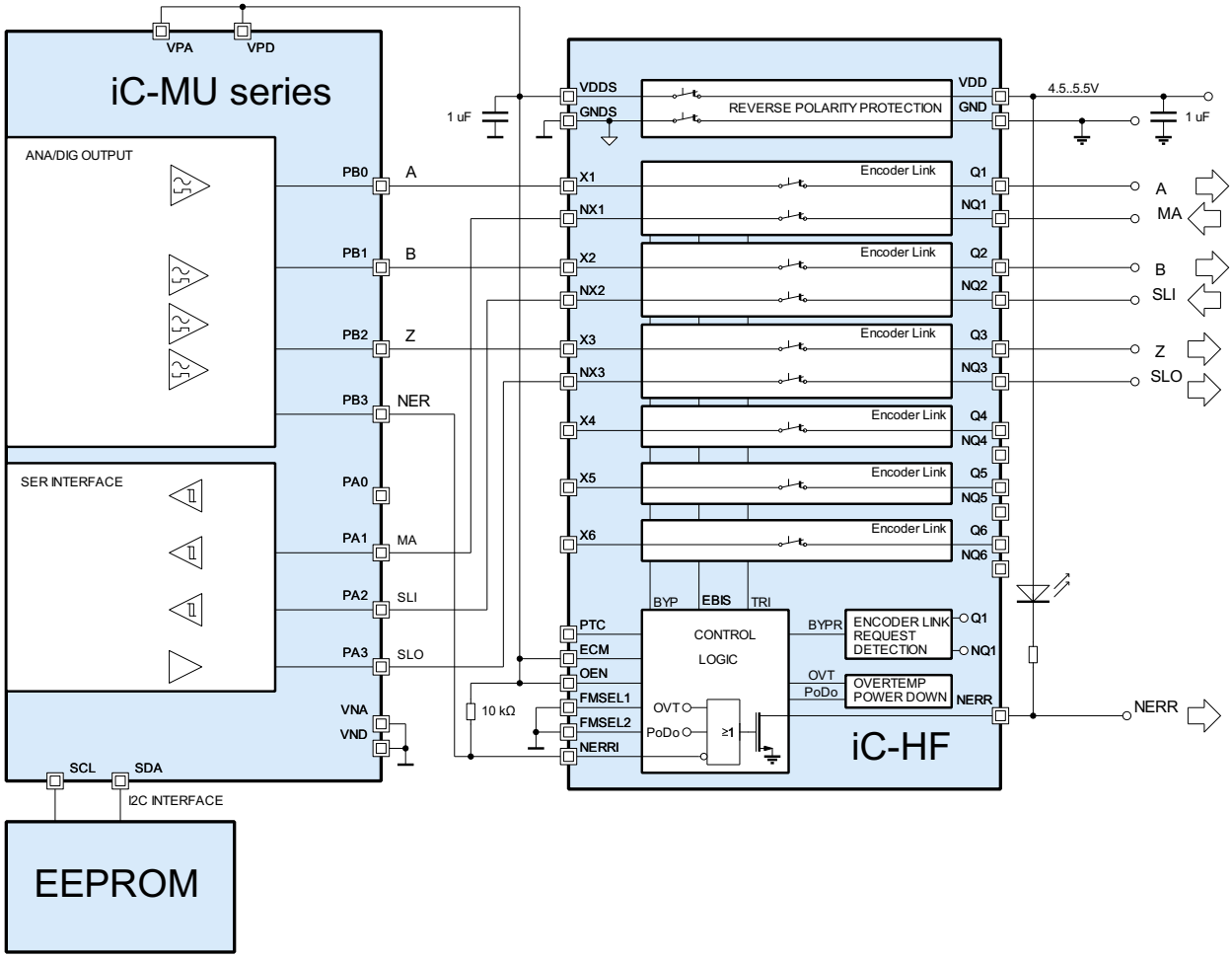


Figure 34: Example application with iC-MU in A/B/Z mode and iC-HF in *Encoder Link State* with BiSS at channels 1,2, and 3

iC-NQC

iC-NQC is a 13-bit sin/cosine-to-digital converter with calibration and can also be driven by iC-HF, as shown in figure 35. iC-HF provides reverse polarity protection to the sensor side interface through pins VDDS and GNDS.

In the example, iC-NQC is a BiSS slave node. iC-HF is configured in *A/B/Z and BiSS/SSI* mode through pins FMSEL2 and FMSEL1. BiSS signals SLO, MA and SLI are carried through iC-HF channels 4, 5 and 6, respectively.

In *Encoder Link State* the TMA mode of iC-NQC can be activated to bypass analog sine/cosine signals on A, B, SDA and SCL signals.

In a default mode, channels 1, 2 and 3 from iC-HF are operated as RS-422 line drivers, outputting A, B and Z signals from iC-NQC. An EEPROM is used in the example and it is accessed via I^2C bus. I^2C signals are also connected to iC-HF input pins NX1 and NX2. If iC-HF enters *Encoder Link State*, signals at X1 to X3 and NX1 to NX3 will be directly linked to output pins Q1 to Q3 and NQ1 to NQ3. Therefore, in this configuration the I^2C bus will be available at pins NQ1 and NQ2.

Error signal from iC-NQC is connected to NERRI of iC-HF. This allows combining an error event from iC-NQC with an error event of iC-HF that is signaled at NERR output of iC-HF.

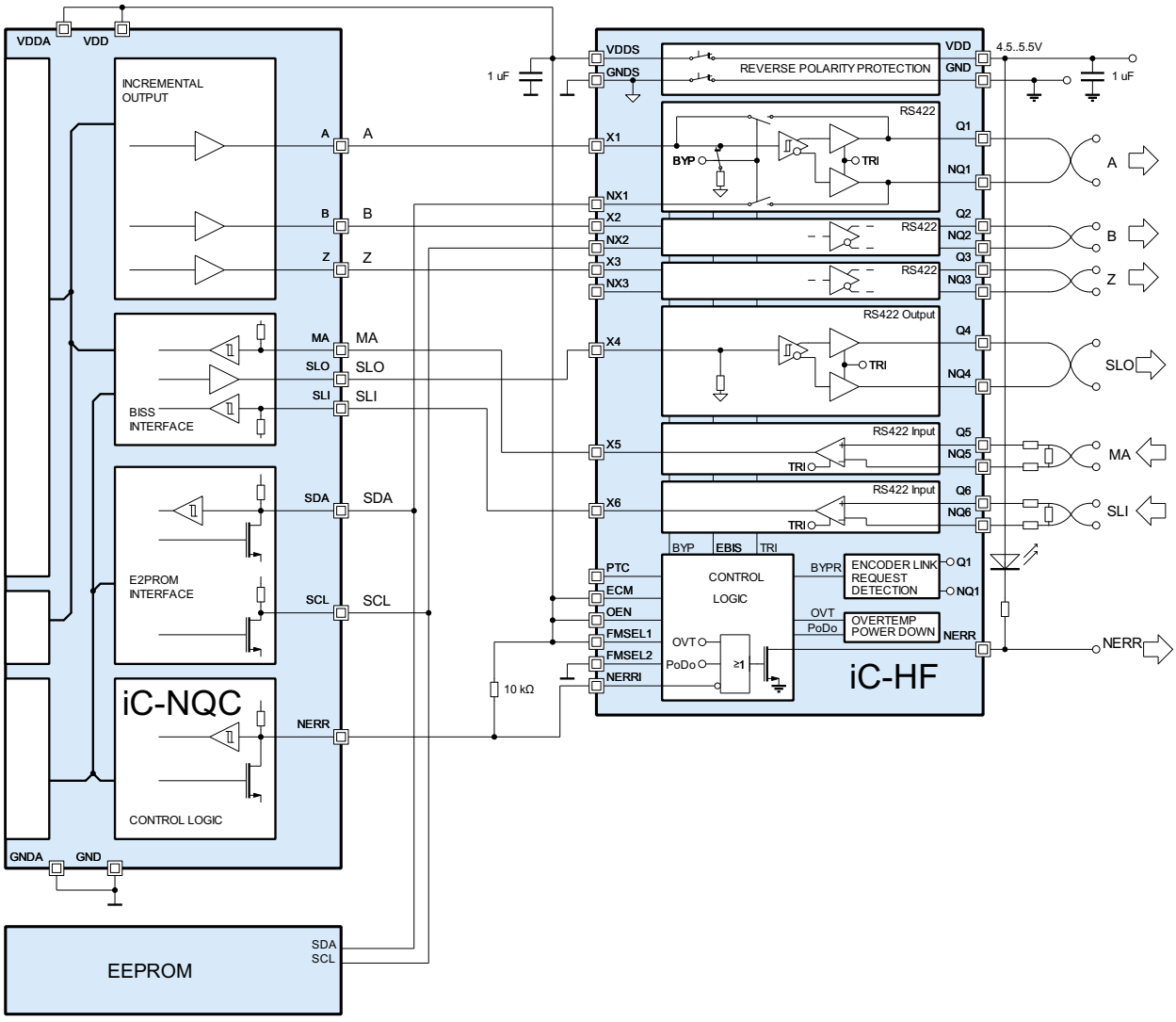


Figure 35: Example application of iC-NQC with iC-HF

ADDITIONAL EXAMPLES

All figures indicate only the basic operation with iC-HF and do not contain all details, connections, configurations and options for a working system.

8 lines encoder operation for ABZ, BiSS and 5 V power supply

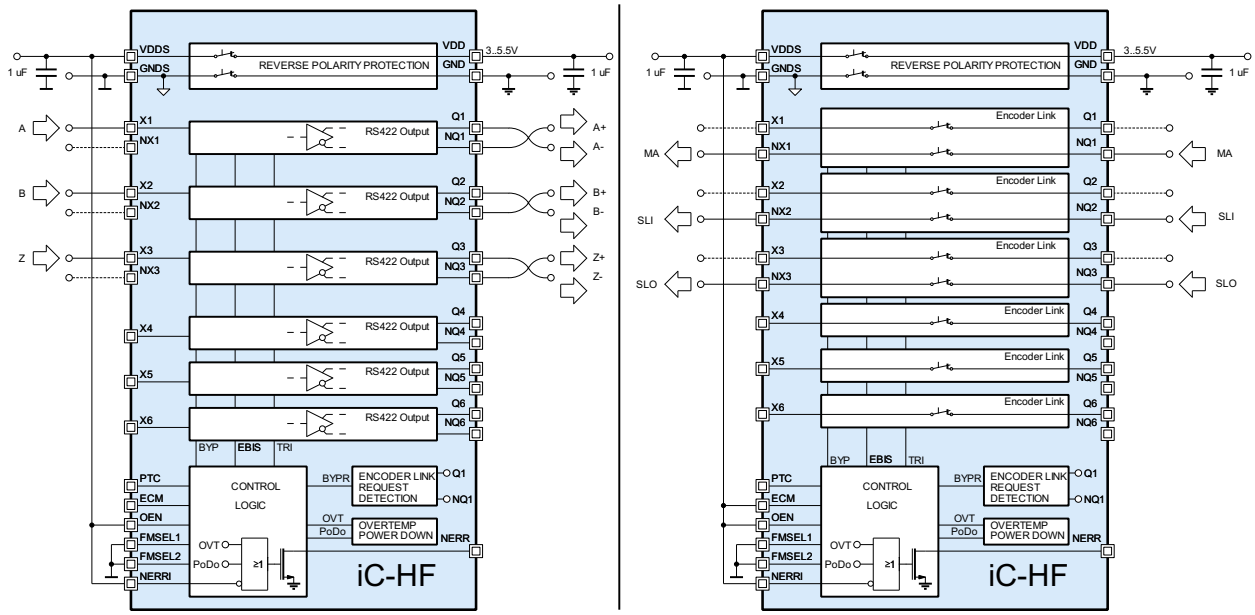


Figure 36: iC-HF with BiSS + A/B/Z using only 8 lines

The left side of figure 36 shows the standard operation of the incremental encoder with differential lines of A+/A-, B+/B-, Z+/Z-, and 5 V power supply. With active *Encoder Link State* figure 36 on the right side showing the *Encoder Link State* operation of the incremental encoder with TTL lines of A, B, Z, BiSS(MA), BiSS(SLI), BiSS(SLO), and 5 V power supply.

The NERR signal is optional and incorporates a sensor's NERR signal and the iC-HF line driver error status.

The SLI signal is only required if the sensor needs to be operated in a *BiSS* bus structure or if MO control is required.

iC-MU with P2P BiSS and iC-HF in Encoder Link State

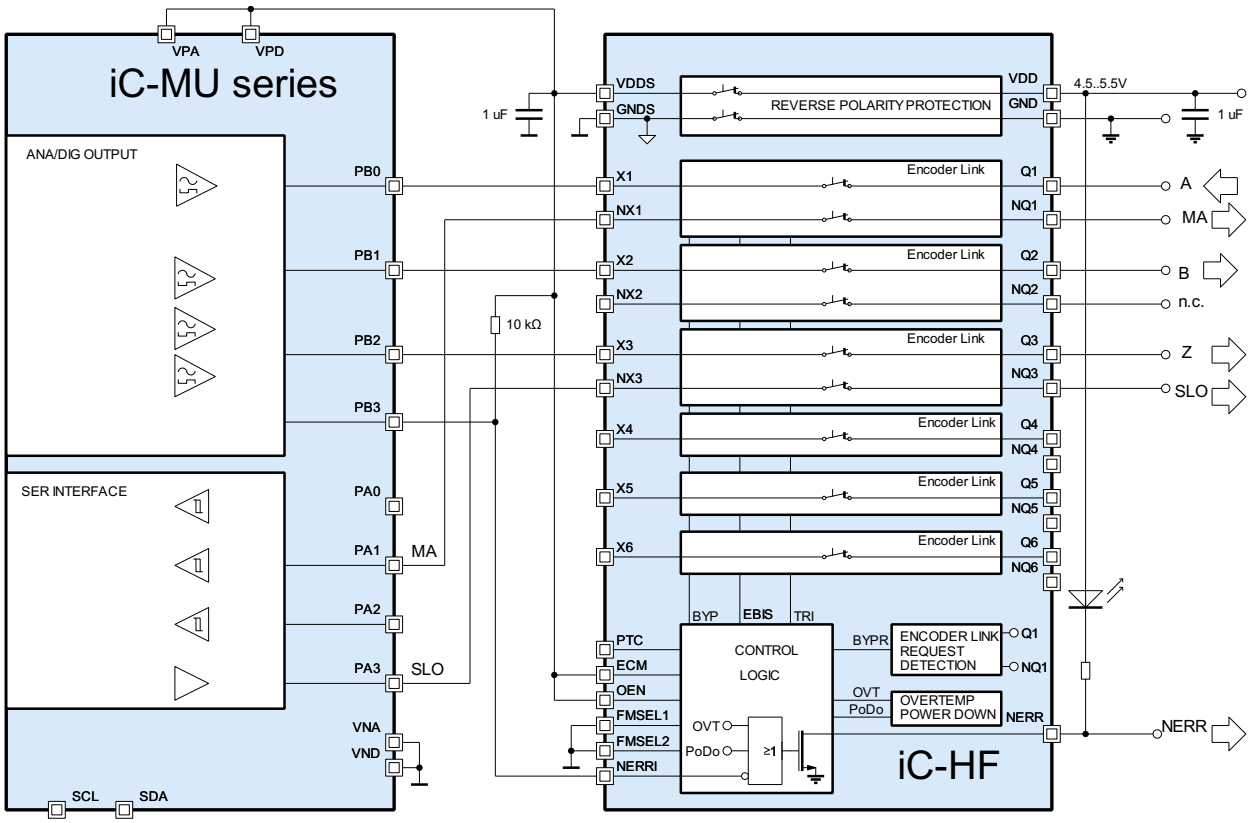


Figure 37: iC-MU with TTL ABZ and TTL BiSS (MA + SLO)

The iC-MU is forced to be operated with BiSS by PA0 to GND.

The iC-MU SLI input can be forced to GND if the BiSS communication is point-to-point.

With active *Encoder Link State* figure 37 shows the *Encoder Link State* operation of the incremental encoder with TTL lines of A, B, Z, BiSS(MA), BiSS(SLO), and 5 V power supply.

The NERR LED signal is optional and incorporates a sensor's NERR signal and the iC-HF line driver error status.

iC-LNB with SPI and iC-HF in Encoder Link State

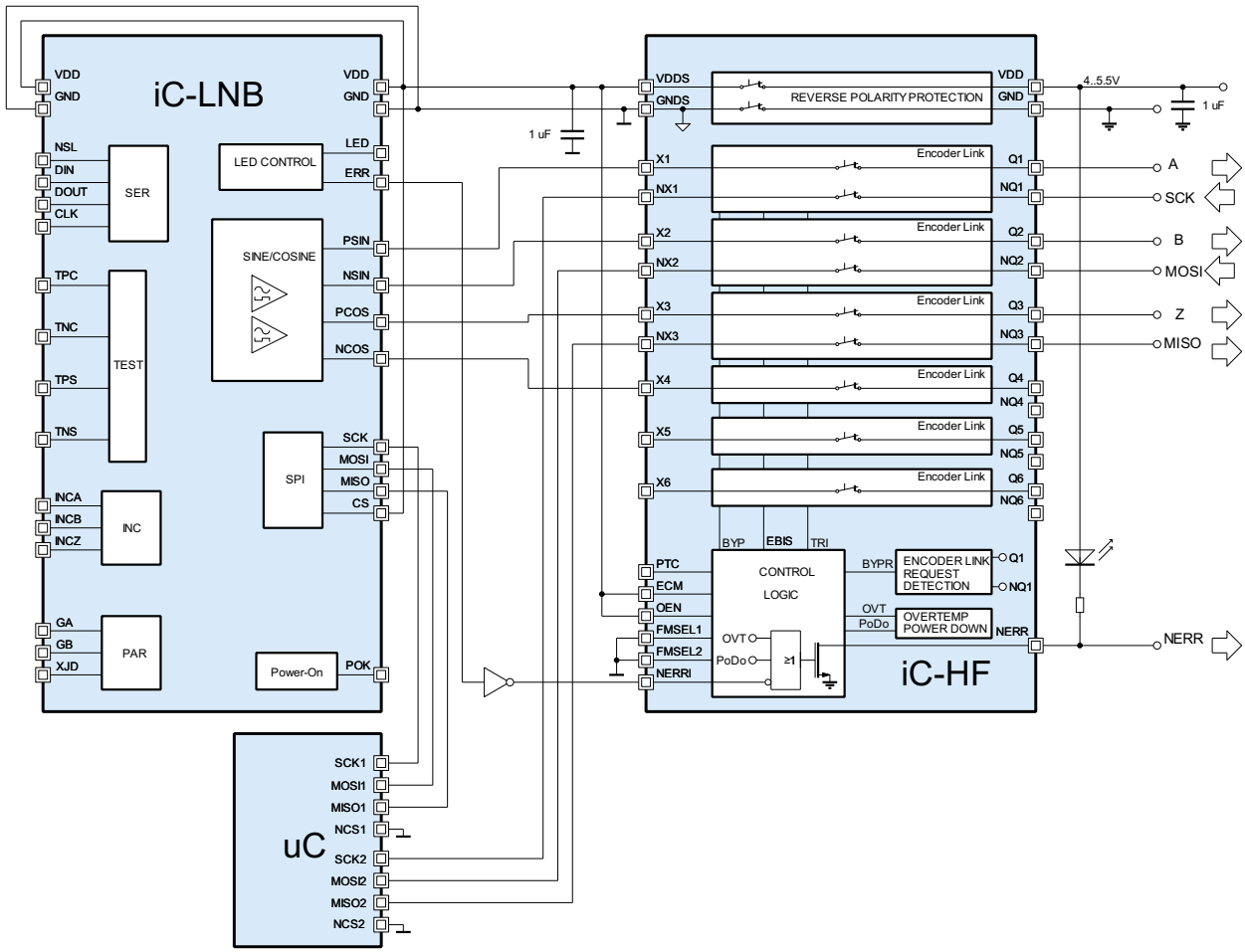


Figure 38: iC-LNB with TTL ABZ and TTL SPI in *Encoder Link State*

The iC-LNB is configured by the sensor's microcontroller via SPI where iC-LNB is the SPI slave and the microcontroller is the SPI master.

The microcontroller and its flash ROM is configured and accessed by an additional 3 wire capable SPI communication where microcontroller is the SPI slave and the external host is the SPI master.

With active *Encoder Link State* figure 38 shows the *Encoder Link State* operation of the incremental encoder with TTL lines of A, B, Z, SPI(CLK), SPI(MISO), SPI(MISO), and 5 V power supply.

The NERR signal is optionally available and incorporates a sensor's NERR signal and the iC-HF line driver error status.

DESIGN REVIEW

iC-HF Y		
No.	Function, parameter/code	Description and application notes
		None at time of release.

Table 11: Notes on chip functions regarding iC-HF chip release Y.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2014-03-21		Initial release.	

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2014-12-10	ABSOLUTE MAXIMUM RATINGS	Item G009: increased from 2 kV to 4 kV	6
		ELECTRICAL CHARACTERISTICS	Item 506: R Termination = 120 Ω added Item 901: Optional C_{PTC} 10nF added	8
		CHANNEL DESCRIPTION	OEN and TRI description added	9
		INTERNAL PROTECTION AND ERROR SIGNALING	Internal signal TRI description added	16
		ENCODER LINK SEQUENCE	Time diagram of the Encoder Link Sequence updated and FMSELx signals removed iC-PT mode control updated and iC-PT H-Series mode control added External capacitor C_{PTC} option added	20, 21
		APPLICATION EXAMPLES	Figure 27 example application of iC-PT/ iC-PT H-Series updated and OTP devices application detail added	25
		Various	TRI added in relevant Figures on pages 1, 9, 11. . . 14, 16. . . 19, 25. . . 35	1. . . 35

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2016-04-08	ELECTRICAL CHARACT.	Item 303: Ilk range updated from ±12 µA to ±35 µA	8
		APPLICATION EXAMPLES	Figure 29: iC-MH16 added Figure 38: updated wiring quadrature encoder application only	27, 36

Rel.	Rel. Date*	Chapter	Modification	Page
D1	2018-05-17	All	Figures updated, blue body	1 . . . 36
		APPLICATION EXAMPLES	iC-MH replaced by iC-MH16	3, 17, 25, 27, 28
		PACKAGING INFORMATION	Thermal Paddle TP renamed to Backside Paddle BP	4
		ELECTRICAL CHARACT.	Item 009, 010 and 011 added	7
		FUNCTION DESCRIPTION	Various Figures updated	12cf
		APPLICATION EXAMPLES	NERRI detail on pull resistor in figures added	26 . . . 33

Rel.	Rel. Date*	Chapter	Modification	Page
D2	2018-10-12	ELECTRICAL CHARACT.	Item 303: symbol updated to Vi(Qx), Vi(NQx)	8
		RS-422 RECEIVER CONFIGURATION	Table 8: Vi updated to Vi(Qx), Vi(NQx) Figure 26 input pins Vi updated to Vi(Qx), Vi(NQx) Note regarding 5 V RS-422 and full RS-422 voltage range added Example layout for RS-422 input receivers added	23, 24
		DESIGN REVIEW	Chapter added	37

Rel.	Rel. Date*	Chapter	Modification	Page
D3	2018-12-21	ENCODER LINK SEQUENCE	Figure 22 and related description updated	21

Rel.	Rel. Date*	Chapter	Modification	Page
D4	2024-12-05	FUNCTION DESCRIPTION	Section Summary of Function Modes added	16
		RS-422 RECEIVER CONFIGURATION	Note box updated for clarity	24
		ABSOLUTE MAXIMUM RATINGS	Item G009, "Reference GNDS" added in parameter Bottom line changed to "All voltages are referenced to pin GND unless otherwise stated."	6
		ELECTRICAL CHARACTERISTICS	Item 012, condition "Vc()lo = V() - V(GNDS)" added	7
		ELECTRICAL CHARACTERISTICS	Item 506, condition "50% Duty Cycle" added	8
		All pages	"preliminary" label removed	all

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-HF	32-pin QFN, 5 mm x 5 mm, thickness 0.9 mm, RoHS compliant		iC-HF QFN32-5x5
Evaluation Board	PCB approx. 80 mm x 100 mm		iC-HF EVAL HF1D

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