iC-WJ, iC-WJZ
LASER DIODE DRIVER

iC·Haus

## FEATURES

♦ Laser diode driver for continuous and pulsed operation (CW to 300 kHz) up to 250 mA

♦ Averaging control of laser power

♦ Simple adjustment of the laser power via external resistor

♦ Adjustable watchdog at the switching input to protect the laser diode

♦ Soft-start after power-on

♦ Driver shutdown with overtemperature and undervoltage

♦ Single 5 V supply

♦ Simple circuitry

♦ **iC-WJ** for laser diodes with 50 to 500 µA monitor current

♦ **iC-WJZ** for laser diodes with 0.15 to 1.5 mA monitor current

APPLICATIONS

♦ General purpose laser diode driver

PACKAGES

SO8   MSOP8

BLOCK DIAGRAM
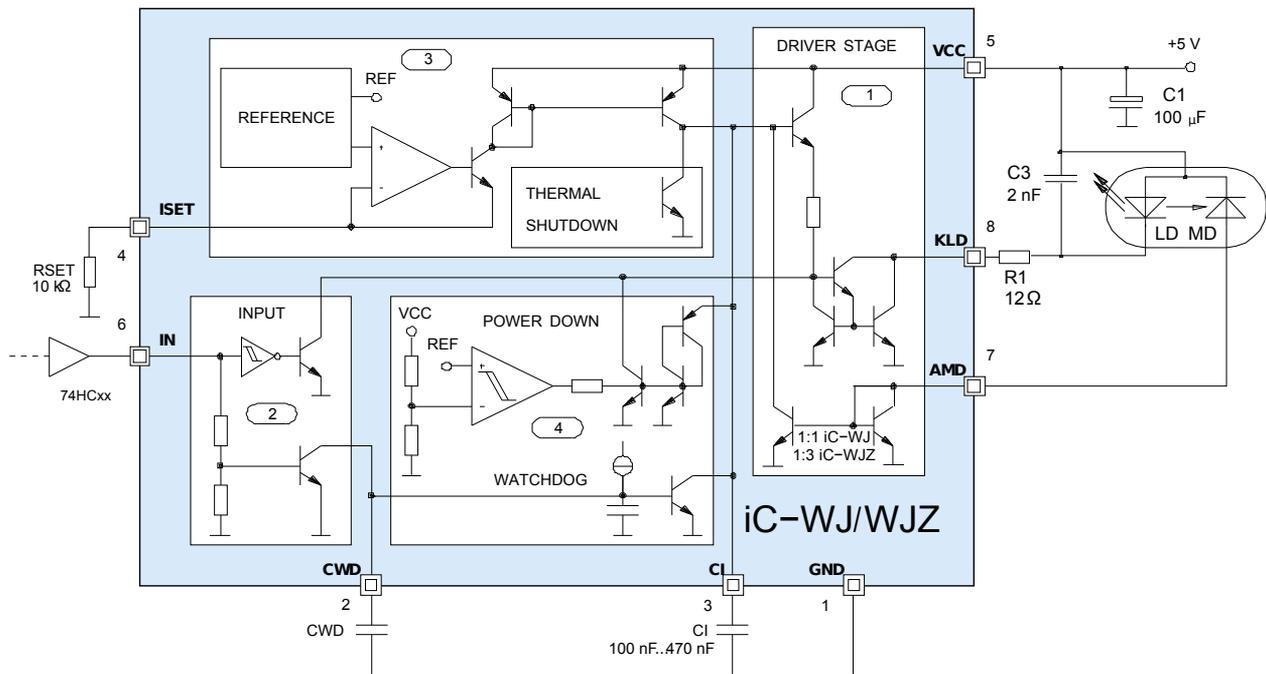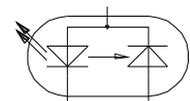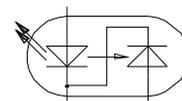
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DESCRIPTION

The iC-WJ and iC-WJZ devices are driver ICs for laser diodes in continuous and pulsed operation up to 300 kHz. The laser diode is activated via switching input IN. A control to the mean value of the optical laser power and integrated protective functions ensure non-destructive operation of the sensitive semiconductor laser.

The IC contains protective diodes to prevent destruction due to ESD, a protective circuit to guard against overtemperature and undervoltage and a soft-start for the laser diode driver to protect the laser diode when switching on the supply voltage.

An external resistor at ISET is utilised to adapt the power control to the laser diode being used. The capacitor at CI determines the recovery time constants and the start-up time.

A watchdog circuit monitors the switching input IN. If IN remains low longer than preset by the capacitor at CWD, the capacitor of the power control is discharged at pin CI. This ensures that the current through the laser diode during the next high pulse at input IN is not impermissibly high.

PACKAGING INFORMATION SO8, MSOP8 to JEDEC Standard

PIN CONFIGURATION SO8

PIN CONFIGURATION MSOP8
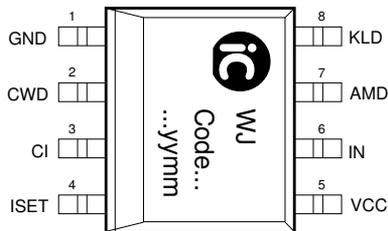
PIN FUNCTIONS

No.	Name	Function
1	GND	Ground
2	CWD	Capacitor for Watchdog
3	CI	Capacitor for Power Control
4	ISET	Attachment for RSET
5	VCC	5 V Supply Voltage
6	IN	Input
7	AMD	Anode Monitor Diode
8	KLD	Cathode Laser Diode
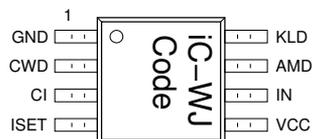
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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Supply Voltage		0	6	V
G002	I(CI)	Current in CI		-4	4	mA
G003	V(KLD)	Voltage at KLD	IN = lo	0	6	V
G004	I(KLD)	Current in KLD	IN = hi	-4	600	mA
G005	I(AMD)	Current in AMD	**iC-WJ** **iC-WJZ**	-4 -6	4 6	mA mA
G006	I(IN)	Current in IN		-10	2	mA
G007	I(ISET)	Current in ISET		-2	2	mA
G008	I(CWD)	Current in CWD	IN = lo	-2	2	mA
G009	Vd()	ESD Susceptibility at CWD, CI, ISET, IN, AMD, KLD	MIL-STD-883, HBM 100 pF discharged through 1.5 kΩ		1.5	kV
G010	Tj	Junction Temperature		-40	150	°C
G011	Ts	Storage Temperature		-40	150	°C

THERMAL DATA

Operating Conditions: VCC = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended temperature range on request)		-25		90	°C
T02	Rthja	Thermal Resistance Chip to Ambient	surface mounted on PCB, without special cooling			140	K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

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ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 5 V ±10 %, RSET = 2.7...27 kΩ,
iC-WJ: I(AMD) = 50...500 µA, **iC-WJZ**: I(AMD) = 0.15...1.5 mA, Tj = -25...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VCC	Permissible Supply Voltage Range				4.5		5.5	V
002	Iav(VCC)	Supply Current in VCC (average value)	Iav(KLD) = 100 mA, f(IN) = 200 kHz ±20 %					15	mA
003	tp(IN-KLD)	Delay Time Pulse Edge V(IN) to I(KLD)	IN(hi ↔ lo), V(50 %) : I(50 %)					135	ns
004	Vc()lo	Clamp Voltage lo at VCC, IN, AMD, KLD, CI, CWD, ISET	I() = -2 mA, other pins open			-1.5		-0.3	V
005	Vc()hi	Clamp Voltage hi at IN, AMD, KLD, GND, CI, CWD, ISET	Vc()hi = V() − VCC; I() = 2 mA, other pins open			0.3		1.5	V
Driver									
101	Vs(KLD)	Saturation Voltage at KLD	IN = hi, I(KLD) = 200 mA					1.3	V
102	I0(KLD)	Leakage Current in KLD	IN = lo, V(KLD) = VCC					10	µA
103	I(KLD)	Current in KLD	IN = hi, I(AMD) = 0	-25 27 70 125		225 250 250 250	250		mA mA mA mA
104	V(AMD)	Voltage at AMD	**iC-WJ:** I(AMD) = 500 µA **iC-WJZ:** I(AMD) = 1.5 mA			0.5 0.4		1.5 1.5	V V
105	tr	Current Rise Time in KLD	Imax(KLD) = 20...250 mA, Ip(): 10 → 90 %					100	ns
106	tf	Current Fall Time in KLD	Imax(KLD) = 20...250 mA, Ip(): 90 % → 10 %					100	ns
107	CR1()	Current Ratio I(AMD) / I(ISET)	I(CI) = 0, closed control loop; **iC-WJ** **iC-WJZ**			0.8 2.4	1 3	1.2 3.6	
108	CR2()	Current Ratio I(AMD) / I(CI)	V(CI) = 1...3.5 V, ISET open; **iC-WJ** **iC-WJZ**			0.9 2.7	1 3	1.1 3.3	
Input IN									
201	Vt()hi	Threshold hi		-25 27 70 125		1.60	1.84 1.87 1.88 1.91	2.40	V V V V V
202	Vt()lo	Threshold lo		-25 27 70 125		1.50	1.76 1.78 1.79 1.81	2.20	V V V V V
203	Vt()hys	Hysteresis		-25 27 70 125		10	80 90 90 100	190	mV mV mV mV mV
204	Rin	Pull-Down Resistor	V(IN) = -0.3...VCC + 0.3 V			4		16	kΩ
205	V0()	Open-loop Voltage	I(IN) = 0					0.1	V
206	Vtwd()	Threshold for Watchdog		-25 27 70 125		2.4 2.0 1.5 1.0		3.2 2.8 2.3 1.8	V V V V
Reference und Thermal Shutdown									
301	V(ISET)	Voltage at ISET		27		1.17	1.22	1.28	V V
302	CR()	Current Ratio I(CI) / I(ISET)	V(CI) = 1...3.5 V, I(AMD) = 0			0.9	1	1.1	

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ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 5 V ±10 %, RSET = 2.7...27 kΩ,
iC-WJ: I(AMD) = 50...500 µA, **iC-WJZ**: I(AMD) = 0.15...1.5 mA, Tj = -25...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
303	RSET	Permissible Resistor at ISET (Control Set-up Range)				2.7		50	kΩ
304	Toff	Thermal Shutdown Threshold				125		150	°C
305	Thys	Thermal Shutdown Hysteresis				10		40	°C
Power-Down and Watchdog									
401	VCCon	Turn-on Threshold VCC		27		3.5	3.8	4.3	V V
402	VCCoff	Undervoltage Threshold at VCC				3.2		3.8	V
403	VCChys	Hysteresis	VCChys = VCCon − VCCoff	27		300	400	450	mV mV
404	Vs(CI)off	Saturation Voltage at CI with undervoltage	I(CI) = 300 µA, VCC < VCCoff					1.6	V
405	Vs(CI)wd	Saturation Voltage at CI with IN = Io	I(CI) = 300 µA, t(IN = Io) > tp [*]					1.5	V
406	Ipu(CWD)	Pull-Up Current at CWD	V(CWD) = 0, IN = Io			-15		-3	µA
407	tpmin	Min. Activation Time for Watchdog	IN = Io, CWD open			10			µs
408	Kwd [*]	Constant for Calculating the Watchdog Activation Time	IN = Io			0.19	0.38	0.57	µs/pF

[*] tp = (C(CWD) ∗ Kwd) + tpmin   (see Applications Information)

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APPLICATIONS INFORMATION

Laser Power Adjustment
The iC-WJ and iC-WJZ devices can be adapted to CW laser diodes from approximately 2 to 40 mW. N- and M-type models can be used.

The pin ISET is used for the adjustment to the sensitivity of the monitor diode and to set the desired optical laser power. The setpoint for the averaging control of the monitor diode current is preset at this pin.
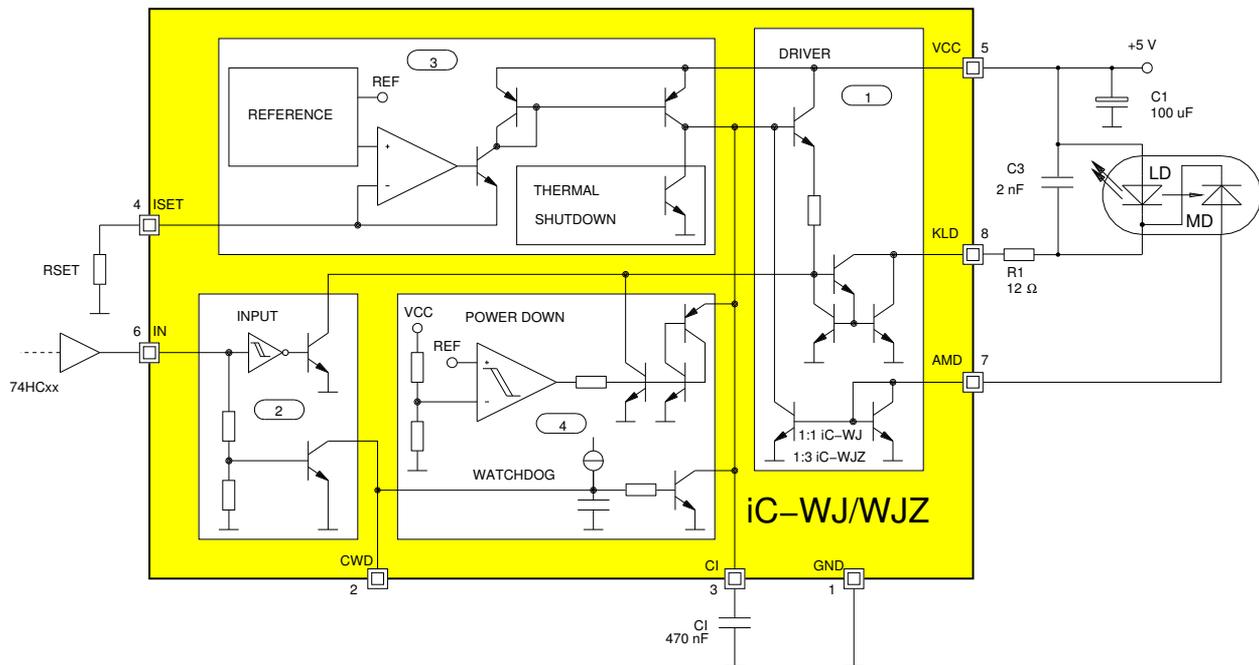
Figure 1: Operation of a laser diode according to the example

To calculate the current required at ISET, the average optical laser power is to determine:

$$P_{av} = P_{peak} * \frac{t_{whi}}{T}$$

with peak value P_{peak} and pulse/period duration t_{whi}/T.
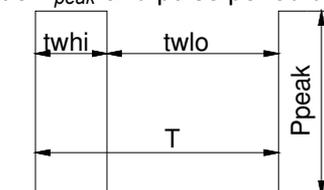
Figure 2: Duty cycle

Example iC-WJ
Laser diode with 5 mW maximum optical output, monitor diode with 0.13 mA/mW, pulse duty factor set to 20 % with P_{peak} = 5 mW:

The resulting average optical power is 1 mW and the average monitor diode current is 0.13 mA. The resistor RSET is calculated as:

$$RSET = \frac{CR1 * V(ISET)}{I_{av}(AMD)} = \frac{1 * 1.22\,V}{0.13\,mA} = 9.4\,k\Omega$$

with the Electrical Characteristics No. 301 for V(ISET) and No. 108 for current ratio CR1.

Example iC-WJZ
Laser diode with 5 mW maximum optical output, monitor diode with 0.75 mA at 3 mW, CW operation (pulse duty factor 100 %) with P_{cw} = 1 mW:

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For the monitor diode current of 0.25 mA the resistor RSET is calculated as:

$$RSET = \frac{CR1 * V(ISET)}{I_{av}(AMD)} = \frac{3 * 1.22\,V}{0.25\,mA} = 14.6\,k\Omega$$

with Electrical Characteristics No. 301 for V(ISET) and No. 108 (iC-WJZ) for current ratio CR1.

Averaging control
The control of the average optical laser power requires a capacitor at pin CI. This capacitor is used for averaging and must be adjusted to the selected pulse repetition frequency and the charging current preset with RSET. The ratios are linear in both cases, i.e. the capacitor CI must be increased in size proportionally as the pulse repetition frequency slows or the current from ISET increases:

$$CI \geq \frac{440 * I(ISET)}{f * V(ISET)} = \frac{440}{f * RSET}$$

Example
Pulse repetition frequency 100 kHz, RSET = 10 kΩ: CI = 440 nF, chosen 470 nF.

Otherwise the charging of the capacitor CI during the pulse pauses (with I(ISET) = 1.22 V / RSET) will create an excessive mean value potential and may destroy the laser diode during the next pulse. The capacitor CI is correctly dimensioned when the current through the laser diode and the optical output signal do not show any overshots following the rising edge.
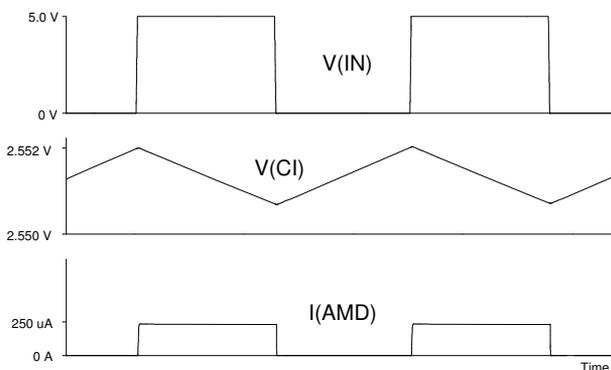
Figure 3: Steady-state averaging control, f(IN) = 100 kHz (1:1), CI = 470 nF, RSET = 10 kΩ

In steady-state condition and for a pulse duty factor of 50 % (pulse/pause 1:1), signals as shown in Figure 3 are present at the IC pins.

Figure 4 shows the corresponding signals for a pulse duty factor of 20 %. The influence of the pulse duty factor on the peak value of the monitor current proportional to the laser current is apparent. The average kept constant by the control (RSET unchanged) means a peak value increased by the factor 2.5. The pulse duty factor for which RSET was dimensioned should therefore be kept constant if possible.
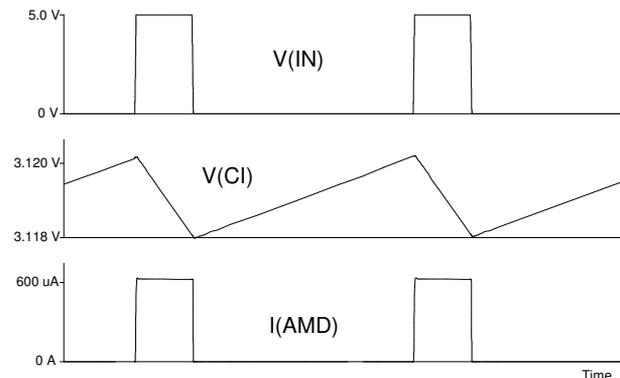
Figure 4: Steady-state averaging, f(IN) = 100 kHz (1:4), CI = 470 nF, RSET = 10 kΩ
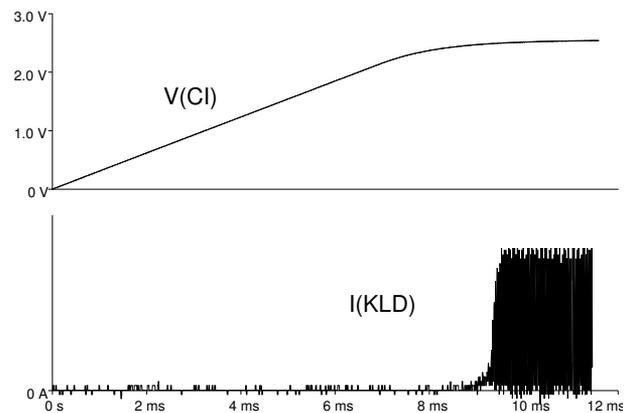
Figure 5: Turn-on behavior, f(IN) = 100 kHz (1:1), CI = 470 nF, RSET = 10 kΩ

Turn-on and turn-off behavior
Capacitor CI also determines the starting time from switching on the supply voltage VCC to steady-state laser pulse operation or after a discharge of CI by the watchdog. The following applies to estimating the starting time (Figure 5):

$$T_{on} = \frac{2.5\,V * CI}{I(ISET)} = \frac{2.5\,V * CI * RSET}{1.22\,V}$$

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Example

CI = 470 nF, RSET = 10 kΩ: T_{on} = 9.6 ms

Figure 6 shows a detailed view of the start of laser operation; Figure 7 shows the shut-down behavior. The decline in the voltage at CI and the absence of the laser pulses are signs that the undervoltage detector is active.
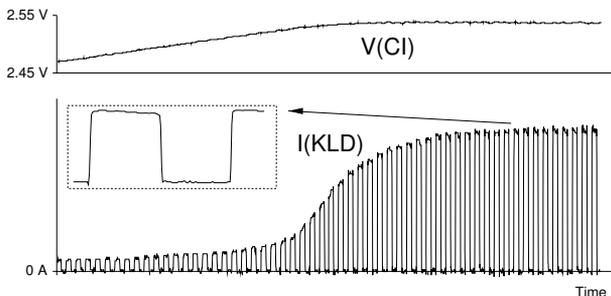

Figure 6: Turn-on behavior, detailed view f(IN) = 100 kHz (1:1), CI = 470 nF, RSET = 10 kΩ
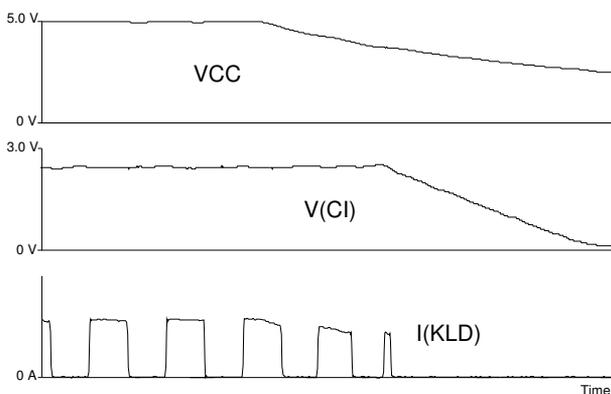
Figure 7: Turn-off behavior, f(IN) = 100 kHz (1:1), CI = 470 nF, RSET = 10 kΩ

Watchdog

In order for the watchdog to function correctly, the input IN must be activated with a CMOS output (e.g. with an HCMOS gate: see Figure 1).

The watchdog ensures that the capacitor CI is discharged during protracted pulse pulses at IN. During the pulse pauses the potential at CI increases by ΔV (Figure 3):

$$\Delta V = \frac{I(ISET) * t_{wlo}}{CI}$$

The discharge of capacitor CI by the watchdog protects the laser diode from being destroyed by an excessive turn-on current during the next pulse.

The capacitor CWD should be dimensioned such that the response time t_p of the watchdog is slightly longer than the pulse pause t_{wlo} of the input signal. As a result, the watchdog is just short of being activated.

For response times t_p longer than t_{pmin} applies:

$$CWD = \frac{t_p - t_{pmin}}{K_{wd}}$$

with t_{pmin} and K_{wd} from Electrical Characteristics No. 407, 408.
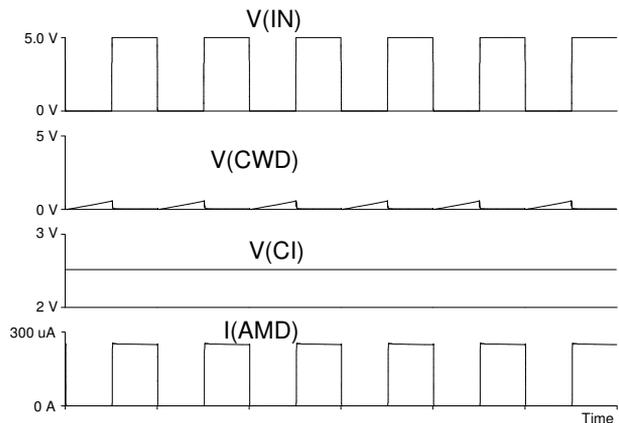
Figure 8: Watchdog, CWD open, f(IN) = 100 kHz (1:1), CI = 470 nF, RSET = 10 kΩ
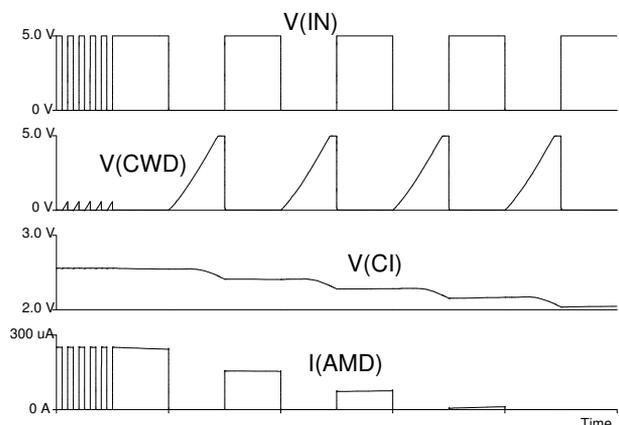
Figure 9: Watchdog, CWD open, f(IN) = 100 kHz → 10 kHz (1:1), CI = 470 nF, RSET = 10 kΩ

Figure 8 shows the signals during normal operation, without the watchdog being activated. The potential at CWD rises during pulse pauses but does not reach the watchdog activation threshold.

Figure 9 shows the watchdog behavior when the input frequency is reduced from 100 kHz to 10 kHz. The pulse pauses are longer than the watchdog's response

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time. The watchdog begins to discharge the capacitor CI current limited. The remaining charge time during the pulse pauses before further watchdog intervention is not sufficient to maintain the initial potential at CI. The potential is thus gradually reduced until it reaches the saturation voltage $Vs(CI)_{wd}$ (Electrical Characteristics No. 405).

The watchdog therefore protects the laser diode from destruction when the input signal change in such a manner that the capacitor CI is not longer adequate for averaging.

Furthermore, the introduction of the watchdog permits long pulse pauses and activation of the laser diode with pulse packets.
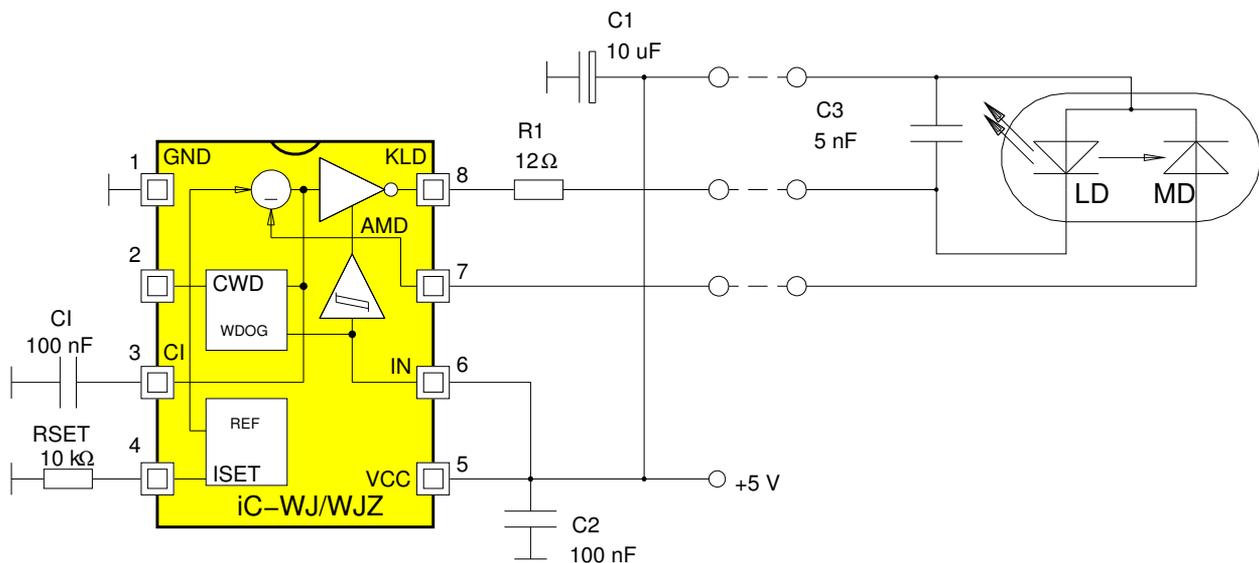
Figure 10: CW operation via cable

CW Operation
In case of CW operation, the input IN can be connected to the power supply VCC. The pin CWD may be left open, because the capacitor for the watchdog is not necessary. The capacitor CI for the averaging control can be reduced to 100 nF.

Operation of laser diode via cable
It is recommended to connect a capacitor of 1 to 10 nF across the laser diode in order to protect the laser diode against destruction due to ESD or transients. This capacitor should be placed close to the laser diode and not at the beginning of the LD supply line.

An approx. $12\,\Omega$ series resistor at pin KLD reduces the IC power consumption and damps possible resonances of the load circuit caused by the inductive LD supply line. This resistor is useful for many applications, also for those which do not operate via cable.

On a PCB the forward path VCC to the laser diode should be arranged in parallel with the return path to KLD even when the line is only a few centimeters in length.

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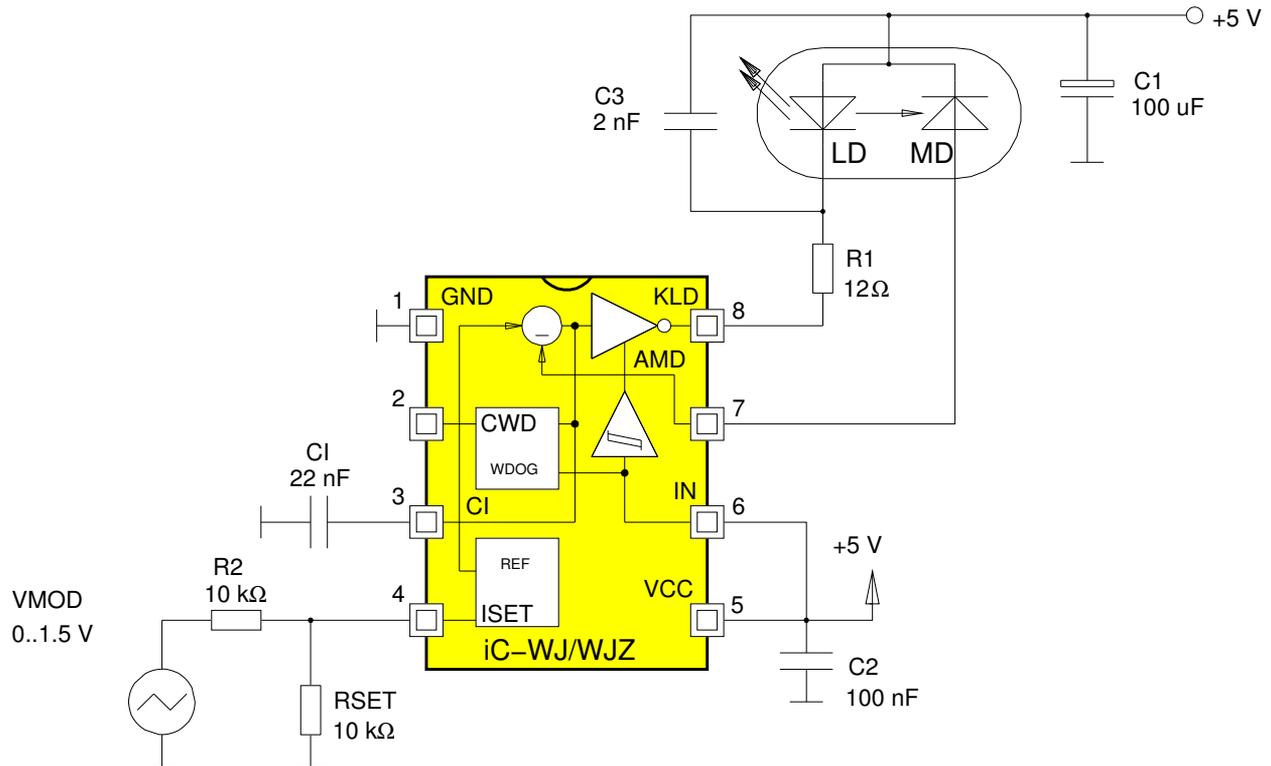
Figure 11: Analogue modulation during CW operation

Analogue modulation during CW operation

The modulation cut-off frequency is determined by the capacitor CI as well as by the operating point set with the resistor RSET. With CI = 100 nF and RSET = R2 = 10 kΩ the cut-off frequency is approx. 40 kHz, with CI = 22 nF and the same resitor value of about 230 kHz.

The laser power can also be modulated by adapting a current source, e.g. by using an operational amplifier with a current output (OTA). To limit the current at pin ISET while turning on the power supply for the OTA circuitry, however, RSET should be connected to the OTA output (instead of to GND). The maximum current possible at ISET must be taken into consideration when dimensioning the capacitor CI.

PC board layout

The ground connections of the external components CI, CWD and RSET have to be directly connected at the IC with the GND terminal.

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DEMO BOARD

For the devices iC-WJ/WJZ/WJB a Demo Board is available for test purposes. The following figures show the schematic diagram and the component side of the test PCB.
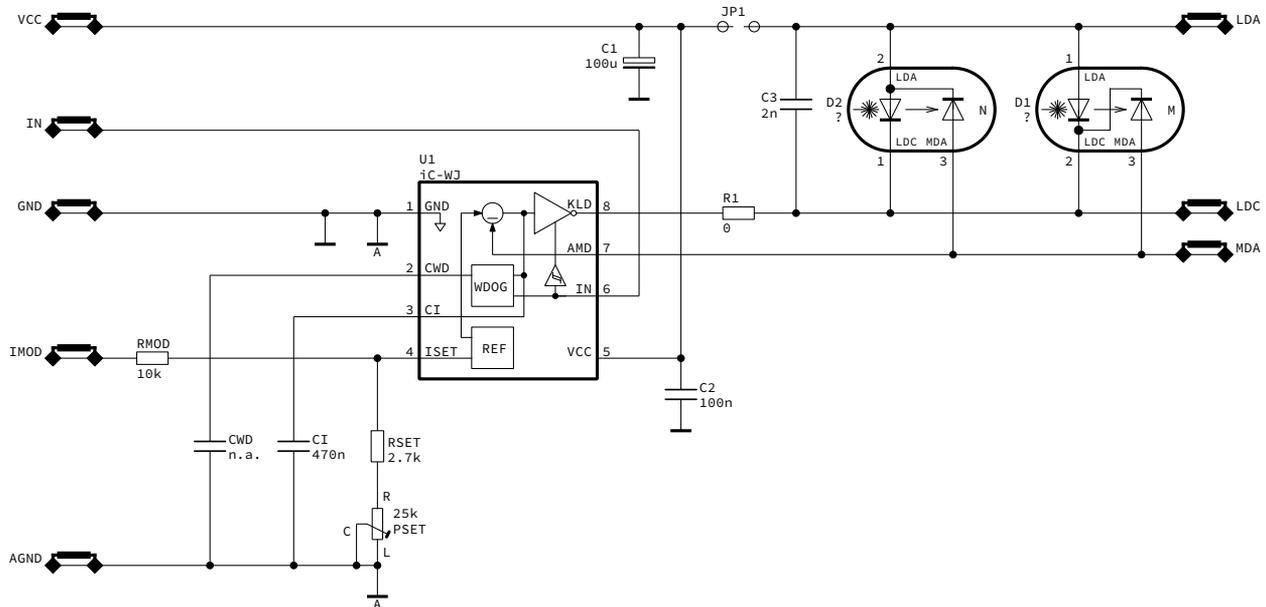
Figure 12: Schematic diagram of the Demo Board
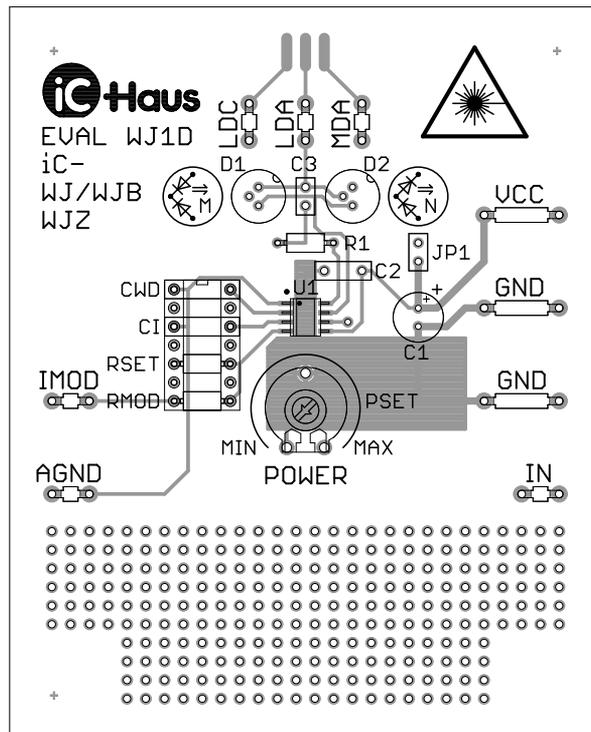
Figure 13: Demo Board (components side)

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
C2	2018-07-05	DEMO BOARD	New demo board	11

* Release Date format: *YYYY-MM-DD*

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ORDERING INFORMATION

Type	Package	Order Designation
iC-WJ	SO8	iC-WJ SO8
iC-WJ	MSOP8	iC-WJ MSOP8
WJ Evaluation Board		iC-WJ EVAL WJ1D
iC-WJZ	SO8	iC-WJZ SO8
iC-WJZ	MSOP8	iC-WJZ MSOP8
WJZ Evaluation Board		iC-WJZ EVAL WJ1D

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