iC213
PROGRAMMABLE OSCILLATOR MODULE

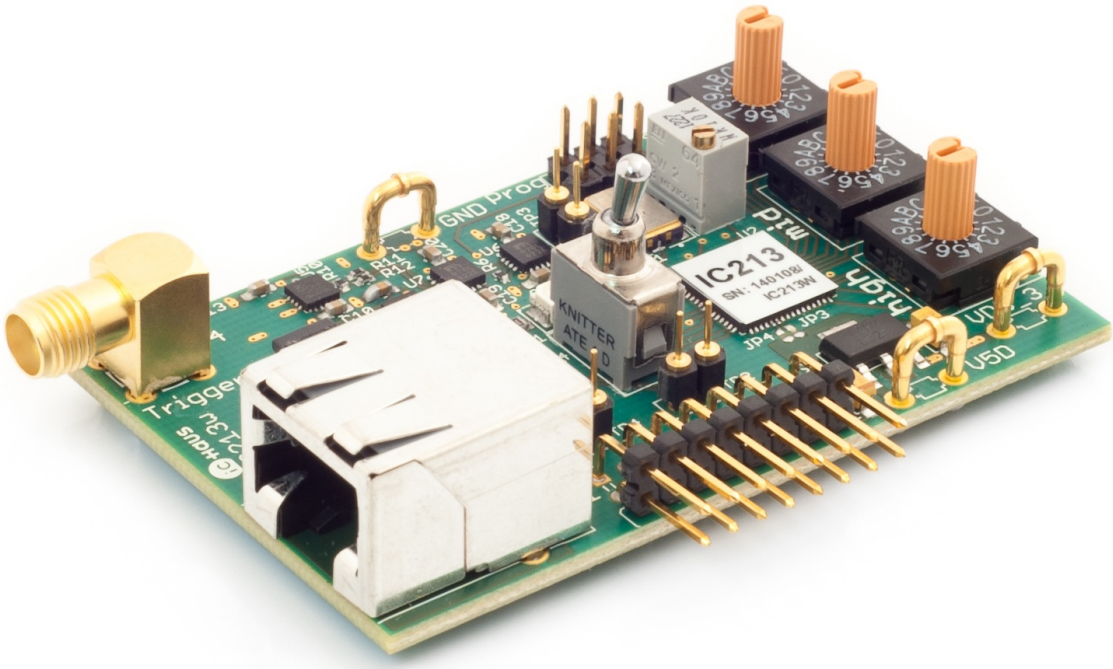
FEATURES

- 40 kHz to 1.4 GHz with 50% duty cycle
- LVDS und TTL outputs
- Compatible with HG1D, HG2D, NZN1D, NZP1D, iC245, ...

APPLICATIONS

- Pulse generator for laser diode drivers

BOARD



DESCRIPTION

The core of the iC213 module is a via I²C programmable oscillator device. To program the frequency, 8 internal 8 bit registers have to be set accordingly. On the iC213 module an ATMega128 micro-controller performs this task.

A selection of 4096 preset frequencies between 39.3 kHz and 1 GHz can be set by means of three HEX switches. A list of these frequencies to choose from is given in the chapter *Selectable Frequencies*.

Using the I²C interface to select a frequency, either one of the 4096 preset frequencies or an arbitrary frequency from 39.0625 kHz to 945 MHz, 970 to 1134 MHz and 1213 to 1417.5 MHz can be programmed.

Switch SW4 enables/disables the iC213 module, as does the NE_OSC pin.

This module is pin compatible to the ns-pulse generator module iC149.

The iC213 module can be used as input for the pulse-width modifier module iC245.

ELECTRICAL CHARACTERISTICS

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	Vs	Supply Voltage	referenced to GND	4.5		5.5	V
002	Is	Current Consumption			460		mA
003	Is_{NEN}	Current Consumption	Oscillator disabled		420		mA
I^2C Interface							
101	V_{IH}	Input Low Level		-0.5		0.3 ∗ Vs	V
102	V_{IL}	Input High Level		0.7 ∗ Vs		Vs + 0.5	V
103	V_{OL}	Output LowLevel	3 mA load current	0		0.4	V
104	t_r	Rise Time at SDA, SCL				300	ns
105	t_{OF}	Fall Time at Output	$V_{IH_{min}} \Rightarrow V_{IL_{max}}$			250	ns
106	t_{SP}	Spikes suppress by input filter		0		50	ns
107	f_{Max}	Maximum Bus Frequency				400	kHz
LVTTL-/LVCMOS Outputs							
201	V_{TTL_L}	Low Level			0.1	0.4	V
202	V_{TTL_H}	High Level		2.7	3.2		V
203	t_{tr}, t_{tf}	Rise/Fall time	10 % until 90 %		350	800	ps
204	f_{max}	Maximum Frequency		250	300		MHz
LVDS Outputs							
301	V_{OUT}	Output Swing	100 Ω temination	250	325		mV
302	V_{DIF_OUT}	Differential Output Swing	100 Ω temination	500	650		mV
303	V_{OCM}	Common Mode Output Voltage		1.125		1.275	V
304	t_r, t_f	Rise/Fall time	10 % until 90 %, full swing		170	270	ps
Trigger Output							
401	V_{TOL}	Low Level	50 Ω temination	80	200		mV
402	V_{TOH}	High Level	50 Ω temination		580	890	mV
403	t_{tr}, t_{tf}	Rise/Fall time	10 % until 90 %		250	280	ps
Programmable Frequency Range							
501	f_{OUT}	Frequency	LVDS Outputs, HEX Switch	39.3 970k		944k 1000k	kHz kHz
502	$f_{OUT'}$	Frequency	LVDS Outputs, I^2C programming	39.0625 970k 1213k		945k 1134k 1417.5k	kHz kHz kHz

PIN CONFIGURATION

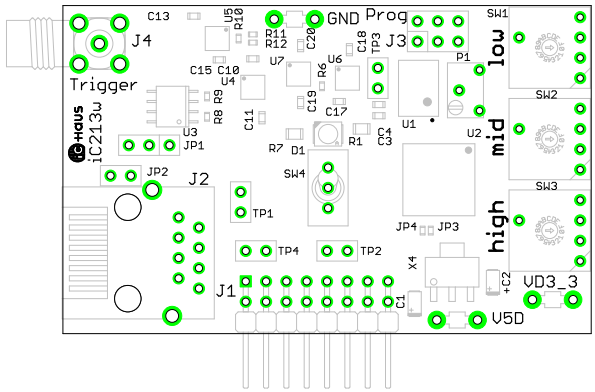


Figure 1: The populated PCB

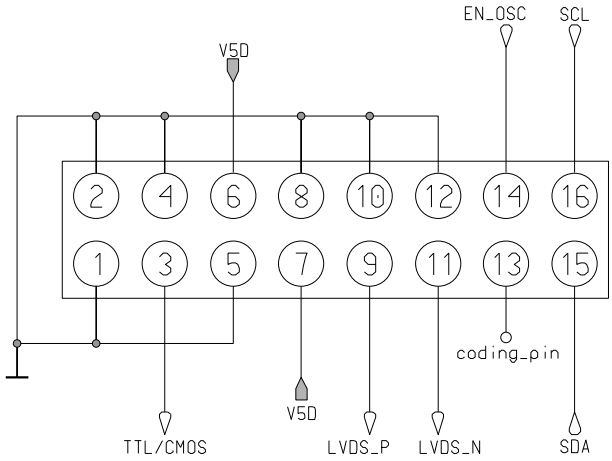


Figure 2: Pin configuration J1 (PCB bottom view)

J1	16 pole pin header for power supply and signal outputs
J2	RJ45 connector for output signals with LVDS or TTL/CMOS levels
J3	reserved
J4	TRIGGER: SMA connector for trigger output, Rout = 50 Ω
JP1	Jumper at position 1-2 selects TTL/CMOS signals for J2
JP2	Connects RJ45 Shield (J2) to GND
JP3/JP4	Selects I^2C Address, see section Programming via I^2C
SW1	Frequency coding switch low (Bit 0-3)
SW2	Frequency Coding switch mid (Bit 4-7)
SW3	Frequency Coding switch high (Bit 8-11)
SW4	Oscillator ON/OFF
TP1	LVDS signal at J2 (must be terminated with 100 Ω for measurement purpose)
TP2	LVDS signal at J1 (must be terminated with 100 Ω for measurement purpose)
TP3	LVDS clock signal at U1 digital oscillator output (for reference only)
TP4	TTL/CMOS signal at J1
P1	Trimmer for fine tuning the frequency
D1	Oscillator ON/OFF indication
GND	GND
V5D	5 V Power supply
VD3_3	3.3 V

Table 1: Connectors on the PCB

LVDS AND TTL OUTPUTS

The clock signal is supplied to J1 both as LVDS and TTL signals. Additionally it is supplied to J2, the RJ45 plug, also both as LVDS and TTL signals. The TTL signal at J2 can be enabled/disabled by means of jumper JP1.

The output of the core oscillator is LVDS level. To be able to set lower frequencies than the lowest oscillator frequency of 10 MHz two downstream LVDS frequency dividers are used. These are cascaded in a way so that the division factor can be set in three steps between 1, 64 and 256. Thus frequencies down to 39.0625 kHz can be programmed.

These dividers are set automatically when choosing from the predefines frequencies. Though they can also be programmed manually via the I^2C interface.

An additional fan-out buffer distributes the LVDS signal to the four outputs (2 x TTL, 2 x LVDS) of the module. The TTL signals are generated by two LDVS/TTL converters. Since the operating frequency of these converters is limited to 300 MHz, the TTL outputs should only be used up to this frequency. For higher frequencies only the LVDS outputs should be used. The LVDS outputs must be differentially terminated with 100 to 110 Ω.

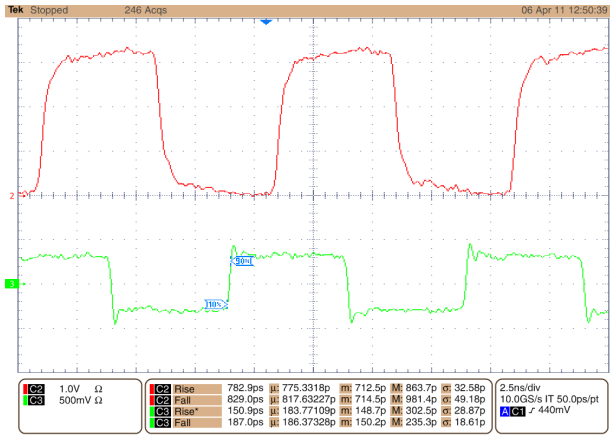


Figure 3: Channel 2 (red) TTL output, Channel 3 (green) LVDS Output

ENABLE INPUT

Via the input EN_OSC the output of the module can be enabled/disabled. This input is high active and features an internal pull-up resistor. That means, connecting this input to GND (low level) disables the outputs. With an unconnected input EN_OSC the outputs are enabled. Switch SW4 performs the same function.

TRIGGER

An SMA connector on the modules serves as a trigger source e.g. for an oscilloscope. This connector supplies the programmed clock signal. The internal resistance of the trigger source is 50 Ω. Hence the connected cable should have a characteristic wave impedance of 50 Ω and be terminated also with a 50 Ω resistor. The signal amplitude will then be about 200 to 600 mV.

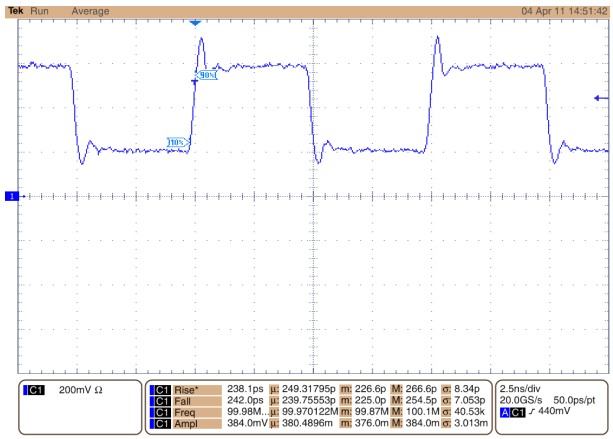


Figure 4: Channel 1 (blue) trigger signal with 100 MHz

SETTING THE FREQUENCY

Using the I²C interface arbitrary output frequencies in the range 39.0625 kHz to 1417.5 MHz can be programmed. The intrinsic oscillator allows frequencies in the ranges of 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417.5 MHz to be programmed.

To this end the oscillator utilises a so called DCO (*Digitally Controlled Oscillator*), consisting of a reference clock oscillator with f_{XTAL} and a multiplier R_{FREQ} following a high-speed divider HS_DIV as well as the output divider N1:

$$f_{out} = \frac{f_{XTAL} * RFREQ}{HS\_DIV * N1}$$

f_{out} Ouptut Frequency
f_{XTAL} Reference Clock (= 114,3363533 MHz)
HS_DIV High-Speed Divider
N1 Output Divider N1
RFREQ Multiplier

Using a PLL the reference clock in the DCO is multiplied with RFREQ. The operating frequency of this PLL is between 4.85 and 5.67 GHz. The thus generated RF signal is divided by means of the high-speed divider HS_DIV and further reduced by divider N1 to the required output frequency.

RFREQ
RFREQ it the multiplier for the *Digitally Controlled Oscillator*. Multiplying it with the referential clock f_{XTAL} = 114.3363533 MHz yields the output frequency of the DCO. Hence the multiplier RFREQ is determined as follws:

$$f_{DCO} = f_{XTAL} * RFREQ$$

$$\Rightarrow RFREQ = \frac{f_{DCO}}{f_{XTAL}}$$

f_{DCO} DCO Output Frequency
f_{XTAL} Reference Clock (= 114.3363533 MHz)
RFREQ Multiplier

RFREQ is a 38 bit number with the upper 10 Bit representing the digits to the left of the decimal point and the lower 28 bit the digits to the right of the decimal point.

Example: RFREQ = 02E0B04CE0

Hex	02E	0B04CE0
Binary	00 0010 1110	0000 1011 0000 0100 1100 1110 0000
	46	: 2^{28}
		0,043042064
Decimal	46,043042064	

Table 2: RFREQ Conversion

HS_DIV
The high-speed divider is coded as a 3 bit digit as shown in Table 3.

HS_DIV[2:0]			Divider
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	not used
1	0	1	9
1	1	0	not used
1	1	1	11

Table 3: Values for HS_DIV

N1
The output divider N1 only allows even values between 1 and 128 to be set, except for the division factor 1. N1 calculates as:

$$Value\ in\ the\ register\ N1 = Divider\ N1 - 1$$

So to set a division factor of e.g. 10, 0001001b (decimal 9) must be programmed.

N1[6:0]	Divider
0000000	1
0010011	36
1111111	128

Table 4: Values for output divider N1

Example
A frequency of 100 MHz at the output of the oscillator is

to be programmed. Therefore the required values for HS_DIV and N1 have to be chosen. The frequency of the DCO f_{DCO} must be between 4.85 and 5.67 GHz.

For a low power consumption HS_DIV should be selected as high as possible and N1 as low as possible. Furthermore the DCO frequency f_{DCO} should also be as low as possible.

For this examples the following values have been chosen as:

HS_DIV = 9
N1 = 6

$$f_{out} = \frac{f_{XTAL} * RFREQ}{HS\_DIV * N1} = \frac{f_{DCO}}{HS\_DIV * N1}$$

$f_{DCO} = f_{out} * HS\_DIV * N1 = 100\,MHz * 9 * 6 = 5400\,MHz$

Thus f_{DCO} is within the valid range between 4.85 and 5.67 GHz. RFREQ multiplied by the referency frequency f_{XTAL} has to yield 5400 MHz and hence:

$$RFREQ = \frac{5400\,MHz}{f_{XTAL}} = \frac{5400\,MHz}{114,3363533\,MHz}$$
$$= 47,229073204$$

f_{out}	Output frequency
f_{XTAL}	Reference frequency (= 114.3363533 MHz)
f_{DCO}	Output frequency of DCO
HS_DIV	High-speed divider
N1	Output divider N1
RFREQ	Multiplier

PROGRAMMING

There are two ways to set the frequency of the iC213 module. Three HEX switches with 4 bit each (= 12 bit) allow the selection from a list of pre-defined frequencies. Alternatively an I²C interface allows this module to be programmed directly. Plus the trimmer P1 allows a fine-tuning of the VCO frequency.

Selectable frequencies
Figure 5 gives the list of frequencies that can be selected via the three HEX switches. The frequencies rise exponential. Thus an even distribution across the whole frequency range from 39.3 kHz up to 1 GHz is granted.

Divider	256		256		64		1		1	
HEX-Sw.	0x000 - 0x1FB		0x1FB - 0x57F		0x57F - 0x903		0x903 - 0xC87		0xC87 - 0xFFF	
Decade	40.5 kHz - 100 kHz		100 kHz - 1 MHz		1 MHz - 10 MHz		10 MHz - 100 MHz		100 MHz - 1 GHz	
	HEX	f / kHz	HEX	f / kHz	HEX	f / MHz	HEX	f / MHz	HEX	f / MHz
			0x1FB	100,0	0x57F	1,000	0x903	10,00	0xC87	100,0
			0x1FC	100,5	0x580	1,005	0x904	10,05	0xC88	100,5
			0x1FD	101,0	0x581	1,010	0x905	10,10	0xC89	101,0
			:	:	:	:	:	:	:	:
			0x2C1	199,0	0x645	1,990	0x9C9	19,90	0xD4D	199,0
			0x2C2	199,5	0x646	1,995	0x9CA	19,95	0xD4E	199,5
			0x2C3	200,0	0x647	2,000	0x9CB	20,00	0xD4F	200,0
	0x000	39,3	0x2C4	201,0	0x648	2,010	0x9CC	20,10	0xD50	201,0
	0x001	39,4	0x2C5	202,0	0x649	2,020	0x9CD	20,20	0xD51	202,0
	:	:	:	:	:	:	:	:	:	:
	0x195	79,8	0x519	798,0	0x89D	7,980	0xC21	79,80	0xFA5	798,0
	0x196	79,9	0x51A	799,0	0x89E	7,990	0xC22	79,90	0xFA6	799,0
	0x197	80,0	0x51B	800,0	0x89F	8,000	0xC23	80,00	0xFA7	800,0
	0x198	80,1	0x51C	802,0	0x8A0	8,020	0xC24	80,20	0xFA8	802,0
	0x199	80,2	0x51D	804,0	0x8A1	8,040	0xC25	80,40	0xFA9	804,0
	:	:	:	:	:	:	:	:	:	:
	0x1F9	99,7	0x57D	996,0	0x901	9,960	0xC85	99,60	0xFEE	942,0
	0x1FA	99,8	0x57E	998,0	0x902	9,980	0xC86	99,80	0xFEF	944,0
	0x1FB	100,0	0x57F	1000,0	0x903	10,000	0xC87	100,00	0xFF0	970,0
									0xFF1	972,0
									0xFF2	974,0
									:	:
									0xFFD	996,0
									0xFFE	998,0
									0xFFF	1000,0

Figure 5: Frequency list

The three HEX switches equal 4 bit each = 1 nibble and are designated as *high* (high nibble), *mid* (middle nibble) and *low* (low nibble). If for example *high* = 6, *mid* = 4, *low* = 7 are chosen, this relates to **0x647** and hence a frequency of 2 MHz.

Programming via I²C

Programming the module via the I²C interface there are two ways to set a frequency.

First one can also select one of the pre-defined frequencies from Table 5. Second an arbitrary frequency between 39.0625 kHz and 1417.5 MHz can be programmed. In both cases the relevant registers have to be set accordingly via the I²C interface.

The I²C bus address is set between 40 (0x28) and 43 (0x2B) by means of soldering bridges JP3 and JP4. The maximum bus frequency is 400 kHz.

JP3	JP4	Addr
open	open	40 (0x28)
open	close	41 (0x29)
close	open	42 (0x2A)
close	close	43 (0x2B)

Table 5: I²C bus address

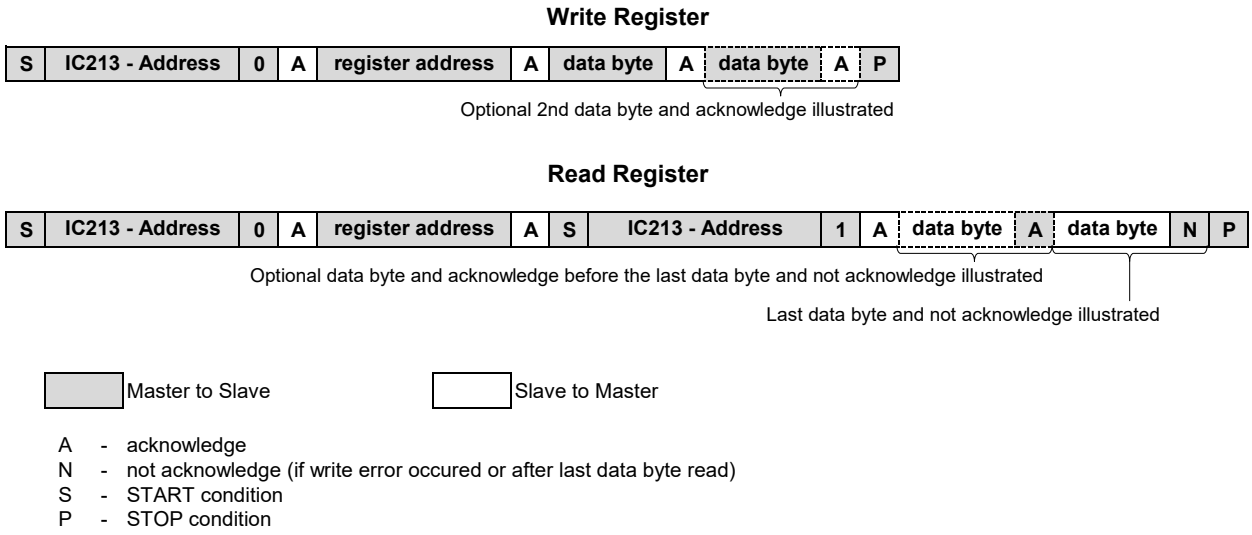


Figure 6: I²C communication

Write

There are 25 registers for programming the frequency. The programming procedure is like with I²C EEPROMs. A transmission starts with sending the START signal and the module address. The first byte contains the register address which is to be written. Following the data byte for this register. An internal address counter allows multiple consecutive bytes to be written. Sending the STOP signal ends the transmission.

Read

For reading the registers, following the I²C START signal and module address, first the address of the register to be read is transmitted. Following this a REPEATED START signal is sent with the R/nW-Bit in the address byte set. Now the register can be read. The internal address counter again allows consecutive registers to be read. The master acknowledges the last byte to be read with *Not Acknowledge* and sends the STOP signal.

Register description

Register / Addr.		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
0	0x00	VER_NR[7:0]								Software version
1	0x01	VER_NR[15:8]								
2	0x02	0	0	0	VER_D[4:0]					Version day
3	0x03	0	0	0	0	VER_M[3:0]				Version month
4	0x04	VER_Y[7:0]								Version year
5	0x05	VER_Y[15:8]								

Table 6: Register map of the µC (version number)

Firmware version
The first six registers of the iC213 module are read-only. These registers hold the version number and respective data of the µC firmware.

VER_NR[15:0] - Software version
Contains the 16 bit version number of the µC software.

VER_D[4:0] - Version date day
Contains a 5 bit value giving the day of version date.

VER_M[3:0] - Version date month
Contains a 4 bit value giving the month of the version date.

VER_Y[15:0] - Version date year
Contains a 16 bit value giving the year of the version date.

Command register
Via the command registers commands are sent to the iC213 module. Currently only a single command is implemented.

Register / Addr.		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
13	0x0D	0	0	0	0	0	0	0	S2H	

Table 7: Command register

S2H - Set to HEX
Setting this bit to *1* takes the current setting of the HEX switches and sets the modules to the corresponding frequency.

HEX switch settings
Register 14 and 15 are read-only. They contain the 12 bit HEX switch setting. The value read from this register does not necessarily represent the frequency number currently set.

Register / Addr.		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
14	0x0E	HEX_ST[7:0]								HEX switch setting
15	0x0F	0	0	0	0	HEX_ST[11:8]				

Table 8: Register for HEX switch setting

Frequency number
Registers 16 and 17 hold the 12 bit value of the set frequency number from Figure 5. Using this register the frequency number can be set or the current frequncy number can be read. If the programmed frequency number is not one of the listed ones, 0xFFFF is returned.

Register / Addr.		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
16	0x10	FREQ_NR[7:0]								Frequency number
17	0x11	0	0	0	0	FREQ_NR[11:8]				

Table 9: Register for 12 bit frequency number

Oscillator calibration bytes
The six registers of the *Oscillator Calibration Bytes* represent the settings of the intrinsic oscillator. Setting these registers via I^2C directly manipulates the settings of the oscillator device. The output frequency of the module however also depends on the settings of the divider (register 24).

The following table shows the register assembly:

Register / Addr.		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
18	0x12	HS_DIV[2:0]			N1[6:2]					
19	0x13	N1[1:0]		RFREQ[37:32]						
20	0x14	RFREQ[31:24]								
21	0x15	RFREQ[23:16]								
22	0x16	RFREQ[15:8]								
23	0x17	RFREQ[7:0]								

Table 10: *Oscillator Calibration Bytes* register

HS_DIV[2:0] - High-speed divider
Using this 3 bit the first frequency divider following the DCO is set.

N1[6:0] - Output divider
These 7 bit set the output divider. N1 must hold only even values between 1 and 128, e.g. 2, 4, 6, etc. up to 128. The only exception is the division factor of 1. Invalid values are rounded up to the next even value.

RFREQ[37:0] - Reference Frequency
RFREQ contains the multiplier for the DCO. The upper 10 bit contain the digits to the left of the decimal point and the lower 28 bit the digits to the right of the decimal point.

ET[1:0] - External divider

ET[1:0]	Divider
00 / 01	1
10	64
11	256

Table 11: Truth table for the external divider

External divider
Using this register the external clock divider of the iC213 module is set. The divider can be set to 1/1, 1/64 or 1/256.

Register / Addr.		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description
24	0x18	0	0	0	0	0	0	ET[1:0]		external divider

Table 12: Register for the external divider

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2012-03-19		Initial release	all

Rel.	Rel. Date*	Chapter	Modification	Page
A2	2023-12-12		Re-ordered and partially re-named chapters.	1–4
		BOARD	New product image	1
		PIN CONFIGURATION	Added populated PCB drawing, added connectors on the PCB Table, moved J1 configuration Table into Pin configuration J1 Figure.	4
		PROGRAMMING	Fixed content of Frequency list around the $2 * 10^n$ MHz values. Fixed example HEX switches values. Added I^2C bus address table. Improved I^2C communication Figure.	7, 8
		all	Fixed typos and improved readability.	all

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Order Designation
iC213	iC213

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